



April 2000
Revised April 2003

NC7WZ02

TinyLogic® UHS Dual 2-Input NOR Gate

General Description

The NC7WZ02 is a dual 2-Input NOR Gate from Fairchild's Ultra High Speed Series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} range. The inputs and output are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 7V independent of V_{CC} operating voltage.

Features

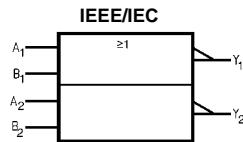
- Space saving US8 surface mount package
- MicroPak™ leadless package
- Ultra High Speed: t_{PD} 2.4 ns typ into 50 pF at 5V V_{CC}
- High Output Drive: ± 24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range: 1.65V to 5.5V
- Matches the performance of LCX when operated at 3.3V V_{CC}
- Power down high impedance inputs/output
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7WZ02K8X	MAB08A	WZ02	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3k Units on Tape and Reel
NC7WZ02L8X (Preliminary)	MAC08A	P5	8-Lead MicroPak, 1.6 mm Wide	5k Units on Tape and Reel

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MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

NC7WZ02

Logic Symbol**Pin Descriptions**

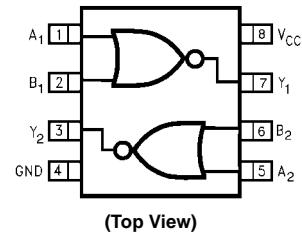
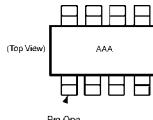
Pin Names	Description
A _n , B _n	Inputs
Y _n	Output

Function Table

$$Y = \overline{A + B}$$

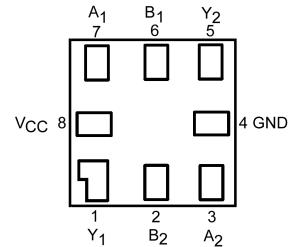
Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

Connection Diagrams**Pin One Orientation Diagram**

AAA represents Product Code Top Mark - see ordering code

Note: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right. Pin One is the lower left pin (see diagram).

Pad Assignments for MicroPak

(Top Thru View)

Absolute Maximum Ratings ^(Note 1)			Recommended Operating Conditions ^(Note 2)				
Supply Voltage (V_{CC})	-0.5V to +7V		Supply Voltage Operating (V_{CC})	1.65V to 5.5V			
DC Input Voltage (V_{IN})	-0.5V to +7V		Supply Voltage Data Retention (V_{CC})	1.5V to 5.5V			
DC Output Voltage (V_{OUT})	-0.5V to +7V		Input Voltage (V_{IN})	0V to 5.5V			
DC Input Diode Current (I_{IK})			Output Voltage (V_{OUT})	0V to V_{CC}			
@ $V_{IN} < -0.5V$	-50 mA		Operating Temperature (T_A)	-40°C to +85°C			
DC Output Diode Current (I_{OK})			Input Rise and Fall Time (t_r, t_f)				
@ $V_{OUT} < -0.5V$	-50 mA		$V_{CC} @ 1.8V \pm 0.15V, 2.5V \pm 0.2V$	0 ns/V to 20 ns/V			
DC Output Current (I_{OUT})	± 50 mA		$V_{CC} @ 3.3V \pm 0.3V$	0 ns/V to 10 ns/V			
DC V_{CC}/GND Current (I_{CC}/I_{GND})	± 100 mA		$V_{CC} @ 5.0V \pm 0.5V$	0 ns to 5 ns/V			
Storage Temperature (T_{STG})	-65°C to +150°C		Thermal Resistance (θ_{JA})	250°C/W			
Junction Temperature under Bias (T_J)	150°C						
Junction Lead Temperature (T_L); (Soldering, 10 seconds)	260°C						
Power Dissipation (P_D) @ +85°C	250 mW						
Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.							
Note 2: Unused inputs must be held HIGH or LOW. They may not float.							
DC Electrical Characteristics							
Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ C$		Units	Conditions	
			Min	Typ			Max
V_{IH}	HIGH Level Input Voltage	1.65 to 1.95 2.3 to 5.5	0.75 V_{CC} 0.7 V_{CC}		0.75 V_{CC} 0.7 V_{CC}	V	
V_{IL}	LOW Level Input Voltage	1.65 to 1.95 2.3 to 5.5		0.25 V_{CC} 0.3 V_{CC}	0.25 V_{CC} 0.3 V_{CC}	V	
V_{OH}	HIGH Level Output Voltage	1.65 2.3 3.0 4.5	1.55 2.2 2.9 4.4	1.65 2.3 3.0 4.5	1.55 2.2 2.9 4.4	V	$V_{IN} = V_{IL}$ $I_{OH} = -100\mu A$
		1.65 2.3 3.0 3.0 4.5	1.29 1.9 2.4 2.3 3.8	1.52 2.15 2.80 2.68 4.20	1.29 1.9 2.4 2.3 3.8		
		1.65 2.3 3.0 3.0 4.5	1.29 1.9 2.4 2.3 3.8	1.52 2.15 2.80 2.68 4.20	1.29 1.9 2.4 2.3 3.8		
		1.65 2.3 3.0 3.0 4.5	0.08 0.10 0.15 0.22 0.22	0.24 0.3 0.4 0.55 0.55	0.24 0.3 0.4 0.55 0.55		
		1.65 2.3 3.0 3.0 4.5	0.0 0.1 0.1 0.1 0.1	0.1 0.1 0.1 0.1 0.1	0.1 0.1 0.1 0.1 0.1		
	LOW Level Output Voltage	1.65 2.3 3.0 4.5	0.0 0.0 0.0 0.0	0.1 0.1 0.1 0.1	0.1 0.1 0.1 0.1	V	$V_{IN} = V_{IH}$ $I_{OL} = 100\mu A$
		1.65 2.3 3.0 3.0 4.5	0.08 0.10 0.15 0.22 0.22	0.24 0.3 0.4 0.55 0.55	0.24 0.3 0.4 0.55 0.55		
		1.65 2.3 3.0 3.0 4.5	0.24 0.3 0.4 0.55 0.55	0.24 0.3 0.4 0.55 0.55	0.24 0.3 0.4 0.55 0.55		
		1.65 2.3 3.0 3.0 4.5	0.24 0.3 0.4 0.55 0.55	0.24 0.3 0.4 0.55 0.55	0.24 0.3 0.4 0.55 0.55		
		1.65 2.3 3.0 3.0 4.5	0.24 0.3 0.4 0.55 0.55	0.24 0.3 0.4 0.55 0.55	0.24 0.3 0.4 0.55 0.55		
I_{IN}	Input Leakage Current	0 to 5.5	±0.1	±1.0	µA	$V_{IN} = 5.5V, GND$	
I_{OFF}	Power Off Leakage Current	0.0	1	10	µA	V_{IN} or $V_{OUT} = 5.5V$	
I_{CC}	Quiescent Supply Current	1.65 to 5.5	1	10	µA	$V_{IN} = 5.5V, GND$	

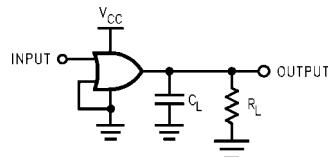
AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ C$			$T_A = -40^\circ C \text{ to } +85^\circ C$		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
t_{PLH}, t_{PHL}	Propagation Delay	1.8 ± 0.15	2.0	5.4	9.8	2.0	10	ns	$C_L = 15 \text{ pF}, R_L = 1 \text{ M}\Omega$	Figures 1, 3
		2.5 ± 0.2	1.2	3.3	5.4	1.2	5.8			
		3.3 ± 0.3	0.8	2.5	3.8	0.8	4.1			
		5.0 ± 0.5	0.5	2.0	3.0	0.5	3.3			
t_{PLH}, t_{PHL}	Propagation Delay	3.3 ± 0.3	1.2	3.1	4.6	1.2	5.0	ns	$C_L = 50 \text{ pF}, R_L = 500\Omega$	Figures 1, 3
		5.0 ± 0.5	0.8	2.4	3.7	0.8	4.0			
C_{IN}	Input Capacitance	0	2.5					pF		
C_{PD}	Power Dissipation Capacitance	3.3 5.0	13.5 17.5					pF	(Note 3)	Figure 2

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression:

$$I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC\text{static}}).$$

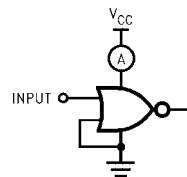
AC Loading and Waveforms



C_L includes load and stray capacitance

Input PRR = 1.0 MHz; $t_W = 500$ ns

FIGURE 1. AC Test Circuit



Input = AC Waveform; $t_f = t_r = 1.8$ ns;

PRR = 10 MHz; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

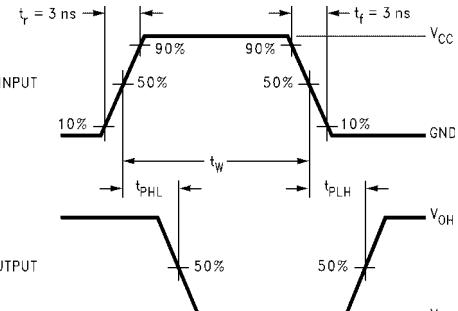


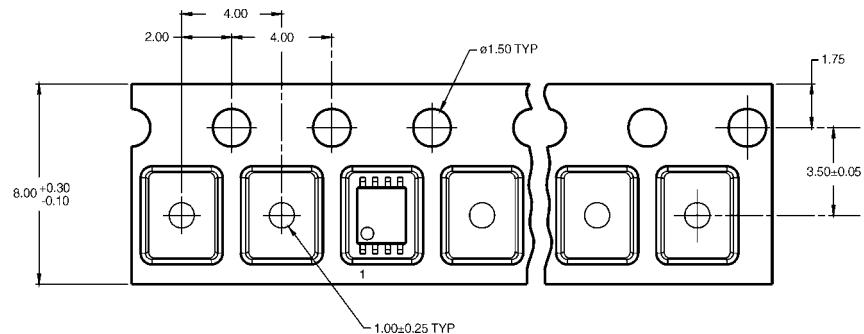
FIGURE 3. AC Waveforms

Tape and Reel Specification

TAPE FORMAT for US8

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
K8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

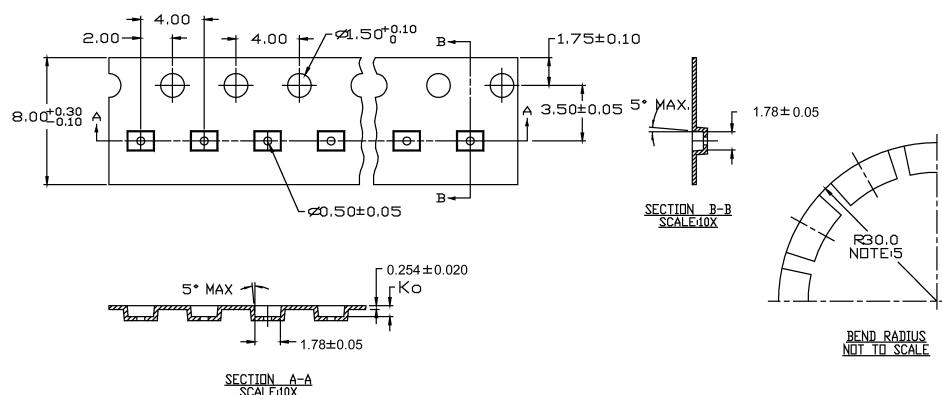
TAPE DIMENSIONS inches (millimeters)

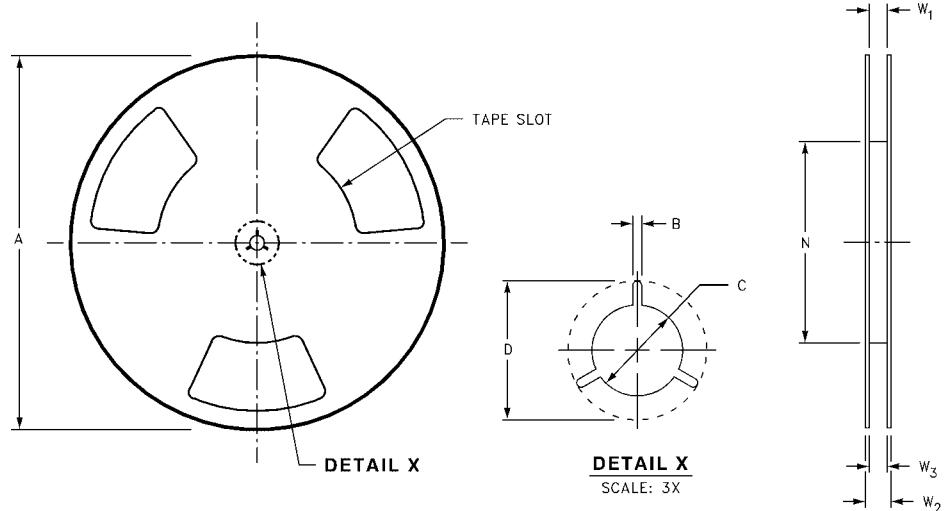


TAPE FORMAT for MicroPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)

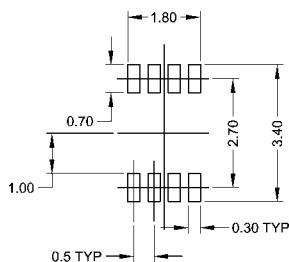
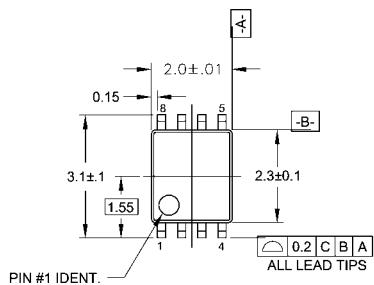


Tape and Reel Specification (Continued)**REEL DIMENSIONS** inches (millimeters)

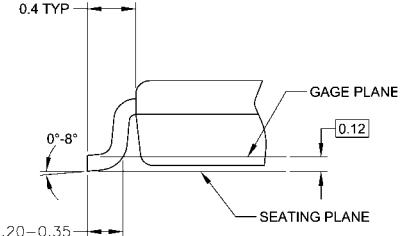
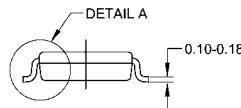
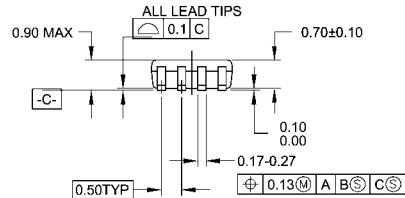
Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	$0.331 + 0.059/-0.000$ $(8.40 + 1.50/-0.00)$	0.567 (14.40)	$W1 + 0.078/-0.039$ $(W1 + 2.00/-1.00)$

NC7WZ02

Physical Dimensions inches (millimeters) unless otherwise noted



LAND PATTERN RECOMMENDATION



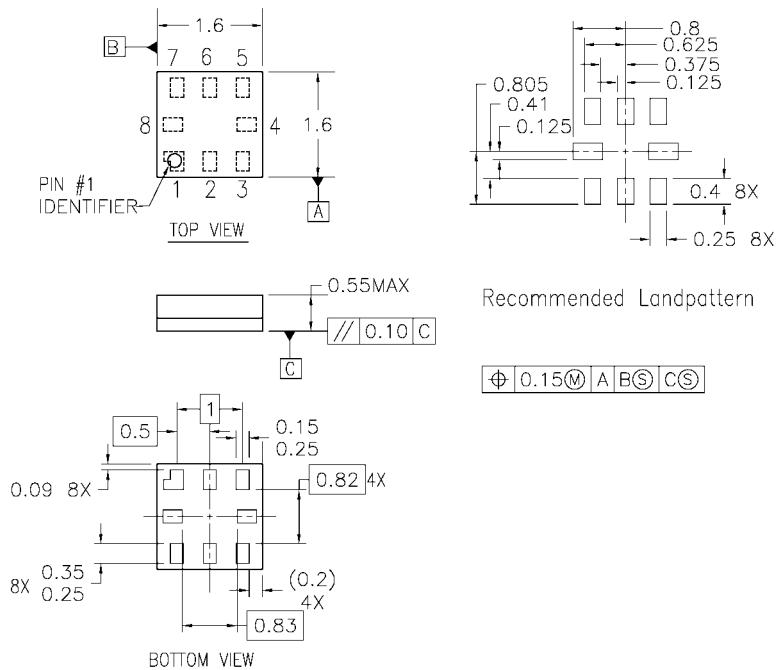
NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-187
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

DETAIL A

MAB08AREVC

8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide
Package Number MAB08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

Notes:

1. PACKAGE REGISTRATION WITH JEDEC IS ANTICIPATED
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994

MAC08AREVB

**8-Lead MicroPak, 1.6 mm Wide
Package Number MAC08A
(Preliminary)**

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