

SANYO

LC89080, 89080Q

Video Signal 3-Channel 8-Bit D/A Converter

Preliminary

Overview

The LC89080 and LC89080Q are high-speed current-output D/A converters. They feature 8-bit resolution, provide 3 channels on a single chip, and can be used in demodulators for high-speed signals such as video signals.

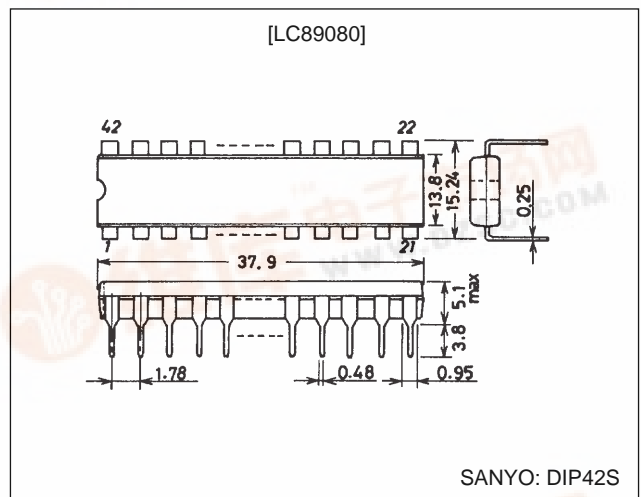
Features

- Resolution: 8 bits
- D/A converters: Three current-output D/A converter channels on a single chip
- Maximum conversion speed: 30 MSPS
- Error: ± 1.0 LSB (maximum)
- Power supply: +5 V single-voltage power supply
- Power dissipation: 330 mW
- Inputs: TTL compatible

Package Dimensions

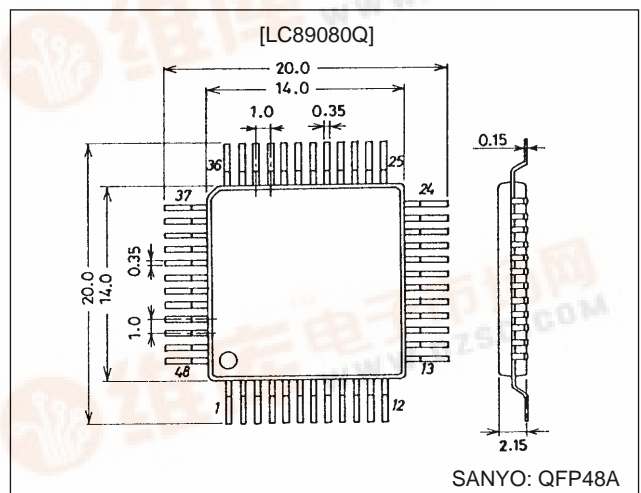
unit: mm

3025B-DIP42S



unit: mm

3052A-QFP48A



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Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$		-0.3 to +7.0	V
Input voltage	V_{IN}		-0.3 to $V_{DD} + 0.3$	V
Operating temperature	T_{opr}		-30 to +75	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to +125	$^\circ\text{C}$

Allowable Operating Ranges

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Reference voltage input	V_{REFIN}			1.0	2.0	V
Output resistance	R_O			75		Ω
Input high-level voltage	V_{IH}		2.2		$V_{DD} + 0.3$	V
Input low-level voltage	V_{IL}		-0.3		+0.8	V
Phase compensation capacitance	C_{comp}		1			μF

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{DD} = 5.0\text{ V}$, $V_{REFIN} = 1.0\text{ V}$, $R_{REF} = 300\ \Omega$, $R_O = 75\ \Omega$

Parameter	Symbol	Conditions	min	typ	max	Unit
Resolution	RES				8	Bits
Maximum conversion speed	$F_s\text{ max}$		30			MSPS
Power dissipation	P_d	$F_s = 30\text{ MSPS}$		330	400	mW
Zero-scale output voltage	V_{zero}	For each channel	-15	0	+15	mV
Full-scale output voltage	V_{full}	For each channel	0.92	1.00	1.08	V
Full-scale voltage ratio	FSR		0	4	8	%
Linearity error	I.L.	DC precision			± 1.0	LSB
Differential linearity error	D.L.	DC precision			± 0.5	LSB
Reference voltage output	V_{REFOUT}		0.99	1.00	1.01	V

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Pin Assignment LC89080 (DIP42S)

Pin No.	Symbol	Description
1	DV _{DD}	Digital system power supply (+5 V)
2	DA1	Channel A digital input (MSB)
3 to 8	DA2 to DA7	Channel A digital input
9	DA8	Channel A digital input (LSB)
10	DB1	Channel B digital input (MSB)
11 to 16	DB2 to DB7	Channel B digital input
17	DB8	Channel B digital input (LSB)
18	DC1	Channel C digital input (MSB)
19 to 24	DC2 to DC7	Channel C digital input
25	DC8	Channel C digital input (LSB)
26	CLK	Clock input
27	DV _{DD}	Digital system power supply (+5 V)
28	DGND	Digital system ground (0 V)
29	ICOB	Channel C negative output. Connect to A.GND through an output resistor R _O (usually 75 Ω).
30	ICO	Channel C positive output. Connect to A.GND through an output resistor R _O (usually 75 Ω).
31	AV _{DD}	Analog system power supply (+5 V)
32	IBOB	Channel B negative output. Connect to A.GND through an output resistor R _O (usually 75 Ω).
33	IBO	Channel B positive output. Connect to A.GND through an output resistor R _O (usually 75 Ω).
34	AGND	Analog system ground (0 V)
35	IAOB	Channel A negative output. Connect to A.GND through an output resistor R _O (usually 75 Ω).
36	IAO	Channel A positive output. Connect to A.GND through an output resistor R _O (usually 75 Ω).
37	AV _{DD}	Analog system power supply (+5 V)
38	COMP	Phase compensation capacitor. Connect a 1 μ F capacitor between this pin and ground.
39	I _{REF}	Reference current output. Connect a resistor that is 4 times the output resistance R _O to this pin.
40	V _{REFIN}	Reference voltage input. This input pin sets the analog output dynamic range.
41	V _{REFOUT}	Reference voltage output. The output voltage is set to 0.2 times V _{DD} by a resistor divider. When V _{DD} is 5.0 V, a 1.0 V reference voltage can be acquired from pin 40.
42	DGND	Digital system ground (0 V)

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Pin Assignment LC89080Q (QFP48A)

Pin No.	Symbol	Description
1 to 3	DA5 to 7	Channel A digital input
4	DA8	Channel A digital input (LSB)
5	DB1	Channel B digital input (MSB)
6	NC	Unused (no connection)
7 to 12	DB2 to DB7	Channel B digital input
13	DB8	Channel B digital input (LSB)
14	DC1	Channel C digital input (MSB)
15 to 18	DC2 to DC5	Channel C digital input
19	DV _{DD}	Digital system power supply (+5 V)
20	DC6	Channel C digital input
21	DC7	Channel C digital input
22	DC8	Channel C digital input (LSB)
23	CLK	Clock input
24	NC	Unused (no connection)
25	DV _{DD}	Digital system power supply (+5 V)
26	DGND	Digital system ground (0 V)
27	ICOB	Channel C negative output. Connect to A.GND through an output resistor R _O (usually 75 Ω).
28	ICO	Channel C positive output. Connect to A.GND through an output resistor R _O (usually 75 Ω).
29	AV _{DD}	Analog system power supply (+5 V)
30	AV _{DD}	Analog system power supply (+5 V)
31	IBOB	Channel B negative output. Connect to A.GND through an output resistor R _O (usually 75 Ω).
32	IBO	Channel B positive output. Connect to A.GND through an output resistor R _O (usually 75 Ω).
33	AGND	Analog system ground (0 V)
34	IAOB	Channel A negative output. Connect to A.GND through an output resistor R _O (usually 75 Ω).
35	IAO	Channel A positive output. Connect to A.GND through an output resistor R _O (usually 75 Ω).
36	AV _{DD}	Analog system power supply (+5 V)
37	COMP	Phase compensation capacitor. Connect a 1 μ F capacitor between this pin and ground.
38	NC	Unused (no connection)
39	I _{REF}	Reference current output. Connect a resistor that is 4 times the output resistance R _O to this pin.
40	V _{REFIN}	Reference voltage input. This input pin sets the analog output dynamic range.
41	V _{REFOUT}	Reference voltage output. The output voltage is set to 0.2 times V _{DD} by a resistor divider. When V _{DD} is 5.0 V, a 1.0 V reference voltage can be acquired from pin 40.
42	DGND	Digital system ground (0 V)
43	DV _{DD}	Digital system power supply (+5 V)
44	DV _{DD}	Digital system power supply (+5 V)
45	DA1	Channel A digital input (MSB)
46 to 48	DA2 to DA4	Channel A digital input

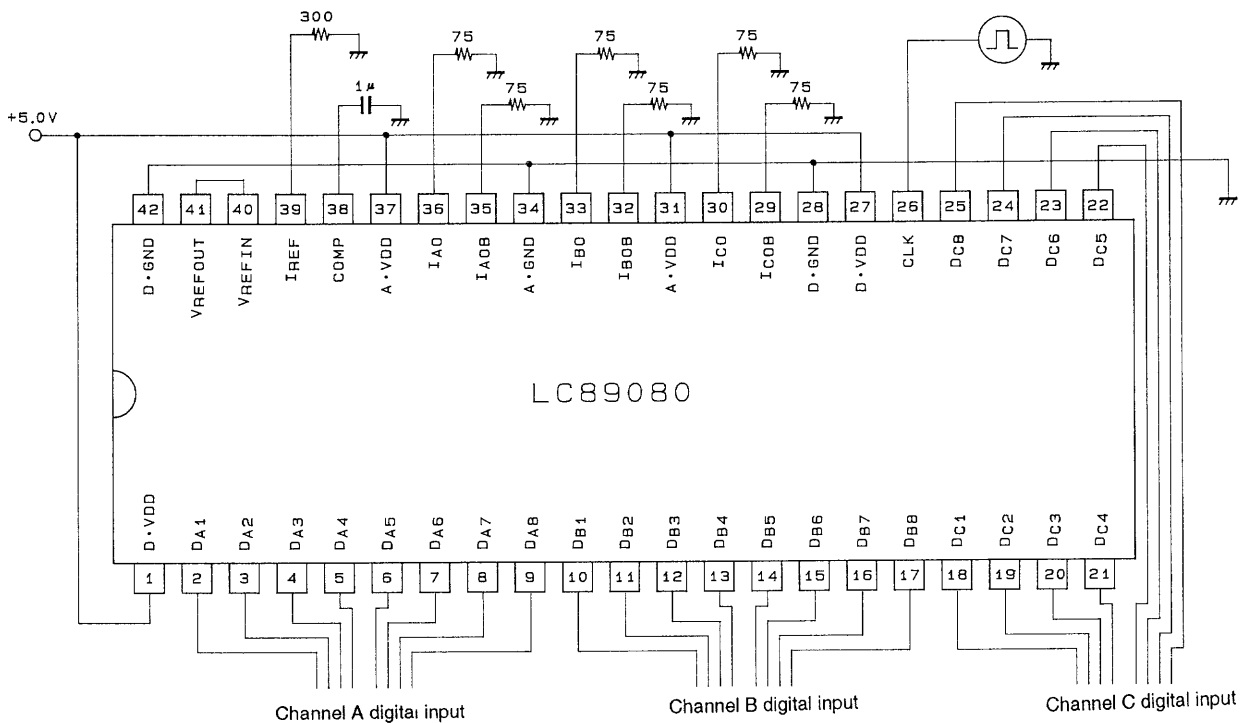
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LC89080 Operation

The LC89080 and LC89080Q include three current-matrix D/A converters on chip. These D/A converters each have 63 basic current cells (with current weight I) and two weighted current cells ($I/2$ and $I/4$). These current cells are turned on or off according to the input digital code (a binary code). The sum of these currents is output to the output pins (IO and IOB) and the output current is converted to a voltage by the output resistor (R_O) to acquire the analog output. The table shows the ideal relationship between the digital input and the analog output when V_{REFIN} is 1 V.

Digital input code								Analog output voltage	
D1 MSB	D2	D3	D4	D5	D6	D7	D8 LSB	IO (positive output)	IOB (negative output)
0	0	0	0	0	0	0	0	0	0.996
0	0	0	0	0	0	0	1	0.004	0.992
0	0	0	0	0	0	1	0	0.008	0.988
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	0.496	0.500
1	0	0	0	0	0	0	0	0.500	0.496
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	0	1	0.988	0.008
1	1	1	1	1	1	1	0	0.992	0.004
1	1	1	1	1	1	1	1	0.996	0

Sample Application Circuit: LC89080

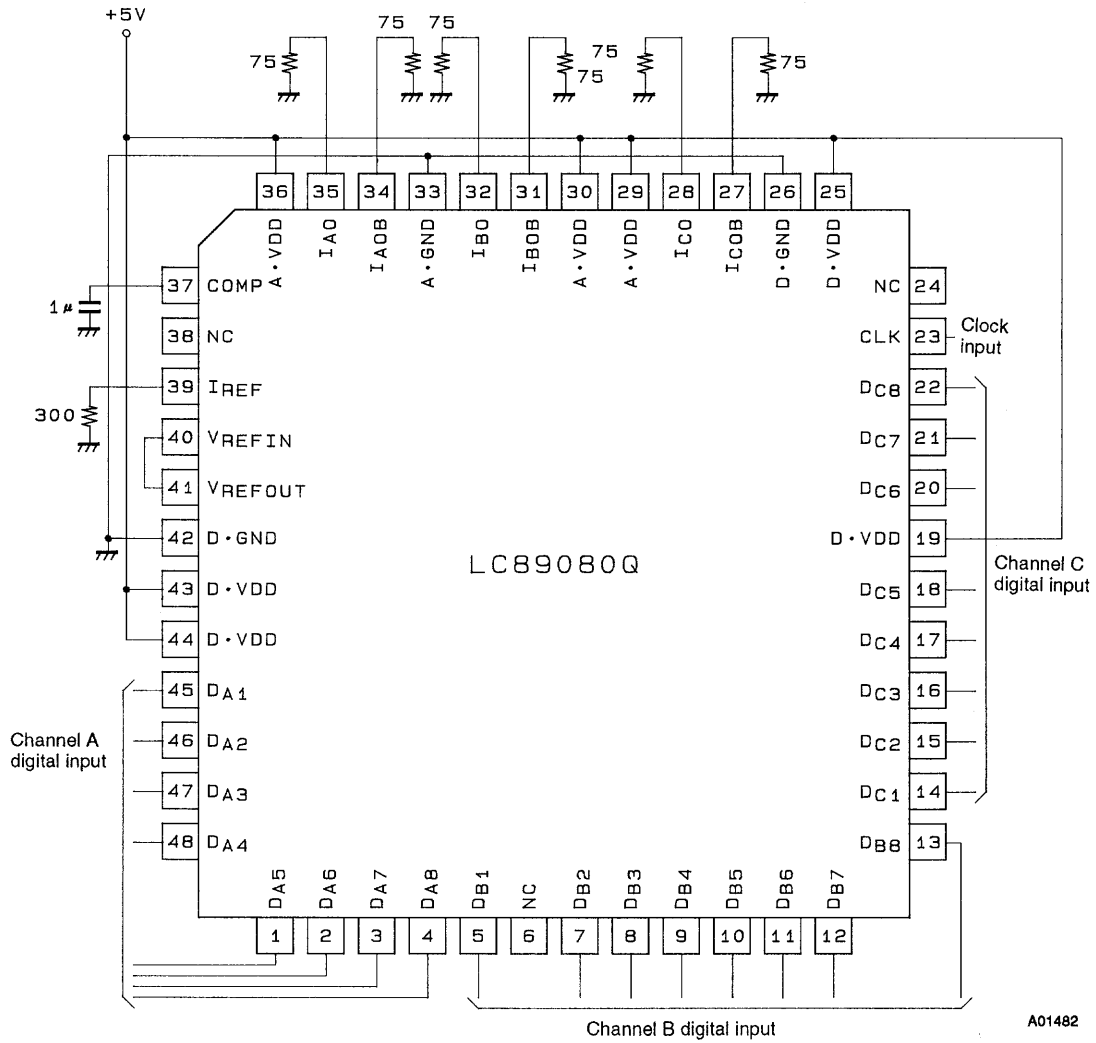


Unit (resistance:Ω, capacitance:F)

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Sample Application Circuit: LC89080Q

Application circuit in which the output resistance is $75\ \Omega$ and the internally generated 1-V reference voltage is used.



Unit (resistance: Ω , capacitance: F)

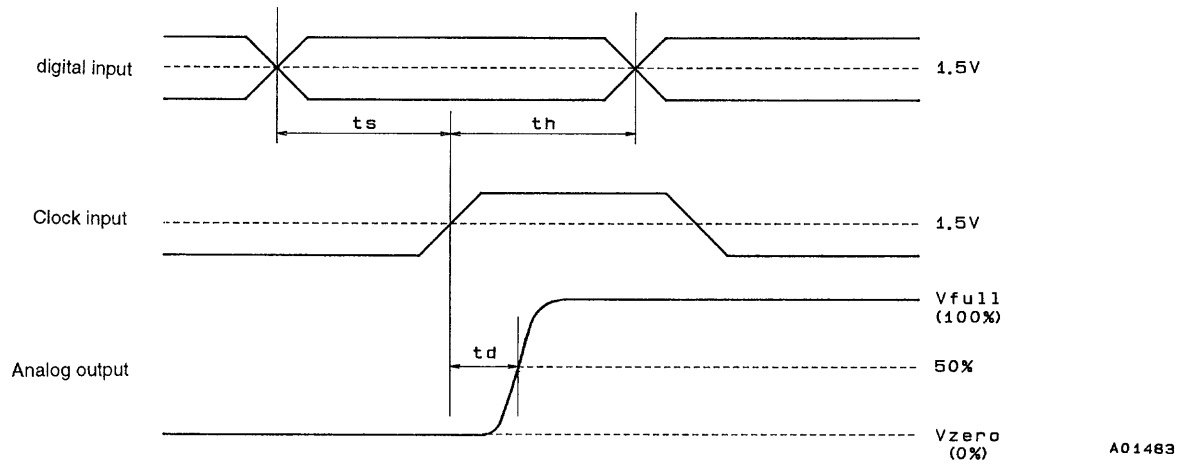
AC Characteristics at $T_a = -30$ to 70°C , $V_{DD} = 4.5$ to 5.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Data setup time	t_s		15			ns
Data hold time	t_h		15			ns
Output delay time	t_d			10		ns

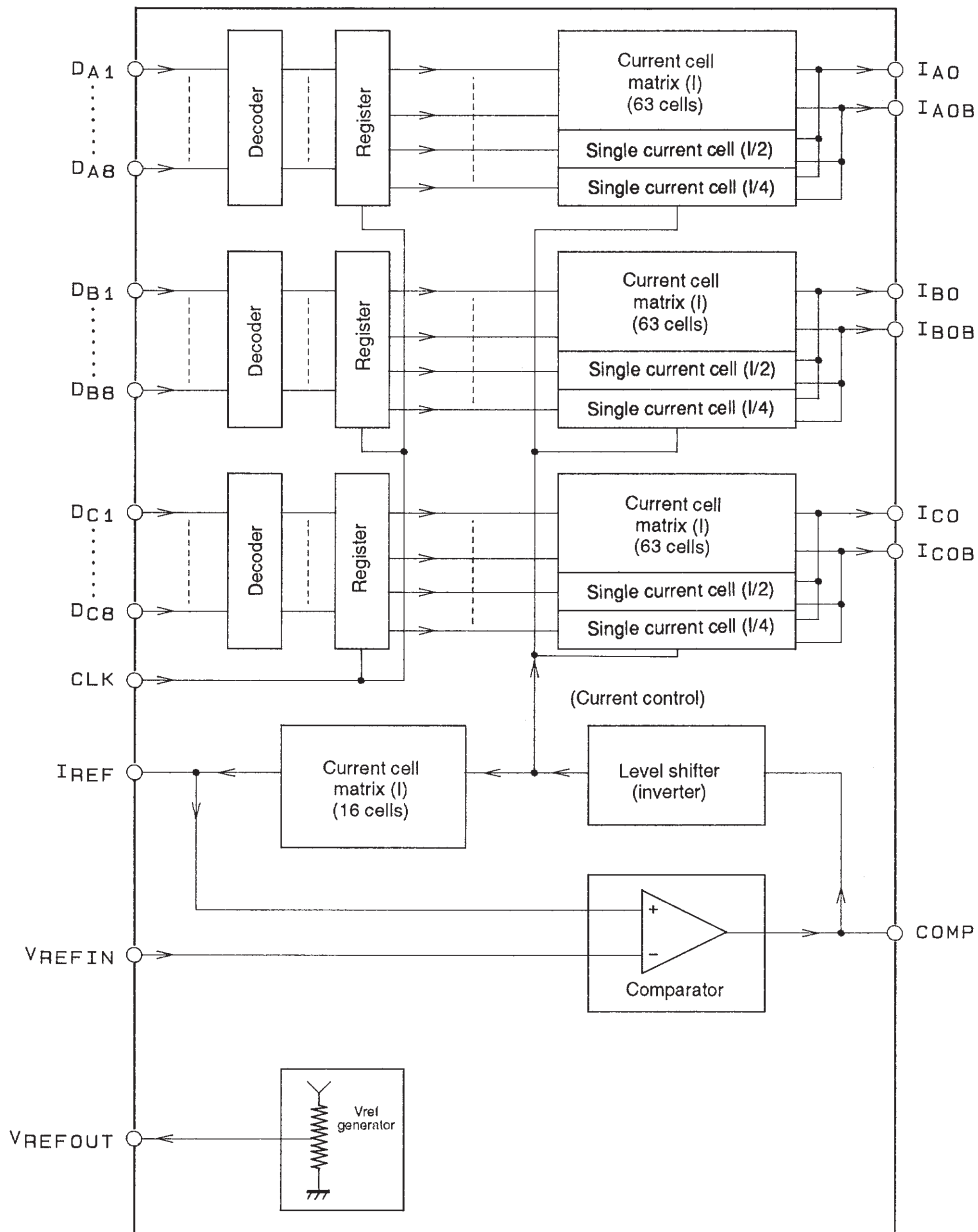
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Timing Chart

The digital inputs for all 3 channels are acquired on the rising edge of the clock input, after which the corresponding analog voltages are output.



Block Diagram



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