CMOS LSI

SANYO

No. ※4854A

LC89517K

Built-in Subcode Interface CD-ROM/CD-I Error Correction LSI

Preliminary

Overview

The LC89517K is a CD-ROM/CD-I error correction LSI that integrates the functions provided by the improved version of the LC89515 and a sub-code function in a single chip. The improved version of the LC89515 additionally supports double speed operation.

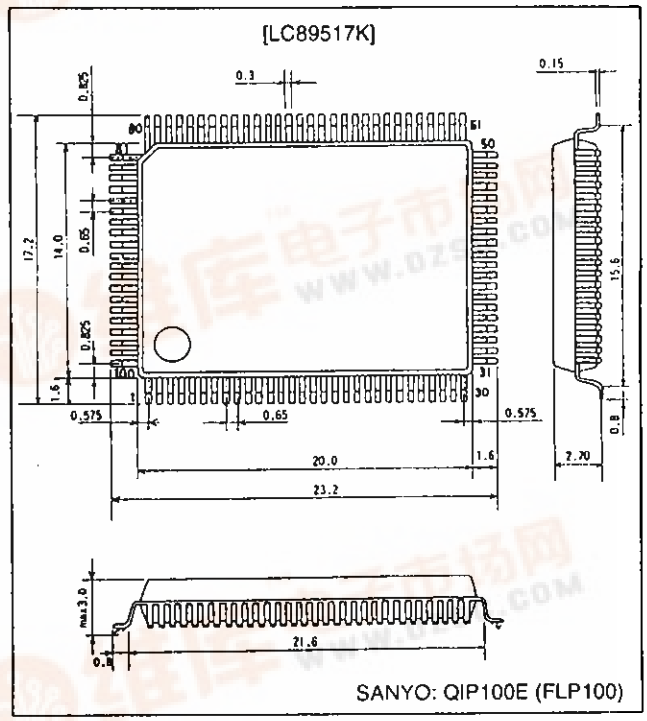
Features

- Support for double speed operation (selectable by setting an internal register) at an operating frequency of 16.9344 MHz
- Built-in 12-byte FIFO for transfers from the system microcontroller to the host computer
- Built-in 12-byte FIFO for transfers from the host computer to the system microcontroller
- Direct connection to the LC8955 (an ADPCM decoder LSI) and the LC8953 (a 68000 CPU peripheral interface LSI)
- Sub-code data can be written to buffer RAM simply by connecting the CD DSP sub-code pin. This allows the system microcontroller to read the sub-code values.
- The system microcontroller can access buffer RAM through the LC89517K.
- Pseudo-SRAM support (An interface circuit is built in.)

Package Dimensions

unit: mm

3151-QIP100E (FLP100)



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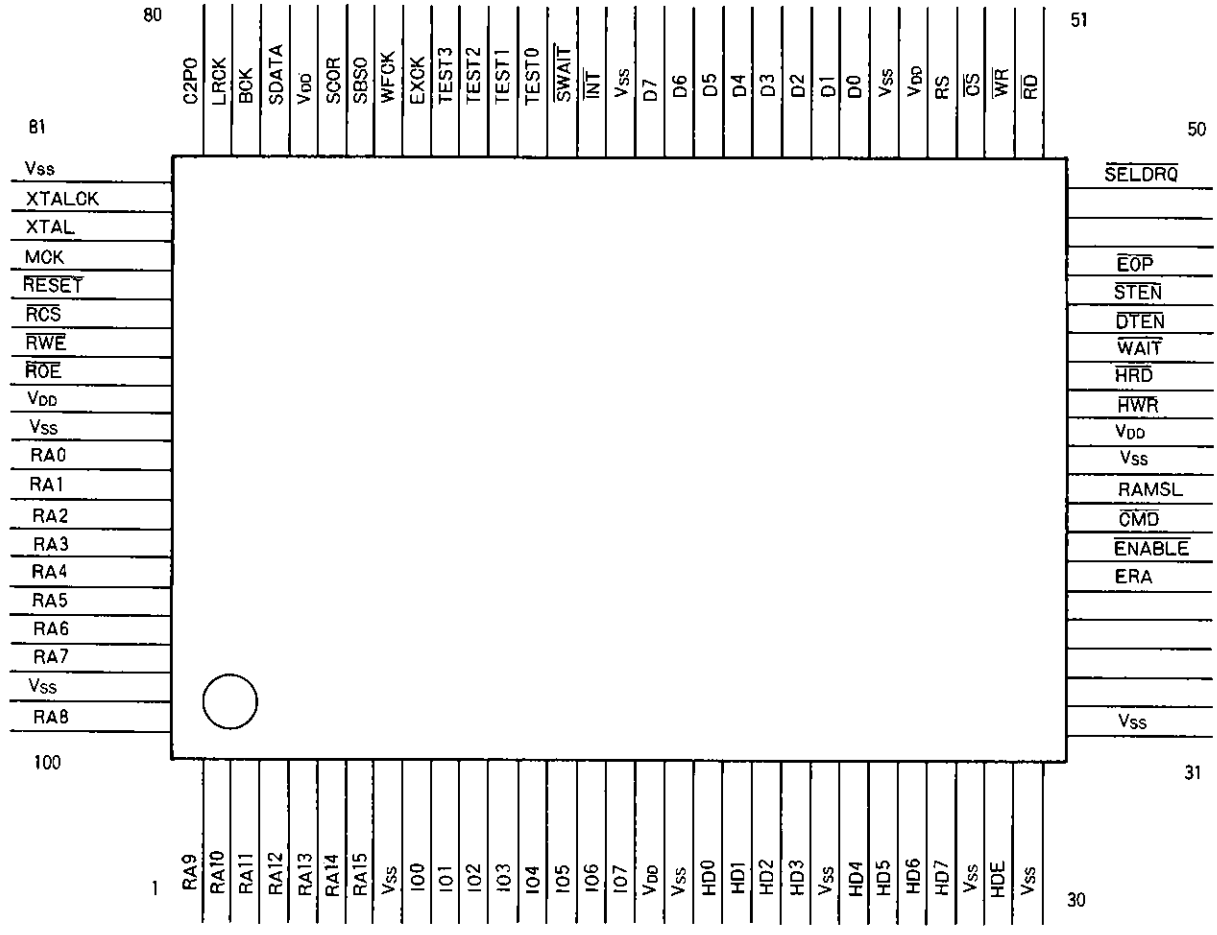
Pin Assignment



Top view

Pin Functions

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: Unconnected pin

Pin No.	Pin	Type	Function
1	RA9	O	Data buffer RAM address signal outputs
2	RA10	O	
3	RA11	O	
4	RA12	O	
5	RA13	O	
6	RA14	O	
7	RA15	O	
8	V_{SS}	P	
9	IO0	B	Data buffer RAM data signals These pins have built-in pull-up resistors.
10	IO1	B	
11	IO2	B	
12	IO3	B	
13	IO4	B	
14	IO5	B	
15	IO6	B	
16	IO7	B	
17	V_{DD}	P	
18	V_{SS}	P	
19	HD0	B	Host data signals These pins have built-in pull-up resistors.
20	HD1	B	
21	HD2	B	
22	HD3	B	
23	V_{SS}	P	
24	HD4	B	Host data signals These pins have built-in pull-up resistors
25	HD5	B	
26	HD6	B	
27	HD7	B	
28	V_{SS}	P	
29	HDE	O	Host erasure flag output (Connect to V_{DD} if unused.)
30	V_{SS}	P	
31	V_{SS}	P	
32		NC	
33		NC	
34		NC	
35		NC	
36	ERA	B	Data buffer RAM erasure flag signal (Connect to V_{SS} if unused.)
37	$\overline{\text{ENABLE}}$	I	Chip select signal input (from host computer)
38	$\overline{\text{CMD}}$	I	Host command/data selection signal
39	RAMSL	I	DRAM/SRAM switch
40	V_{SS}	P	
41	V_{DD}	P	
42	$\overline{\text{HWR}}$	I	Host data write signal input
43	$\overline{\text{HRD}}$	I	Host data read signal input
44	$\overline{\text{WAIT}}$	O	Wait signal output (to host). This pin can be switched to function as the DRQ signal.
45	$\overline{\text{DTEN}}$	O	Data enable signal output
46	$\overline{\text{STEN}}$	O	Status enable signal output
47	$\overline{\text{EOP}}$	O	End of process signal output. Used during DMA transfers.
48		NC	
49		NC	
50	$\overline{\text{SELDRQ}}$	I	Selects the mode for data transfers to the host.

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Pin No.	Pin	Type	Function
51	$\overline{RD}$	I	Microcontroller data read signal input
52	$\overline{WR}$	I	Microcontroller data write signal input
53	$\overline{CS}$	I	Chip select signal input (from microcontroller)
54	RS	I	Register selection signal
55	V_{DD}	P	
56	V_{SS}	P	
57	D0	B	Microcontroller data signals. These pins have built-in pull-up resistors.
58	D1	B	
59	D2	B	
60	D3	B	
61	D4	B	
62	D5	B	
63	D6	B	
64	D7	B	
65	V_{SS}	P	
66	$\overline{INT}$	O	Interrupt request signal output (to the microcontroller) This pin is an open drain output with a built-in pull-up resistor.
67	$\overline{SWAIT}$	O	System microcontroller wait signal
68	TEST0	I	Test inputs. These pins should be tied low during normal operation.
69	TEST1	I	
70	TEST2	I	
71	TEST3	I	
72	EXCK	O	Sub-code I/O
73	WFCK	I	
74	SBSO	I	
75	SCOR	I	
76	V_{DD}	P	
77	SDATA	I	Serial data input
78	BCK	I	Serial data input clock
79	LRCK	I	44.1 kHz strobe signal input
80	C2PO	I	C2 pointer input
81	V_{SS}	P	
82	XTALCK	I	Crystal oscillator input
83	XTAL	O	Crystal oscillator output
84	MCK	O	Outputs the XTALCK input signal divided by 2.
85	$\overline{RESET}$	I	Chip select signal input
86	$\overline{RCS}$	O	RAM chip select
87	$\overline{RWE}$	O	RAM data write signal
88	$\overline{ROE}$	O	RAM data read signal
89	V_{DD}	P	
90	V_{SS}	P	
91	RA0	O	Data buffer RAM address signal outputs
92	RA1	O	
93	RA2	O	
94	RA3	O	
95	RA4	O	
96	RA5	O	
97	RA6	O	
98	RA7	O	
99	V_{SS}	P	
100	RA8	O	Data buffer RAM address signal output

Specifications

Absolute Maximum Ratings at V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	Ta = 25°C	−0.3 to +7.0	V
I/O voltage	V_I, V_O	Ta = 25°C	−0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	350	mW
Operating temperature	Topr		−30 to +70	°C
Storage temperature	Tstg		−55 to +125	°C
Soldering temperature		10 seconds	260	°C

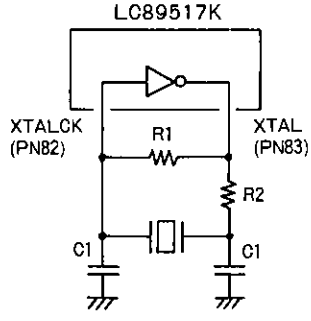
Allowable Operating Ranges at Ta = −30 to +70°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		3.5	5.0	5.5	V
Input voltage range	V_{IN}		0		V_{DD}	V

DC Characteristics at Ta = −30 to +70°C, V_{SS} = 0 V, V_{DD} = 3.5 to 5.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high level voltage	V_{IH1}	All input pins other than (1) and XTALCK	2.2			V
Input low level voltage	V_{IL1}				0.8	V
Input high level voltage	V_{IH2}	$\overline{RESET}$, all bus pins ($\overline{HRD}$, $\overline{HWR}$, $\overline{ENABLE}$, $\overline{CMD}$, $\overline{RD}$, $\overline{CS}$, $\overline{WR}$, WFCK, SBSO, SCOR) (1)	2.5			V
Input low level voltage	V_{IL2}				0.6	V
Output high level voltage	V_{OH1}	I_{OH1} = −2 mA: All output pins (including bus pins) other than (2) and XTALCK	2.4			V
Output low level voltage	V_{OL1}	I_{OL1} = 2 mA: All output pins (including bus pins) other than (2) and XTALCK			0.4	V
Output low level voltage	V_{OL2}	I_{OL2} = 2 mA: $\overline{INT}$ (open drain circuit with pull-up resistor) (2)			0.4	V
Output high level voltage	V_{OH3}	I_{OH3} = −6 mA: HD0 to HD7	2.4			V
Output low level voltage	V_{OL3}	I_{OL3} = 6 mA: HD0 to HD7			0.4	V
Input leakage current	I_L	V_I = V_{SS}, V_{DD}: All input pins	−25		+25	μA
Pull-up resistance	R_{UP}	All bus pins, $\overline{INT}$	10	20	40	kΩ

Sample Recommended Oscillator Circuit



R1 = 120 kΩ
R2 = 47 Ω
C1 = 30 pF
Crystal oscillator frequency = 16.9344 MHz