

SANYO

LC895925

Signal Processing LSI for CD-R Drives

Preliminary

Overview

The LC895925 provides the following signal processing functions for CD-R drives: CD-ROM decoding/encoding (complete with ECC processing for the former), subcode decoding/encoding, CD encoding, ATIP decoding, CLV servo, and SCSI interface registers.

Features

- CD-ROM decoding/encoding complete with error detection and error correction
- Subcode decoding/encoding complete with error correction
- ATIP decoding and CRC checking for both encoding and decoding
- CLV servo control using ATIP data during encoding
- CIRC code insertion and EFM modulation during encoding
- Support for PCA random EFM output during encoding
- Support for CD-ReWritable (CD-RW) Write Strategy signal output
- Access to buffer RAM from microcontroller via LC895925
- Built-in SCSI interface
- Speeds of 12× for decoding and 4× for encoding
 - Frequencies
 - Decoding: 17.2872 MHz
 - Encoding: 17.2872 MHz without Write Strategy support
 - 69.1488 MHz with Write Strategy support
- Transfers speeds of 10 megabytes/s (synchronous) and 5 megabytes/s (asynchronous) with 16 80-ns DRAMs *1

- Buffer RAM sizes between 1 and 32 megabits (using 16-bit DRAMs)
- User control over sizes of CD main channel, C2 flag, and subcode areas in buffer RAM
- Built-in batch transfer function for transferring entire CD main channel, C2 flag, or subcode area in a single operation
- Built-in multiblock transfer function for transferring multiple blocks in a single operation

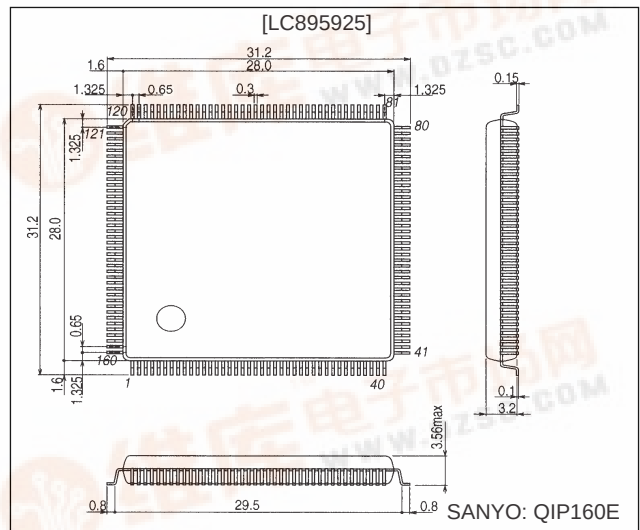
Notes:

1. Using a SCSI master clock of 20 MHz with speeds up to 8×.
2. Using a SCSI master clock of 17.2872 MHz with speeds up to 4×.

Package Dimensions

unit: mm

3153A-QFP160E



LC895925

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum power supply voltage	$V_{DD\text{ max}}$		-0.3 to +7.0	V
I/O voltage	V_I, V_O		-0.3 to $V_{DD}+0.3$	V
Maximum power dissipation	$P_d\text{ max}$	$T_a \leq 70^\circ\text{C}$	600	mW
Operating temperature	T_{opr}		-30 to +70	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +125	$^\circ\text{C}$
Solder resistance		10 seconds	260	$^\circ\text{C}$

Permissible Operating Range at $T_a = -30$ to $+70^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage range	V_{IN}		0		V_{DD}	V

DC Characteristics at $T_a = -30$ to $+70^\circ\text{C}$, $V_{SS} = 0\text{ V}$, $V_{DD} = 4.5$ to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high level voltage	V_{IH}	TTL levels, for pin types 1 and 6	2.2			V
Input low level voltage	V_{IL}				0.8	V
Input high level voltage	V_{IH}	TTL levels, for pin type 4, with pull-up resistors	2.2			V
Input low level voltage	V_{IL}				0.8	V
Input high [†] level voltage	V_{IH}	TTL levels, for pin 0 and 7, with Schmitt inputs	2.5			V
Input low level voltage	V_{IL}				0.6	V
Output high level voltage	V_{OH}	$I_{OH} = -2\text{ mA}$, for pin type 3	$V_{DD} - 2.1$			V
Output low level voltage	V_{OL}	$I_{OL} = 2\text{ mA}$, for pin type 3			0.4	V
Output high level voltage	V_{OH}	$I_{OH} = -2\text{ mA}$, for pin types 2, 4, and 6	$V_{DD} - 2.1$			V
Output low level voltage	V_{OL}	$I_{OL} = 2\text{ mA}$, for pin types 2, 4, and 6			0.4	V
Output high level voltage	V_{OH}	$I_{OH} = -48\text{ mA}$, for pin type 7	$V_{DD} - 2.1$			V
Output low level voltage	V_{OL}	$I_{OL} = 48\text{ mA}$, for pin type 7			0.4	V
Output low level voltage	V_{OL}	$I_{OL} = 2\text{ mA}$, for pin type 5			0.4	V
Input leak current	I_{IL}	$V_I = V_{SS}, V_{DD}$, for pin types 0, 1, 6, and 7	-10		+10	μA
Pull-up resistance	R_{UP}	For pin types 4 and 5	40	80	160	k Ω

The pin types above refer to the following groups.

Input

(0) $\overline{\text{BCK}}$, $\overline{\text{BICKIN}}$, $\overline{\text{BIDATAI}}$, $\overline{\text{C2PO}}$, $\overline{\text{LOCKIN}}$, $\overline{\text{LRCK}}$, $\overline{\text{PLLOUTIN}}$, $\overline{\text{ROUGH}}$, $\overline{\text{SBSO}}$, $\overline{\text{SCOR}}$, $\overline{\text{SDATA}}$, $\overline{\text{WFCK}}$, $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$

(1) $\overline{\text{SUA0}}$ to $\overline{\text{SUA6}}$, $\overline{\text{TEST0}}$ to $\overline{\text{TEST6}}$, $\overline{\text{X1EN}}$, $\overline{\text{RESET}}$

Output

(2) CLV^+ , CLV^- , FSW

(3) $\overline{\text{DATAACKO}}$, $\overline{\text{EFM}}$, $\overline{\text{EFMG}}$, $\overline{\text{EFMGATE0}}$ to $\overline{\text{EFMGATE6}}$, $\overline{\text{EXCK}}$, $\overline{\text{LOCK}}$, $\overline{\text{MCK}}$, $\overline{\text{MON}}$, $\overline{\text{PSUBSYNC}}$, $\overline{\text{RA0}}$ to $\overline{\text{RA9}}$, $\overline{\text{SUBSYNC}}$, $\overline{\text{CAS0}}$ to $\overline{\text{CAS1}}$, $\overline{\text{RAS0}}$ to $\overline{\text{RAS1}}$, $\overline{\text{ERROR}}$, $\overline{\text{EXTACK}}$, $\overline{\text{FRCK}}$, $\overline{\text{LWE}}$, $\overline{\text{UWE}}$, $\overline{\text{OE}}$

Input/Output

(4) $\overline{\text{D0}}$ to $\overline{\text{D7}}$, $\overline{\text{IO0}}$ to $\overline{\text{IO15}}$

(5) $\overline{\text{INT0}}$ to $\overline{\text{INT1}}$, $\overline{\text{SWAIT}}$

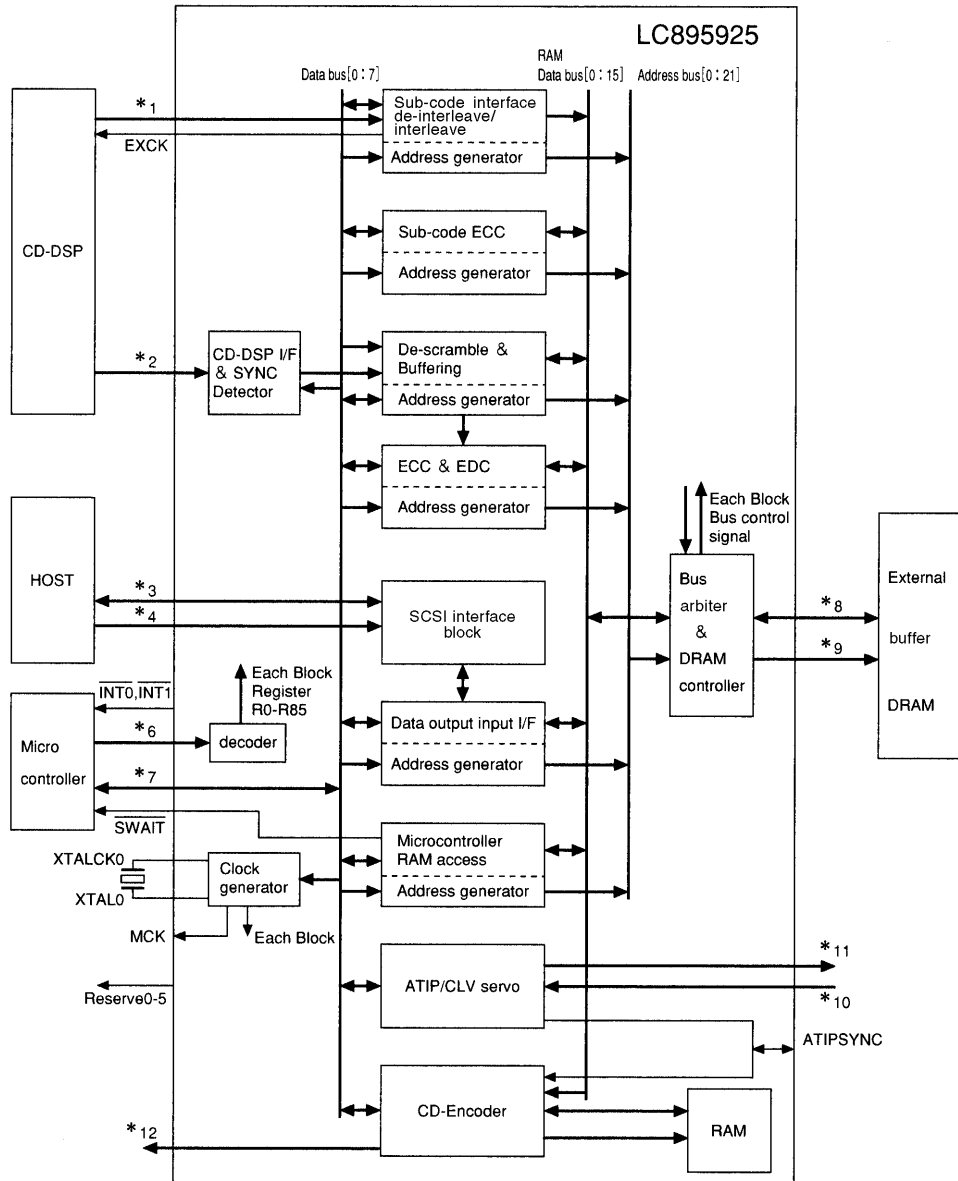
(6) $\overline{\text{ATIPSYNC}}$, $\overline{\text{Reserve0}}$ to $\overline{\text{Reserve5}}$

(7) $\overline{\text{ACK}}$, $\overline{\text{ATN}}$, $\overline{\text{BSY}}$, $\overline{\text{C/D}}$, $\overline{\text{DB0}}$ to $\overline{\text{DB7}}$, $\overline{\text{DBP}}$, $\overline{\text{I/O}}$, $\overline{\text{MSG}}$, $\overline{\text{REQ}}$, $\overline{\text{RST}}$, $\overline{\text{SEL}}$

Note: The $\overline{\text{XTAL0}}$, $\overline{\text{XTAL1}}$, $\overline{\text{XTALCK0}}$, and $\overline{\text{XTALCK1}}$ pins fall outside of these DC characteristic specifications.

LC895925

Block Diagram



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*1 WFCK, SBSO, SCOR

*2 BCK, SDATA, LRCK, C2PO

*3 DB0 to DB7, DBP, BSY, MSG, SEL, RST, REQ, I/O, C/D

*4 ACK, ATN

*6 RD, WR, SUA0 to SUA6, CS

*7 D0 to D7

*8 IO0 to IO15

*9 RA0 to RA9, RAS0, RAS1, CAS0, CAS1, OE, UWE, LWE

*10 PLLOUTIN, ROUGH, LOCKIN, BICLKIN, BIDATAIN

*11 ERROR, LOCK, CLV⁺ (MDP), CLV⁻ (MDS), MON, FSW

*12 SUBSYNC, PSUBSYNC, FRCK, EFM, EFMG, EFMGATE3 to EFMGATE0, EXTACK, DATAACK0

LC895925

Pin Descriptions

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, N: No connection pin

Pin Number	Pin Name	Type	Description
1	V _{SS}	P	
2	Reserve0	B	Reserved for future expansion (leave open)
3	Reserve1	B	Reserved for future expansion (connect to ground)
4	Reserve2	B	Reserved for future expansion (connect to ground)
5	TEST1	I	Test pin (connect to V _{SS})
6	XTALCK0	I	Crystal oscillator circuit input pin (17.2872 to 69.1488 MHz)
7	XTAL0	O	Crystal oscillator circuit output pin
8	TEST2	I	Test pin (connect to V _{SS})
9	MCK	O	Master Clock output pin
10	TEST3	I	Test pin (connect to V _{SS})
11	XTALCK1	I	Crystal oscillator circuit input pin (20 MHz)
12	XTAL1	O	Crystal oscillator circuit output pin
13	TEST4	I	Test pin (connect to V _{SS})
14	V _{DD}	P	
15	V _{SS}	P	
16	CLV+ (MDP)	O	CLV servo signal output pins
17	CLV- (MDS)	O	
18	MON	O	
19	FSW	O	
20	V _{DD}	P	
21	V _{SS}	P	
22	PLLOUTIN	I	Wobble signal carrier clock input pin
23	ROUGH	I	Rough CLV servo wobble signal input pin
24	LOCKIN	I	CD decoder lock signal input pin
25	LOCK	O	CLV servo lock monitor pin
26	ERROR	O	ATIP parity error detection pin
27	ATIPSYNC	B	ATIP synchronization signal I/O pin
28	BIDATAI	I	Biphase data input pin
29	BICLKIN	I	Biphase data transfer clock input pin
30	V _{DD}	P	
31	IO0	B	Data signal pins for ROM encoder/decoder buffer RAM, with pull-up resistors
32	IO1	B	
33	IO2	B	
34	IO3	B	
35	IO4	B	
36	IO5	B	
37	IO6	B	
38	IO7	B	
39	IO8	B	
40	V _{DD}	P	
41	V _{SS}	P	

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LC895925

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, N: No connection pin

Pin Number	Pin Name	Type	Description
42	IO9	B	Data signal pins for ROM encoder/decoder DRAM, with pull-up resistors
43	IO10	B	
44	IO11	B	
45	IO12	B	
46	IO13	B	
47	IO14	B	
48	IO15	B	
49	V _{SS}	P	
50	RA0	O	Address signal pins for ROM encoder/decoder DRAM
51	RA1	O	
52	RA2	O	
53	RA3	O	
54	RA4	O	
55	RA5	O	
56	RA6	O	
57	RA7	O	
58	RA8	O	
59	RA9	O	
60	V _{DD}	P	
61	V _{SS}	P	
62	$\overline{\text{RAS0}}$	O	DRAM $\overline{\text{RAS}}$ signal output pins
63	$\overline{\text{RAS1}}$	O	
64	$\overline{\text{CAS0}}$	O	DRAM $\overline{\text{CAS}}$ signal output pins
65	$\overline{\text{CAS1}}$	O	
66	$\overline{\text{OE}}$	O	DRAM Output Enable signal output pin
67	$\overline{\text{UWE}}$	O	DRAM Output Upper Write Enable signal output pin
68	$\overline{\text{LWE}}$	O	DRAM Output Lower Write Enable signal output pin
69	TEST0	I	Test pin (connect to V _{SS})
70	V _{DD}	P	
71	EXCK	O	Subcode data read shift clock output pin
72	WFCK	I	Subcode frame synchronization input pin
73	SBSO	I	Subcode serial data input pin
74	SCOR	I	Subcode block synchronization input pin
75	V _{SS}	P	
76	BCK	I	Serial data input clock input pin
77	SDATA	I	Serial data input pin
78	LRCK	I	44.1-kHz strobe signal input pin
79	C2PO	I	C2 pointer input pin
80	V _{DD}	P	
81	V _{SS}	P	
82	$\overline{\text{DB0}}$	B	SCSI pins
83	$\overline{\text{DB1}}$	B	
84	V _{DD}	P	
85	$\overline{\text{DB2}}$	B	SCSI pins
86	$\overline{\text{DB3}}$	B	
87	V _{SS}	P	
88	$\overline{\text{DB4}}$	B	SCSI pins
89	$\overline{\text{DB5}}$	B	

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LC895925

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, N: No connection pin

Pin Number	Pin Name	Type	Description
90	V _{DD}	P	
91	DB6	B	SCSI pins
92	V _{DD}	P	
93	V _{SS}	P	
94	DB7	B	SCSI pins
95	DBP	B	
96	V _{DD}	P	
97	V _{SS}	P	
98	ATN	B	SCSI pins
99	BSY	B	
100	V _{DD}	P	
101	V _{SS}	P	
102	ACK	B	SCSI pins
103	RST	B	
104	V _{DD}	P	
105	V _{SS}	P	
106	MSG	B	SCSI pins
107	SEL	B	
108	V _{DD}	P	
109	C/D	B	SCSI pins
110	V _{DD}	P	
111	REQ	B	SCSI pins
112	I/O	B	
113	V _{SS}	P	
114	X1EN	I	Pin for selecting SCSI interface clock (XTALCK0 or XTALCK1)
115	RESET	I	RESET pin
116	V _{DD}	P	
117	DATAACKO	O	4.3218-MHz (Normal Speed) oscillator output pin
118	PSUBSYNC	O	Pseudo subcode synchronization output pin
119	EXTACK	O	ATIP synchronization interval acknowledgment output pin
120	V _{DD}	P	
121	V _{SS}	P	
122	SUBSYNC	O	Subcode synchronization signal output pin
123	FRCK	O	EFM frame synchronization signal output pin
124	FRCK	O	EFM output gate signal output pin
125	EFM	O	EFM signal output pin
126	EFMGATE0	O	EFM pulse width detection gate signals
127	EFMGATE1	O	
128	EFMGATE2	O	
129	EFMGATE3	O	
130	TEST5	I	Test pin (connect to V _{SS})
131	V _{SS}	P	
132	TEST6	I	Test pin (connect to V _{SS})

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LC895925

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, N: No connection pin

Pin Number	Pin Name	Type	Description
133	SUA0	I	Command register selection address input pinsI
134	SUA1	I	
135	SUA2	I	
136	SUA3	I	
137	SUA4	I	
138	SUA5	I	
139	SUA6	I	
140	V _{DD}	P	
141	V _{SS}	P	
142	D0	B	Microcontroller data signal pins, with pull-up resistors
143	D1	B	
144	D2	B	
145	D3	B	
146	D4	B	
147	D5	B	
148	D6	B	
149	D7	B	
150	V _{DD}	P	
151	CS	I	Chip select signal from microcontroller
152	RD	I	Data read signal from microcontroller
153	WR	I	Data write signal from microcontroller
154	SWAIT	O	Wait signal to microcontroller
155	INT0	O	Interrupt request signals to microcontroller. Open drain outputs with built-in pull-up resistors
156	INT1	O	
157	Reserve3	B	Reserved for future expansion (leave open)
158	Reserve4	B	
159	Reserve5	B	
160	V _{DD}	P	

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