

SANYO

CD-R Encoder/Decoder IC with Built-in SCSI Interface

Overview

The LC895926 is a CD-R IC that provides a wide range of functions including CD-ROM decoding (including ECC) and encoding, subcode encoding and decoding, CD encoding, ATIP decoding and CLV servo, and a SCSI interface that includes the register block.

Features

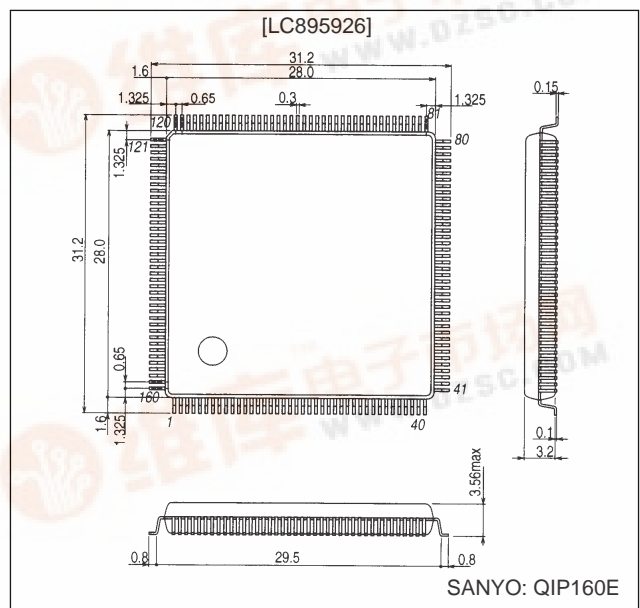
- ECC and EDC correction/addition for CD-ROM data (during decoding and encoding)
- Subcode decoding/encoding complete with error detection and error correction
- ATIP decoding and CRC checking for both encoding and decoding
- CLV servo control using ATIP data during encoding
- CIRC code insertion and EFM modulation during encoding
- Access to buffer RAM from microcontroller via LC895926
- Built-in SCSI interface
- Speeds of 24× for decoding and 12× for encoding
- Transfers speeds of 10 megabytes/s (synchronous) and 5 megabytes/s (asynchronous) with 16-bit 50-ns EDO-DRAMs
- Buffer RAM sizes between 1 and 32 megabits (using 16-bit EDO-DRAMs)
- User control over sizes of CD main channel, C2 flag, and subcode areas in buffer RAM
- Built-in batch transfer function for transferring entire CD main channel, C2 flag, or subcode area in a single operation.

- Built-in multiblock transfer function for transferring multiple blocks in a single operation.
- Automatic sequencing of encoding and decoding processing for a reduced processing load on the system microcontroller.

Package Dimensions

unit: mm

3153A-QFP160E



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Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-------------------------------|---------------------|-----------------------------|----------------------|------------------|
| Maximum power supply voltage | $V_{DD\text{ max}}$ | | -0.3 to +7.0 | V |
| I/O voltage | V_I, V_O | | -0.3 to $V_{DD}+0.3$ | V |
| Allowable power dissipation | $P_d\text{ max}$ | $T_a \leq 70^\circ\text{C}$ | 600 | mW |
| Operating temperature | T_{opr} | | -30 to +70 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -55 to +125 | $^\circ\text{C}$ |
| Solder resistance (Pins only) | | 10 seconds | 260 | $^\circ\text{C}$ |

Allowable Operating Ranges at $T_a = -30$ to $+70^\circ\text{C}$, $V_{SS} = 0\text{ V}$

| Parameter | Symbol | 3.3V | | | 5V | | | Unit |
|----------------------|----------|------|-----|----------|-----|-----|----------|------|
| | | min | typ | max | min | typ | max | |
| Power supply voltage | V_{DD} | 3.0 | 3.3 | 3.6 | 4.5 | 5.0 | 5.5 | V |
| Input voltage range | V_{IN} | 0 | | V_{DD} | 0 | | V_{DD} | V |

DC Characteristics at $T_a = -30$ to $+70^\circ\text{C}$, $V_{SS} = 0\text{ V}$, $V_{DD} = 4.5$ to 5.5 V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---------------------------|----------|--|----------------|-----|-----|---------------|
| | | | min | typ | max | |
| Input high level voltage | V_{IH} | TTL levels, for pins (1) and (6) | 2.2 | | | V |
| Input low level voltage | V_{IL} | | | | 0.8 | V |
| Input high level voltage | V_{IH} | TTL levels, for pin (4), with pull-up resistors | 2.2 | | | V |
| Input low level voltage | V_{IL} | | | | 0.8 | V |
| Input high level voltage | V_{IH} | TTL levels, for pins (0) and (7), with Schmitt inputs | 2.5 | | | V |
| Input low level voltage | V_{IL} | | | | 0.6 | V |
| Output high level voltage | V_{OH} | $I_{OH} = -2\text{ mA}$, for pin (3) | $V_{DD} - 2.1$ | | | V |
| Output low level voltage | V_{OL} | $I_{OL} = 2\text{ mA}$, for pin (3) | | | 0.4 | V |
| Output high level voltage | V_{OH} | $I_{OH} = -2\text{ mA}$, for pins (2), (4), and (6) | $V_{DD} - 2.1$ | | | V |
| Output low level voltage | V_{OL} | $I_{OL} = 2\text{ mA}$, for pins (2), (4), and (6) | | | 0.4 | V |
| Output high level voltage | V_{OH} | $I_{OH} = -48\text{ mA}$, for pin (7) | $V_{DD} - 2.1$ | | | V |
| Output low level voltage | V_{OL} | $I_{OL} = 48\text{ mA}$, for pin (7) | | | 0.4 | V |
| Output low level voltage | V_{OL} | $I_{OL} = 2\text{ mA}$, for pin (5) | | | 0.4 | V |
| Input leak current | I_{IL} | $V_I = V_{SS}, V_{DD}$, for pins (0), (1), (6), and (7) | -10 | | +10 | μA |
| Pull-up resistance | R_{UP} | For pins (4) and (5) | 40 | 80 | 160 | k Ω |

The pins above refer to the following groups.

Input

(0) $\overline{\text{BCK}}$, $\overline{\text{BICKIN}}$, $\overline{\text{BIDATAI}}$, $\overline{\text{C2PO}}$, $\overline{\text{LOCKIN}}$, $\overline{\text{LRCK}}$, $\overline{\text{PLOWTIN}}$, $\overline{\text{ROUGH}}$, $\overline{\text{SBSO}}$, $\overline{\text{SCOR}}$, $\overline{\text{SDATA}}$, $\overline{\text{WFCK}}$, $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$

(1) $\overline{\text{SUA0}}$ to $\overline{\text{SUA7}}$, $\overline{\text{TEST0}}$ to $\overline{\text{TEST6}}$, $\overline{\text{RESET}}$

Output

(2) $\overline{\text{CLV}^+}$, $\overline{\text{CLV}^-}$, $\overline{\text{FSW}}$

(3) $\overline{\text{EFM}}$, $\overline{\text{EFMG}}$, $\overline{\text{EFMGATE0}}$ to $\overline{\text{EFMGATE3}}$, $\overline{\text{EXCK}}$, $\overline{\text{LOCK}}$, $\overline{\text{MON}}$, $\overline{\text{RA0}}$ to $\overline{\text{RA9}}$, $\overline{\text{SUBSYNC}}$, $\overline{\text{CAS0}}$ to $\overline{\text{CAS1}}$, $\overline{\text{RAS0}}$ to $\overline{\text{RAS1}}$, $\overline{\text{LWE}}$, $\overline{\text{UWE}}$, $\overline{\text{OE}}$

Input

(4) $\overline{\text{D0}}$ to $\overline{\text{D7}}$, $\overline{\text{IO0}}$ to $\overline{\text{IO15}}$

(5) $\overline{\text{INT0}}$ to $\overline{\text{INT1}}$, $\overline{\text{SWAIT}}$

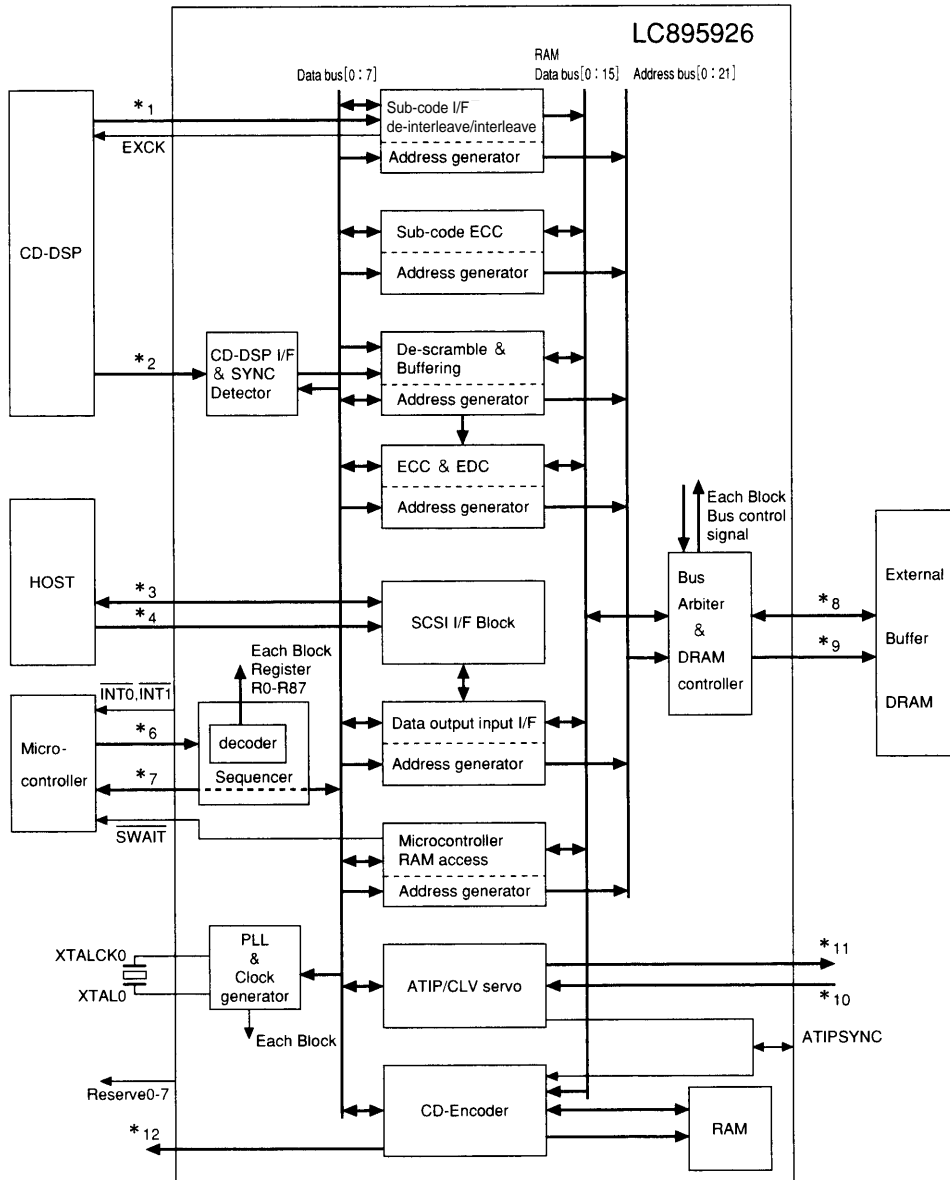
(6) $\overline{\text{ATIPSYNC}}$, $\overline{\text{Reserve0}}$ to $\overline{\text{Reserve7}}$

(7) $\overline{\text{ACK}}$, $\overline{\text{ATN}}$, $\overline{\text{BSY}}$, $\overline{\text{C/D}}$, $\overline{\text{DB0}}$ to $\overline{\text{DB7}}$, $\overline{\text{DBP}}$, $\overline{\text{I/O}}$, $\overline{\text{MSG}}$, $\overline{\text{REQ}}$, $\overline{\text{RST}}$, $\overline{\text{SEL}}$

Note: The $\overline{\text{XTAL0}}$, $\overline{\text{XTAL1}}$, $\overline{\text{XTALCK0}}$, and $\overline{\text{XTALCK1}}$ pins are not included in these DC characteristic specifications.

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Block Diagram



A10142

- *1 WFCK, SBSO, SCOR
- *2 BCK, SDATA, LRCK, C2PO
- *3 DB0 to DB7, DBP, BSY, MSG, SEL, RST, REQ, I/O, C/D
- *4 ACK, ATN
- *6 RD, WR, SUA0 to SUA7, CS
- *7 D0 to D7
- *8 IO0 to IO15
- *9 RA0 to RA9, RAS0, RAS1, CAS0, CAS1, OE, UWE, LWE
- *10 PLLOUTIN, ROUGH, LOCKIN, BICLKIN, BIDATAIN
- *11 LOCK, CLV⁺ (MDP), CLV⁻ (MDS), MON, FSW
- *12 SUBSYNC, EFM, EFMG, EFMGATE0 to EFMGATE3

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Pin Descriptions

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, N: No connection pin

| Pin Number | Pin Name | Type | Description |
|------------|------------------------|------|---|
| 1 | V _{SS} | P | |
| 2 | XTALCK0 | I | Xtal oscillator circuit input pin (17.2872 MHz) |
| 3 | XTAL0 | O | Xtal oscillator circuit output pin |
| 4 | TEST0 | I | Test pin (connect to V _{SS}) |
| 5 | RESET | I | Reset pin |
| 6 | V _{DD} | P | 5V |
| 7 | SUBSYNC | O | Subcode synchronization signal output pin |
| 8 | EFMG | O | EFM output gate signal output pin |
| 9 | EFM | O | EFM signal output pin |
| 10 | EFMGATE0 | O | EFM pulse width detection gate signals |
| 11 | EFMGATE1 | O | |
| 12 | EFMGATE2 | O | |
| 13 | EFMGATE3 | O | |
| 14 | TEST1 | I | Test pin (connect to V _{SS}) |
| 15 | Reserve0 | B | Reserved for future expansion (connect to V _{SS} if unused.) |
| 16 | Reserve1 | B | |
| 17 | Reserve2 | B | |
| 18 | Reserve3 | B | |
| 19 | Reserve4 | B | |
| 20 | V _{DD} | P | 3.3V |
| 21 | V _{SS} | P | |
| 22 | Reserve5 | B | Reserved for future expansion (connect to V _{SS} if unused.) |
| 23 | Reserve6 | B | |
| 24 | Reserve7 | B | |
| 25 | TEST2 | I | Test pin (connect to V _{SS}) |
| 26 | LOCKIN | I | CD decoder lock signal input pin |
| 27 | LOCK | O | CLV servo lock monitor pin |
| 28 | PLL0UTIN | I | Wobble signal carrier clock input pin |
| 29 | V _{SS} | P | |
| 30 | ROUGH | I | Rough CLV servo wobble signal input pin |
| 31 | ATIPSYNC | B | ATIP synchronization signal I/O pin |
| 32 | BICKIN | I | Biphase data transfer clock input pin |
| 33 | BIDATAI | I | Biphase data input pin |
| 34 | V _{DD} | P | 3.3V |
| 35 | V _{SS} | P | |
| 36 | CLV ⁺ (MDP) | O | CLV servo signal output pin |
| 37 | CLV ⁻ (MDS) | O | |
| 38 | MON | O | |
| 39 | FSW | O | |
| 40 | V _{DD} | P | 5V |
| 41 | V _{SS} | P | |

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, N: No connection pin

| Pin Number | Pin Name | Type | Description |
|------------|--------------------------|------|---|
| 42 | IO0 | B | Data signal pins for ROM encoder/decoder DRAM, with pull-up resistors |
| 43 | IO1 | B | |
| 44 | IO2 | B | |
| 45 | IO3 | B | |
| 46 | IO4 | B | |
| 47 | IO5 | B | |
| 48 | V _{DD} | P | 5V |
| 49 | IO6 | B | Data signal pins for ROM encoder/decoder DRAM, with pull-up resistors |
| 50 | IO7 | B | |
| 51 | IO8 | B | |
| 52 | IO9 | B | |
| 53 | V _{SS} | P | |
| 54 | IO10 | B | Data signal pins for ROM encoder/decoder DRAM, with pull-up resistors |
| 55 | IO11 | B | |
| 56 | IO12 | B | |
| 57 | IO13 | B | |
| 58 | IO14 | B | |
| 59 | IO15 | B | |
| 60 | V _{DD} | P | 3.3V |
| 61 | V _{SS} | P | |
| 62 | RA0 | O | Address signal pins for ROM encoder/decoder DRAM |
| 63 | RA1 | O | |
| 64 | RA2 | O | |
| 65 | RA3 | O | |
| 66 | RA4 | O | |
| 67 | RA5 | O | |
| 68 | RA6 | O | |
| 69 | V _{SS} | P | |
| 70 | RA7 | O | Address signal pins for ROM encoder/decoder DRAM |
| 71 | RA8 | O | |
| 72 | RA9 | O | |
| 73 | $\overline{\text{RAS0}}$ | O | $\overline{\text{RAS}}$ signal pins for ROM encoder/decoder DRAM |
| 74 | $\overline{\text{RAS1}}$ | O | |
| 75 | $\overline{\text{CAS0}}$ | O | $\overline{\text{CAS}}$ signal pins for ROM encoder/decoder DRAM |
| 76 | $\overline{\text{CAS1}}$ | O | |
| 77 | $\overline{\text{OE}}$ | O | Output enable signal pin for ROM encoder/decoder DRAM |
| 78 | $\overline{\text{UWE}}$ | O | Upper write enable signal pin for ROM encoder/decoder DRAM |
| 79 | $\overline{\text{LWE}}$ | O | Lower write enable signal pin for ROM encoder/decoder DRAM |
| 80 | V _{DD} | P | 5V |
| 81 | V _{SS} | P | |
| 82 | $\overline{\text{DB0}}$ | B | SCSI pins |
| 83 | $\overline{\text{DB1}}$ | B | |
| 84 | V _{DD} | P | 3.3V |
| 85 | $\overline{\text{DB2}}$ | B | SCSI pins |
| 86 | $\overline{\text{DB3}}$ | B | |
| 87 | V _{SS} | P | |
| 88 | $\overline{\text{DB4}}$ | B | SCSI pins |
| 89 | $\overline{\text{DB5}}$ | B | |

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power Supply pin, N: No connection pin

| Pin Number | Pin Name | Type | Description |
|------------|-----------------|------|---|
| 90 | V _{DD} | P | 3.3V |
| 91 | DB6 | B | SCSI pin |
| 92 | V _{DD} | P | 5V |
| 93 | V _{SS} | P | |
| 94 | DB7 | B | SCSI pins |
| 95 | DBP | B | |
| 96 | V _{DD} | P | 5V |
| 97 | V _{SS} | P | |
| 98 | ATN | B | SCSI pin |
| 99 | BSY | B | SCSI pin |
| 100 | V _{DD} | P | 5V |
| 101 | V _{SS} | P | |
| 102 | ACK | B | SCSI pins |
| 103 | RST | B | |
| 104 | V _{DD} | P | 5V |
| 105 | V _{SS} | P | |
| 106 | MSG | B | SCSI pins |
| 107 | SEL | B | |
| 108 | V _{DD} | P | 3.3V |
| 109 | C/D | B | SCSI pin |
| 110 | V _{DD} | P | 5V |
| 111 | REQ | B | SCSI pins |
| 112 | I/O | B | |
| 113 | V _{SS} | P | |
| 114 | XTALCK1 | I | Xtal oscillator circuit input pin for SCSI interface (20 MHz) |
| 115 | XTAL1 | O | Xtal oscillator circuit output pin for SCSI interface |
| 116 | TEST3 | I | Test pin (connect to V _{SS}) |
| 117 | TEST4 | I | Test pin (connect to V _{SS}) |
| 118 | TEST5 | I | Test pin (connect to V _{SS}) |
| 119 | BCK | I | Serial data input clock input pin |
| 120 | V _{DD} | P | 5V |
| 121 | V _{SS} | P | |
| 122 | SDATA | I | Serial data input pin |
| 123 | LRCK | I | 44.1 kHz strobe signal input pin |
| 124 | C2PO | I | C2 pointer input pin |
| 125 | EXCK | O | Subcode data read shift clock output pin |
| 126 | WFCK | I | Subcode frame synchronization input pin |
| 127 | SBSO | I | Subcode serial data input pin |
| 128 | SCOR | I | Subcode block synchronization input pin |
| 129 | V _{SS} | P | |
| 130 | SUA0 | I | Commande register selection address input pins |
| 131 | SUA1 | I | |
| 132 | SUA2 | I | |
| 133 | SUA3 | I | |
| 134 | SUA4 | I | |
| 135 | SUA5 | I | |
| 136 | SUA6 | I | |
| 137 | SUA7 | I | |

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power Supply pin, N: No connection pin

| Pin Number | Pin Name | Type | Description |
|------------|--------------------|------|--|
| 138 | \overline{WR} | I | Data write signal from microcontroller |
| 139 | \overline{RD} | I | Data read signal from microcontroller |
| 140 | V _{DD} | P | 3.3V |
| 141 | V _{SS} | P | |
| 142 | \overline{CS} | I | Chip select signal from microcontroller |
| 143 | D0 | B | Microcontroller data signal pins, with pull-up resistors |
| 144 | D1 | B | |
| 145 | D2 | B | |
| 146 | D3 | B | |
| 147 | D4 | B | |
| 148 | D5 | B | |
| 149 | D6 | B | |
| 150 | D7 | B | |
| 151 | \overline{SWAIT} | O | Wait signal to microcontroller |
| 152 | V _{DD} | P | 5V |
| 153 | $\overline{INT0}$ | O | Interrupt request signals to microcontroller. Open drain outputs with built-in pull-up resistors |
| 154 | $\overline{INT1}$ | O | |
| 155 | TEST6 | I | Test pin (connect to V _{SS}) |
| 156 | PD | O | Charge pump output pin |
| 157 | VCNT | I | VCO control voltage pin |
| 158 | R | I | VCO bias resistor pin |
| 159 | V _{SS} | P | |
| 160 | V _{DD} | P | 3.3V |

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