

Ordering number: EN3202A



LC8991

NTSC CCD 1H Delay Line

Overview

The Sanyo LC8991 is a 1H delay line for NTSC television systems.

- Sample-and-hold circuit

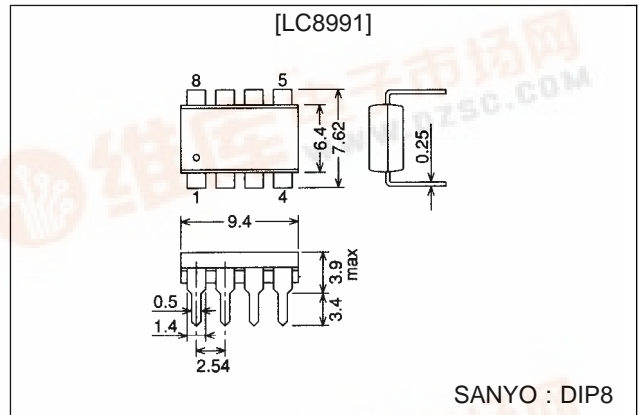
Features

- Single 9 V power supply
- Low clock input voltage
- 1H delay signal can be obtained with low-pass filter and 7.16 MHz clock input
- Minimum number of external components required because timing generator, driver, bias generator and output amplifier are built in
- 8-pin DIP (Small package)

Package Dimensions

unit : mm

3001B-DIP8



Functions

- 453 stages CCD shift register
- CCD drive circuit
- Auto-bias circuit
- Sync tip clamp circuit

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{DD} max		11	V
Allowable power dissipation	P _d max		500	mW
Operating temperature	T _{opr}		-10 to +60	°C
Storage temperature	T _{stg}		-55 to +125	°C

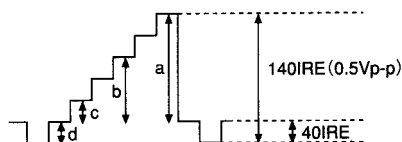


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Electrical Characteristics

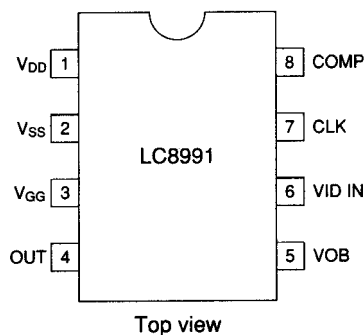
Parameter	Symbol	Conditions	min	typ	max	Unit
DC Characteristics at Ta = 25°C, V _{DD} = 9 V, CLOCK = 7.15909 MHz; 0.3 Vp-p						
Supply voltage	V _{DD}		8.5	9.0	9.5	V
Supply current	I _{DD}			16.5	20.0	mA
DC output voltage	V _{GG}			13.5		V
	OUT			3.1		V
	VOB			4.5		V
	VID IN			2.8		V
	CLK			2.0		V
	COMP			2.7		V
AC Characteristics at Ta = 25°C, V _{DD} = 9 V, CLOCK = 7.15909 MHz ; 0.3 Vp-p						
Maximum input voltage	V _{IN} max			0.5	0.7	Vp-p
Voltage gain	V _G	Input : 15 kHz, 0.5 Vp-p	6	9	11	dB
Linearity	L6	b/a, Note 1	56	60	64	%
	L2	c/a, Note 1	18	20	22	%
	LS	d/a, Note 1	37	40	43	%
Frequency response	G _f	Note 2	-3.0	-2.3		dB
Noise	V _{NO}	3.4 MHz bandwidth		1.1		mVrms
Clock input voltage	Eck		0.1	0.3	1.0	Vp-p
Output impedance	Z _O			520		Ω
Delay time	t _O			63.42		μs

Note 1) Linearity test
Input: 5 step staircase signal



Note 2) Frequency response test
Input = 0.5 Vp-p sine wave (2.4 MHz)/(20 kHz)

Pin Assignment

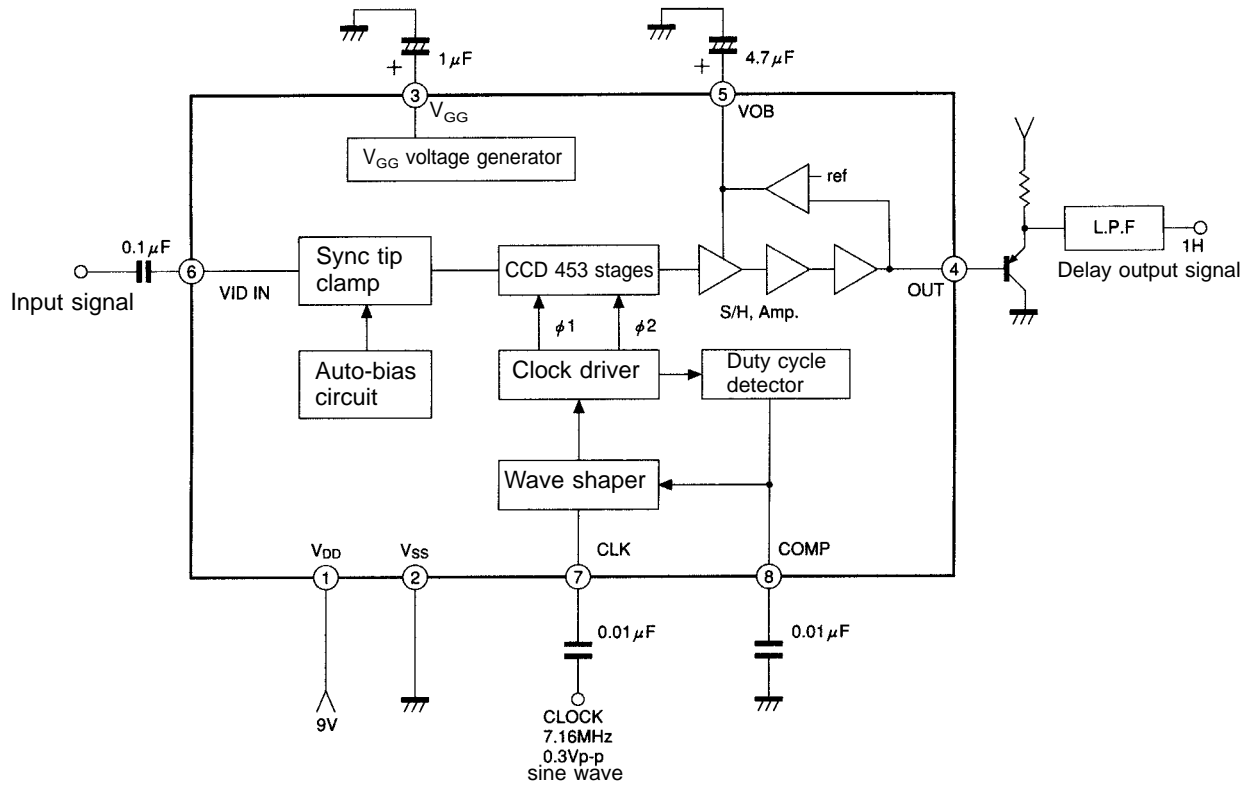


Pin Description

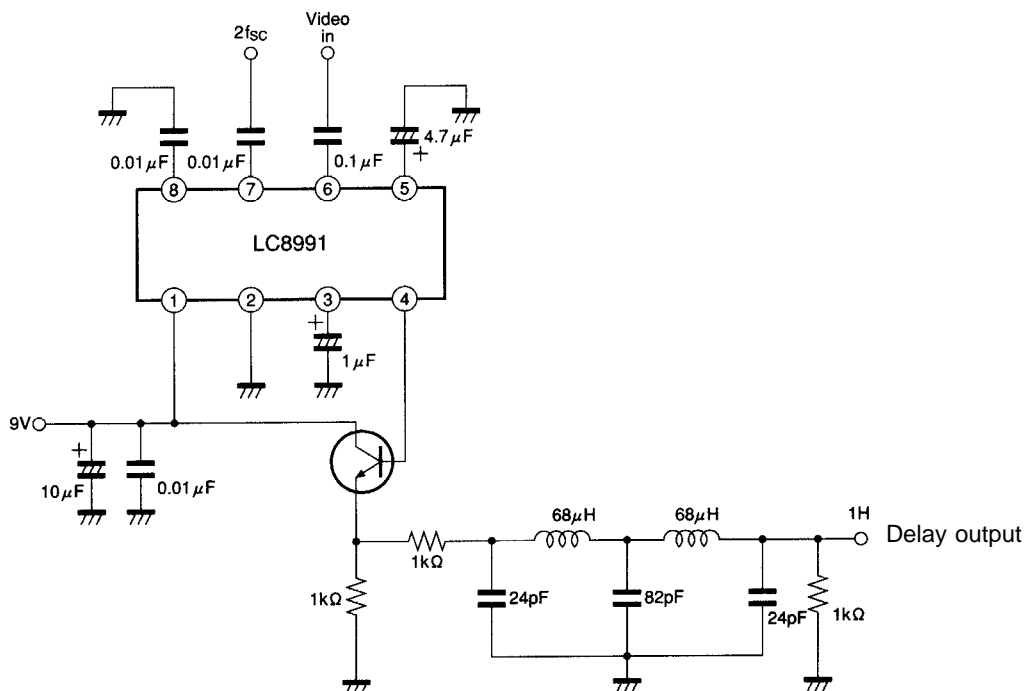
Pin No.	Symbol	Function
1	V _{DD}	Power supply
2	V _{SS}	GND
3	V _{GG}	V _{GG} voltage output
4	OUT	Delay signal output
5	VOB	Feedback output
6	VID IN	Signal input
7	CLK	Clock input
8	COMP	Duty cycle compensation output

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Block Diagram



Sample Application Circuit



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