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#### MOS LSI

LC89977M

CCD Delay Line for PAL



## **Preliminary**

## **Overview**

The LC89977M is CCD delay line for PAL television system that includes a chrominance signal crosstalk exclusion filter and a luminance signal 1-H delay line on WWW.DZSC chip.

WWW.DZSC.CO

## **Features**

- 5-V single-voltage power supply
- Built-in 3 × PLL frequency multiplier circuit allows 3fsc operation from an fsc (4.43 MHz) input.
- Can be switched between the PAL/GBI, and 4.43NTSC formats by setting control pin values.
- Includes a built-in crosstalk exclusion comb filter for the chrominance signal that provides high-precision comb characteristics in an adjustment-free circuit.
- Peripheral circuits provided on chip for operation with a minimum of external components.
- Positive-phase signal input, positive-phase signal output (luminance signal)

# **Functions**

- CCD shift registers (for chrominance and luminance signals)
- · Timig generator and clock driver for CCD
- · Delay time selective circuit
- · CCD signal adder
- Auto-bias circuit
- Sync tip clamp circuit (luminance signal)
- Center bias circuit (chrominance signal)
- · Sample-and-hold circuit
- 3 × PLL frequency multiplier circuit
- · 3fsc clock output circuit
- High voltage generator for CCD Reset Drain (RD)

# **Specifications**

PDF

Absolute Maximum Ratings at  $Ta = 25^{\circ}CD$ 

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V <sub>DD</sub>		-0.3 to +6.0	V
Allowable power dissipation	Pd max		250	mW
Operating temperature	Topr		-10 to +60	°C
Storage temperature	Tstg		-55 to +125	°C

# Package Dimensions

unit: mm 3111-MFP14S





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#### LC89977M

## Allowable Operating Ranges at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions		Linit		
		Conditions	min	typ	max	
Supply voltage	V <sub>DD</sub>		4.75	5.00	5.25	V
Clock input amplitude	V <sub>CLK</sub>		300	500	1000	mVp-p
Clock frequency	F <sub>CLK</sub>	Sine wave		4.43361875		MHz
Chrominance signal input amplitude	V <sub>IN-C</sub>			350	500	mVp-p
Luminance signal input amplitude	V <sub>IN-Y</sub>			400	572	mVp-p

## **Pin Assignment**

		Г						
Chrominance signal input 1	C-IN1	1	$\bigcirc$		14	VSS	Ground	
Power supply	VDD	2			13	C-OUT	Chrominance signa	l output
Chrominance signal input 2	C-IN2	3			12	CONT	Control	
	NC	4	LC89977	М	11	3FSC	3fsc clock output	
Luminance signal input	Y-IN	5			10	CLK	Clock input	
	NC	6			9	VCO	VCO filter output	
Luminance signal output	Y-OUT	7			8	RD	Step-up circuit outp	ut
							Top view	A06298

## **Block Diagram**



#### **Control Pin Functions**

CONT	Mode (representative)	Chrominance signal delay (number of CCD stages)	Luminance signal delay (number of CCD stages)
Low	PAL/GBI	2H (1703.5) + 0H (1)	1H (848)
High	4.43NTSC	1H (845.5) + 0H (1)	1H (842)

#### **Switching Voltage Levels**

Parameter	Symbol	Conditions		Linit		
		Conditions	min	typ	max	
Switching voltage level: low	VL		-0.3	0.0	+0.5	V
Switching voltage level: high	V <sub>H</sub>		2.0	5.0	6.0	V

Note: \*Since the control pins have built-in pull-down resistors (about 70 kΩ), leaving these pins opens effectively sets them to the low level.

#### Function of the 3FSC Pin

This pin provides a 3fsc clock signal generated by the  $3 \times PLL$  frequency multiplier circuit.



## Electrical Characteristics at $V_{DD}$ = 5.0 V, Ta = 25°C, $F_{CLK}$ = 4.43361875 MHz, $V_{CLK}$ = 500 mVp-p

Deremeter	Qumbal			Switc	h states		Ratings			
Parameter	Symbol	SW1	SW2	SW3	Test conditions	min	typ	max	Unit	
Supply current	I <sub>DD-1</sub>	а	а	b	*1	27	32	37	mA	
	I <sub>DD-2</sub>	b	а	b	*1	21				
[Chrominance signal characteristics] (with no input to Y-IN)										
	V <sub>INC-1</sub>	а	а	b	*2	10	2.4	20	V	
DC output voltage	V <sub>INC-2</sub>	b	а	b	*2	1.0		2.5		
	V <sub>OUTC-1</sub>	а	а	b	*2	14	10	2.4	V	
	V <sub>OUTC-2</sub>	b	а	b	*2	1.4	1.0			
Voltage gain	G <sub>VC-1</sub>	а	а	b	*3	2	0	+2	dB	
	G <sub>VC-2</sub>	b	а	b	*3	2				
Comb depth	C <sub>D-1</sub>	а	а	b	*4	_	-40	-35	dB	
	C <sub>D-2</sub>	b	а	b	*4					
Linearity	L <sub>NC-1</sub>	а	а	b	*5	-0.3	0.0	+0.3	dB	
	L <sub>NC-2</sub>	b	а	b	*5	0.0	0.0	10.0		
Clock leakage (3fsc)	L <sub>CK3C-1</sub>	а	а	b	*6	_	10	50	m\/rms	
	L <sub>CK3C-2</sub>	b	а	b	*6		10			
Clock leakage (fsc)	L <sub>CK1C-1</sub>	а	а	b	*6	_	0.5	15	m\/rmc	
	L <sub>CK1C-2</sub>	b	а	b	*6		0.0	1.0		
Noise	N <sub>C-1</sub>	а	а	b	*7	_	0.5	2.0	mVrms	
110136	N <sub>C-2</sub>	b	а	b	*7		0.0	2.0		
	Z <sub>OC-1</sub>	а	а	a, b	*8	200	350	500	0	
	Z <sub>OC-2</sub>	b	а	a, b	*8	200	000			
0-H delay time	T <sub>DC-1</sub>	а	а	b	*9		130		ns	
	T <sub>DC-2</sub>	b	a	b	*9		130		115	

LC89977M

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Deremeter	Quarkal			Switch	n states		Ratings		– Unit
Parameter	Symbol	SW1	SW2	SW3	Test conditions	min	typ	max	
[Luminance signal characteristics] (With no sign	als input to (	C-IN1 a	nd C-IN	2)					
	V <sub>INY-1</sub>	а	а	b	*10	1.2	1 0	2.2	v
DC output voltage	V <sub>INY-2</sub>	b	а	b	*10	1.5	1.0	2.3	
	V <sub>OUTY-1</sub>	а	а	b	*10	0.7	1.2	17	V
	V <sub>OUTY-2</sub>	b	а	b	*10	0.7	1.2	1.7	v
Voltago gain	G <sub>VY-1</sub>	а	а	b	*11	2	0	+2	dB
	G <sub>VY-2</sub>	b	а	b	*11	-2	0		
Eroqueney response	G <sub>FY-1</sub>	а	b	b	*12	2	0	+2	dB
Frequency response	G <sub>FY-2</sub>	b	b	b	*12				
Differential gain	D <sub>GY-1</sub>	а	а	b	*13	0	5	8	0/
Diferential gain	D <sub>GY-2</sub>	b	а	b	*13	0			70
Differential phase	D <sub>PY-1</sub>	а	а	b	*13	0	5	8	deg
	D <sub>PY-2</sub>	b	а	b	*13				
Linearity	L <sub>SY-1</sub>	а	а	b	*14	27	40	43	%
Linearity	L <sub>SY-2</sub>	b	а	b	*14	57			
Clock lookage (3fsc)	L <sub>CK3Y-1</sub>	а	а	b	*15		10	50	mVrms
Clock leakage (Sisc)	L <sub>CK3Y-2</sub>	b	а	b	*15		10		
Clock lookage (fsc)	L <sub>CK1Y-1</sub>	а	а	b	*15		0.5	15	
Clock leakage (ISC)	L <sub>CK1Y-2</sub>	b	а	b	*15		0.5	1.5	111111115
Noico	N <sub>Y-1</sub>	а	а	b	*16		0.5	2.0	m\/rmc
INDISE	N <sub>Y-2</sub>	b	а	b	*16		0.5	2.0	111111115
Output impodance	Z <sub>OY-1</sub>	а	а	c, b	*17	250	400	550	
	Z <sub>OY-2</sub>	а	b	c, b	*17	200			52
Delay time	T <sub>DY-1</sub>	а	а	b	*18		63.81		μs
Delay time	T <sub>DY-2</sub>	b	а	b	*18		63.36		μs

## **Test Conditions**

- 1. The supply current with no input signal
- 2. The pin output voltage (the center bias voltage) with no input signal
- 3. Measure the C-OUT output when a 350-mVp-p sine wave is input to C-IN1 and C-IN2.

$$G_{VC} = 20\log \frac{C-OUT \text{ output } [mVp-p]}{250 \text{ [dB]}}$$
 [dB]

350 [mVp-p]

Test frequencies: G<sub>VC-1</sub>: 4.429662 MHz (PAL/GBI) G<sub>VC-2</sub>: 4.425694 MHz (4.43NTSC)

4. Measure the comb depth from the C-OUT output when a 350-mVp-p sine wave with frequency fa is input to C-IN1 and C-IN2, and when a sine wave of frequency fb is input.

 $C_{D} = 20log \frac{The C-OUT output for an fb input [mVp-p]}{The C-OUT output for an fa input [mVp-p]} [dB]$ Test Frequencies  $fa \qquad fb$   $C_{D-1}: 4.429662 \text{ MHz} \qquad 4.425756 \text{ (PAL/GBI)}$   $G_{D-2}: 4.425694 \text{ MHz} \qquad 4.417819 \text{ (4.43NTSC)}$   $Gain \begin{bmatrix} Gain \\ IdB \end{bmatrix} = \begin{bmatrix} fa & fb \\ fa & fb \\ Frequency [Hz] \\ Frequency [Hz] \end{bmatrix}$ 

5. Measure the C-OUT output when a 200-mVp-p sine wave is input to C-IN1 and C-IN2, and when a 500-mVp-p sine wave is input, and calculate the gain difference as follows:

$$\begin{array}{c} L_{NC} = 20 log & \left( \begin{array}{c} \hline \text{The output for a 500-mVp-p input [mVp-p]} \\ \hline 500 \ [mVp-p] \end{array} \right) \begin{array}{c} \hline \text{The output for a 200-mVp-p input [mVp-p]} \\ \hline 200 \ [mVp-p] \end{array} \right) \begin{array}{c} \hline \text{C} B \end{array} \end{array} \right) \\ \hline \text{Test Frequencies} \\ L_{NC-1} & 4.429662 MHz \ (PAL/GBI) \\ L_{NC-2} & 4.425694 MHz \ (4.43 NTSC) \end{array} \right) \\ \end{array}$$

- 6. Measure the 3fsc (13.3 MHz) and fsc (4.43 MHz) components in the C-OUT output with no input signal.
- 7. Measure the noise in the C-OUT output with no input signal.
- Measure the noise with a noise meter with a 200-kHz high-pass filter and a 5-MHz low-pass filter.
- 8. Input a 350-mVp-p sine wave to C-IN1 and C-IN2. Let V1 be the C-OUT output when SW3 is set to the 'a' position, and let V2 be the C-OUT output when SW3 is set to the 'b' position.

$$Z_{OC} = \frac{V2 [mVp-p] - V1 [mVp-p]}{V1 [mVp-p]} \times 500 [dB]$$

Test Frequencies

Z<sub>OC-1</sub>: 4.429662 MHz (PAL/GBI) Z<sub>OC-2</sub>: 4.425694 MHz (4.43NTSC)

- 9. The delay time in the C-OUT output with respect to the C-IN1 input. This is the CCD 1-bit delay.
- 10. The pin output voltage (clamp voltage) with no input signal.
- 11. Measure the Y-OUT output with a 200-kHz 400-mVp-p sine wave input to Y-IN.

$$G_{VY} = 20\log \frac{Y - OUT \text{ output } [mVp-p]}{400 \ [mVp-p]} \ [dB]$$

12. Measure the Y-OUT output when a 200-kHz 200-mVp-p sine wave is input to Y-IN, and when a 3.3-MHz 200-mVp-p sine wave is input.

$$G_{FY} = 20\log \frac{\text{The Y-OUT output for a 3.3-MHz input [mVp-p]}}{\text{The Y-OUT output for a 200-kHz input [mVp-p]}} [dB]$$

Here, adjust Vbias so that the clamp level is +250 mV.

13. Apply a 5-step staircase wave (as in the figure below) to Y-IN, and measure the differential gain and differential phase in the Y-OUT output using a vector scope.



14. Apply a 5-step staircase wave (as in the figure below) to Y-IN, and measure the luminance level (Y) and the sync level (S) in the Y-OUT output.



- 15. Measure the 3fsc (13.3 MHz) and fsc (4.43 MHz) components in the Y-OUT output with no input signal.
- 16. Measure the noise in the Y-OUT output with no input signal. Measure the noise with a noise meter with a 200-kHz low-pass filter, a 5-MHz low-pass filter, and a 4.43-MHz trap filter.
- 17. Input a 200-kHz, 400-mVp-p sine wave to Y-IN1. Let V1 be the V-OUT output when SW3 is set to the 'c' position, and let V2 be the Y-OUT output when SW3 is set to the 'b' position.

 $Z_{\rm OY} = \ \frac{V2 \ [mVp-p] - V1 \ [mVp-p]}{V1 \ [mVp-p]} \times 500 \ [\Omega]$ 

18. Measure the delay time in the Y-OUT output with respect to the input to Y-IN.

#### **Test Circuit**



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