Ordering number : EN5545

MOS LSI

LC89977M

CCD Delay Line for PAL

Preliminary

Overview

The LC89977M is CCD delay line for PAL television system that includes a chrominance signal crosstalk exclusion filter and a luminance signal 1-H delay line on chip.

Features

- 5-V single-voltage power supply
- Built-in 3 × PLL frequency multiplier circuit allows 3fsc operation from an fsc (4.43 MHz) input.
- Can be switched between the PAL/GBI, and 4.43NTSC formats by setting control pin values.
- Includes a built-in crosstalk exclusion comb filter for the chrominance signal that provides high-precision comb characteristics in an adjustment-free circuit.
- Peripheral circuits provided on chip for operation with a minimum of external components.
- Positive-phase signal input, positive-phase signal output (luminance signal)

Functions

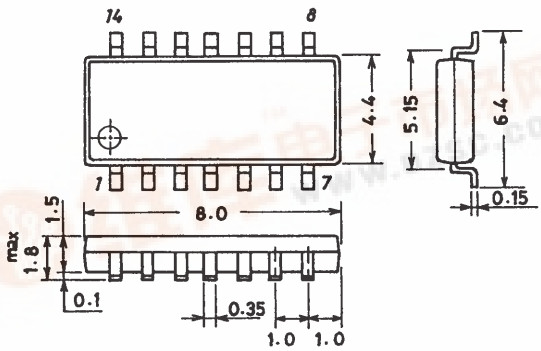
- CCD shift registers (for chrominance and luminance signals)
- Timig generator and clock driver for CCD
- Delay time selective circuit
- CCD signal adder
- Auto-bias circuit
- Sync tip clamp circuit (luminance signal)
- Center bias circuit (chrominance signal)
- Sample-and-hold circuit
- 3 × PLL frequency multiplier circuit
- 3fsc clock output circuit
- High voltage generator for CCD Reset Drain (RD)

Package Dimensions

unit: mm

3111-MFP14S

[LC89977M]



SANYO: MFP14S

Specifications

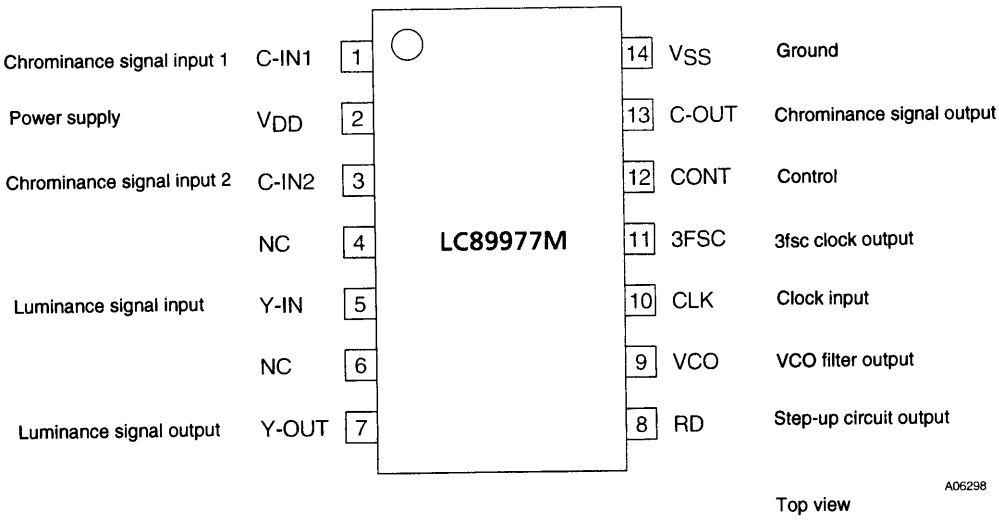
Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +6.0	V
Allowable power dissipation	Pd max		250	mW
Operating temperature	Topr		–10 to +60	°C
Storage temperature	Tstg		–55 to +125	°C

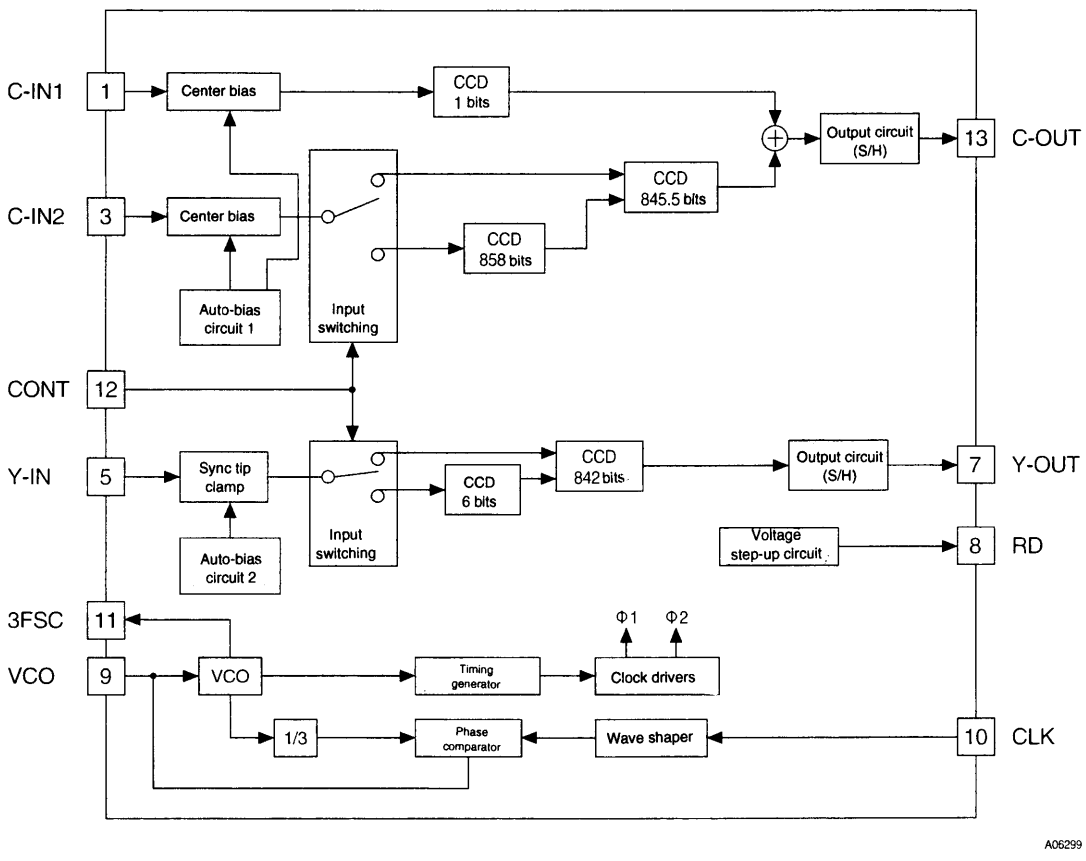
Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.75	5.00	5.25	V
Clock input amplitude	V_{CLK}		300	500	1000	mVp-p
Clock frequency	F_{CLK}	Sine wave		4.43361875		MHz
Chrominance signal input amplitude	V_{IN-C}			350	500	mVp-p
Luminance signal input amplitude	V_{IN-Y}			400	572	mVp-p

Pin Assignment



Block Diagram



Control Pin Functions

CONT	Mode (representative)	Chrominance signal delay (number of CCD stages)	Luminance signal delay (number of CCD stages)
Low	PAL/GBI	2H (1703.5) + 0H (1)	1H (848)
High	4.43NTSC	1H (845.5) + 0H (1)	1H (842)

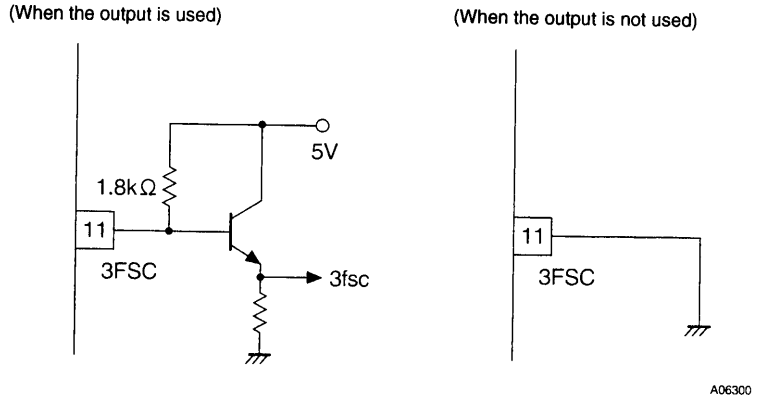
Switching Voltage Levels

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Switching voltage level: low	V_L		–0.3	0.0	+0.5	V
Switching voltage level: high	V_H		2.0	5.0	6.0	V

Note: *Since the control pins have built-in pull-down resistors (about 70 kΩ), leaving these pins opens effectively sets them to the low level.

Function of the 3FSC Pin

This pin provides a 3fsc clock signal generated by the 3 × PLL frequency multiplier circuit.



Electrical Characteristics at V_{DD} = 5.0 V, Ta = 25°C, F_{CLK} = 4.43361875 MHz, V_{CLK} = 500 mVp-p

Parameter	Symbol	Switch states				Ratings			Unit
		SW1	SW2	SW3	Test conditions	min	typ	max	
Supply current	I_{DD-1}	a	a	b	*1	27	32	37	mA
	I_{DD-2}	b	a	b	*1				
[Chrominance signal characteristics] (with no input to Y-IN)									
DC output voltage	V_{INC-1}	a	a	b	*2	1.9	2.4	2.9	V
	V_{INC-2}	b	a	b	*2				
	V_{OUTC-1}	a	a	b	*2	1.4	1.9	2.4	V
	V_{OUTC-2}	b	a	b	*2				
Voltage gain	G_{VC-1}	a	a	b	*3	–2	0	+2	dB
	G_{VC-2}	b	a	b	*3				
Comb depth	C_{D-1}	a	a	b	*4		–40	–35	dB
	C_{D-2}	b	a	b	*4				
Linearity	L_{NC-1}	a	a	b	*5	–0.3	0.0	+0.3	dB
	L_{NC-2}	b	a	b	*5				
Clock leakage (3fsc)	L_{CK3C-1}	a	a	b	*6		10	50	mVrms
	L_{CK3C-2}	b	a	b	*6				
Clock leakage (fsc)	L_{CK1C-1}	a	a	b	*6		0.5	1.5	mVrms
	L_{CK1C-2}	b	a	b	*6				
Noise	N_{C-1}	a	a	b	*7		0.5	2.0	mVrms
	N_{C-2}	b	a	b	*7				
Output impedance	Z_{OC-1}	a	a	a, b	*8	200	350	500	Ω
	Z_{OC-2}	b	a	a, b	*8				
0-H delay time	T_{DC-1}	a	a	b	*9		130		ns
	T_{DC-2}	b	a	b	*9				

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Switch states				Ratings			Unit
		SW1	SW2	SW3	Test conditions	min	typ	max	
[Luminance signal characteristics] (With no signals input to C-IN1 and C-IN2)									
DC output voltage	V_{INY-1}	a	a	b	*10	1.3	1.8	2.3	V
	V_{INY-2}	b	a	b	*10				
	V_{OUTY-1}	a	a	b	*10	0.7	1.2	1.7	V
	V_{OUTY-2}	b	a	b	*10				
Voltage gain	G_{VY-1}	a	a	b	*11	–2	0	+2	dB
	G_{VY-2}	b	a	b	*11				
Frequency response	G_{FY-1}	a	b	b	*12	–2	0	+2	dB
	G_{FY-2}	b	b	b	*12				
Differential gain	D_{GY-1}	a	a	b	*13	0	5	8	%
	D_{GY-2}	b	a	b	*13				
Differential phase	D_{PY-1}	a	a	b	*13	0	5	8	deg
	D_{PY-2}	b	a	b	*13				
Linearity	L_{SY-1}	a	a	b	*14	37	40	43	%
	L_{SY-2}	b	a	b	*14				
Clock leakage (3fsc)	L_{CK3Y-1}	a	a	b	*15		10	50	mVrms
	L_{CK3Y-2}	b	a	b	*15				
Clock leakage (fsc)	L_{CK1Y-1}	a	a	b	*15		0.5	1.5	mVrms
	L_{CK1Y-2}	b	a	b	*15				
Noise	N_{Y-1}	a	a	b	*16		0.5	2.0	mVrms
	N_{Y-2}	b	a	b	*16				
Output impedance	Z_{OY-1}	a	a	c, b	*17	250	400	550	Ω
	Z_{OY-2}	a	b	c, b	*17				
Delay time	T_{DY-1}	a	a	b	*18		63.81		µs
	T_{DY-2}	b	a	b	*18		63.36		µs

Test Conditions

1. The supply current with no input signal
2. The pin output voltage (the center bias voltage) with no input signal
3. Measure the C-OUT output when a 350-mVp-p sine wave is input to C-IN1 and C-IN2.

$$G_{VC} = 20\log \frac{\text{C-OUT output [mVp-p]}}{350\ \text{[mVp-p]}}\ \text{[dB]}$$

Test frequencies:

G_{VC-1}: 4.429662 MHz (PAL/GBI)

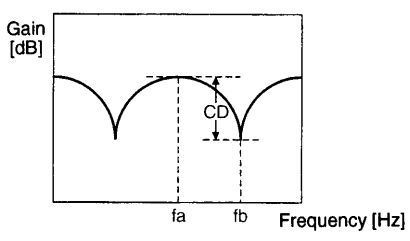
G_{VC-2}: 4.425694 MHz (4.43NTSC)

4. Measure the comb depth from the C-OUT output when a 350-mVp-p sine wave with frequency fa is input to C-IN1 and C-IN2, and when a sine wave of frequency fb is input.

$$C_D = 20\log \frac{\text{The C-OUT output for an fb input [mVp-p]}}{\text{The C-OUT output for an fa input [mVp-p]}}\ \text{[dB]}$$

Test Frequencies

fa	fb
C_{D-1}: 4.429662 MHz	4.425756 (PAL/GBI)
G_{D-2}: 4.425694 MHz	4.417819 (4.43NTSC)



5. Measure the C-OUT output when a 200-mVp-p sine wave is input to C-IN1 and C-IN2, and when a 500-mVp-p sine wave is input, and calculate the gain difference as follows:

$$L_{NC} = 20\log \left(\frac{\text{The output for a 500-mVp-p input [mVp-p]}}{500\ \text{[mVp-p]}} \Big/ \frac{\text{The output for a 200-mVp-p input [mVp-p]}}{200\ \text{[mVp-p]}} \right) \text{[dB]}$$

Test Frequencies

L_{NC-1} 4.429662MHz (PAL/GBI)

L_{NC-2} 4.425694MHz (4.43NTSC)

6. Measure the 3fsc (13.3 MHz) and fsc (4.43 MHz) components in the C-OUT output with no input signal.
7. Measure the noise in the C-OUT output with no input signal.
   Measure the noise with a noise meter with a 200-kHz high-pass filter and a 5-MHz low-pass filter.
8. Input a 350-mVp-p sine wave to C-IN1 and C-IN2. Let V1 be the C-OUT output when SW3 is set to the ‘a’ position, and let V2 be the C-OUT output when SW3 is set to the 'b' position.

$$Z_{OC} = \frac{\text{V2 [mVp-p]} - \text{V1 [mVp-p]}}{\text{V1 [mVp-p]}} \times 500\ \text{[dB]}$$

Test Frequencies

Z_{OC-1}: 4.429662 MHz (PAL/GBI)

Z_{OC-2}: 4.425694 MHz (4.43NTSC)

9. The delay time in the C-OUT output with respect to the C-IN1 input. This is the CCD 1-bit delay.
10. The pin output voltage (clamp voltage) with no input signal.
11. Measure the Y-OUT output with a 200-kHz 400-mVp-p sine wave input to Y-IN.

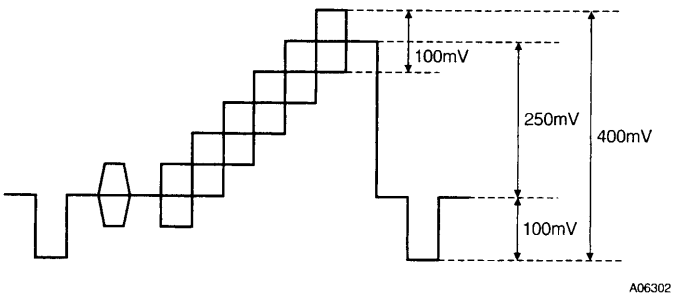
$$G_{VY} = 20\log \frac{\text{Y-OUT output [mVp-p]}}{400\ \text{[mVp-p]}} \text{[dB]}$$

12. Measure the Y-OUT output when a 200-kHz 200-mVp-p sine wave is input to Y-IN, and when a 3.3-MHz 200-mVp-p sine wave is input.

$$G_{FY} = 20\log \frac{\text{The Y-OUT output for a 3.3-MHz input [mVp-p]}}{\text{The Y-OUT output for a 200-kHz input [mVp-p]}} \text{[dB]}$$

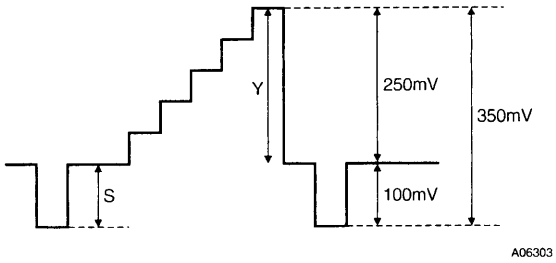
Here, adjust Vbias so that the clamp level is +250 mV.

13. Apply a 5-step staircase wave (as in the figure below) to Y-IN, and measure the differential gain and differential phase in the Y-OUT output using a vector scope.



14. Apply a 5-step staircase wave (as in the figure below) to Y-IN, and measure the luminance level (Y) and the sync level (S) in the Y-OUT output.

$$L_S = \frac{S\ [mV]}{Y\ [mV]} \times 100\ [\%]$$



15. Measure the 3fsc (13.3 MHz) and fsc (4.43 MHz) components in the Y-OUT output with no input signal.

16. Measure the noise in the Y-OUT output with no input signal.
Measure the noise with a noise meter with a 200-kHz low-pass filter, a 5-MHz low-pass filter, and a 4.43-MHz trap filter.

17. Input a 200-kHz, 400-mVp-p sine wave to Y-IN1. Let V1 be the V-OUT output when SW3 is set to the ‘c’ position, and let V2 be the Y-OUT output when SW3 is set to the ‘b’ position.

$$Z_{OY} = \frac{V2\ [mVp\text{-}p] - V1\ [mVp\text{-}p]}{V1\ [mVp\text{-}p]} \times 500\ [\Omega]$$

18. Measure the delay time in the Y-OUT output with respect to the input to Y-IN.

Test Circuit