HARRIS Semiconductor

CA3060

110kHz, Operational Transconductance Amplifier Array

January 1999

Features

- Low Power Consumption as Low as 100mW Per Amplifier
- Independent Biasing for Each Amplifier
- High Forward Transconductance
- Programmable Range of Input Characteristics
- Low Input Bias and Input Offset Current
- High Input and Output Impedance
- No Effect on Device Under Output Short-Circuit Conditions
- Zener Diode Bias Regulator

Applications

- For Low Power Conventional Operational Amplifier Applications
- Active Filters
- Comparators
- Gyrators
- Mixers
- Modulators
- Multiplexers
- Multipliers
- Strobing and Gating Functions
- Sample and Hold Functions

Description

The CA3060 monolithic integrated circuit consists of an array of three independent Operational Transconductance Amplifiers (see Note). This type of amplifier has the generic characteristics of an operational voltage amplifier with the exception that the forward gain characteristic is best described by transconductance rather than voltage gain (open-loop voltage gain is the product of the transconductance and the load resistance, $g_M R_L$). When operated into a suitable load resistor and with provisions for feedback, these amplifiers are well suited for a wide variety of operational-amplifier and related applications. In addition, the extremely high output impedance makes these types particularly well suited for service in active filters.

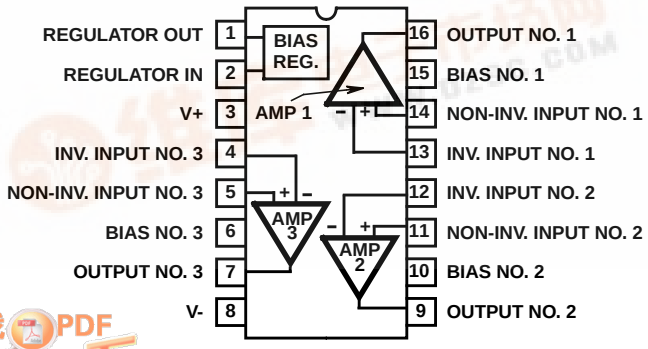
The three amplifiers in the CA3060 are identical push-pull Class A types which can be independently biased to achieve a wide range of characteristics for specific application. The electrical characteristics of each amplifier are a function of the amplifier bias current (I_{ABC}). This feature offers the system designer maximum flexibility with regard to output current capability, power consumption, slew rate, input resistance, input bias current, and input offset current. The linear variation of the parameters with respect to bias and the ability to maintain a constant DC level between input and output of each amplifier also makes the CA3060 suitable for a variety of nonlinear applications such as mixers, multipliers, and modulators.

In addition, the CA3060 incorporates a unique Zener diode regulator system that permits current regulation below supply voltages normally associated with such systems.

NOTE: Generic applications of the OTA are described in AN-6668. For improved input operating ranges, refer to CA3080 and CA3280 data sheets (File Nos. 475 and 1174) and application notes AN6668 and AN6818.

Pinout

CA3060
(PDIP)
TOP VIEW



Part Number Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CA3060E	-40 to 85	16 Ld PDIP	E16.3

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) . . . . . 36V (±18V)
Input Voltage. . . . . V+ to V-
Differential Input Voltage (Each Amplifier) 5V
Input Current (Each Amplifier) . . . . . ±1mA
Amplifier Bias Current (Each Amplifier) 2mA
Bias Regulator Input Current . . . . . -5mA
Output Short Circuit Duration (Note 1) . . . . . Indefinite

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
PDIP Package	90

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Short circuit may be applied to ground or to either supply.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$

PARAMETER	SYMBOL	AMPLIFIER BIAS CURRENT									UNITS
		$I_{ABC} = 1\mu A$			$I_{ABC} = 10\mu A$			$I_{ABC} = 100\mu A$			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (See Figure 1)	V_{IO}	-	1	-	-	1	-	-	1	5	mV
Input Offset Current (See Figure 2)	I_{IO}	-	3	-	-	30	-	-	250	1000	nA
Input Bias Current (See Figures 3, 4)	I_{IB}	-	33	-	-	300	-	-	2500	5000	nA
Peak Output Current (See Figures 5, 6)	I_{OM}	-	2.3	-	-	26	-	150	240	-	µA
Peak Output Voltage (See Figure 7)											
Positive	$V_{OM}+$	-	13.6	-	-	13.6	-	12	13.6	-	V
Negative	$V_{OM}-$	-	14.7	-	-	14.7	-	12	14.7	-	V
Amplifier Supply Current (Each Amplifier) (See Figures 8, 9)	I_A	-	8.5	-	-	85	-	-	850	1200	µA
Power Consumption (Each Amplifier)	P	-	0.26	-	-	2.6	-	-	26	36	mW
Input Offset Voltage Sensitivity (Note 3)											
Positive	$\Delta V_{IO}/\Delta V+$	-	1.5	-	-	2	-	-	2	150	µV/V
Negative	$\Delta V_{IO}/\Delta V-$	-	20	-	-	20	-	-	30	150	µV/V
Amplifier Bias Voltage (Note 4, See Figure 10)	V_{ABC}	-	0.54	-	-	0.60	-	-	0.66	-	V
DYNAMIC CHARACTERISTICS At 1kHz, Unless Otherwise Specified											
Forward Transconductance (Large Signal) (See Figures 11, 12)	g_{21}	-	1.55	-	-	18	-	30	102	-	mS
Common Mode Rejection Ratio	CMRR	-	110	-	-	110	-	70	90	-	dB
Common Mode Input Voltage Range	V_{ICR}	+12 to -12	+13 to -14	-	+12 to -12	+13 to -14	-	+12 to -12	+13 to -14	-	V
Slew Rate (Test Circuit) (See Figure 17)	SR	-	0.1	-	-	1	-	-	8	-	V/µs
Open Loop (g_{21}) Bandwidth (See Figure 13)	BW_{OL}	-	20	-	-	45	-	-	110	-	kHz

Electrical Specifications $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$ **(Continued)**

PARAMETER	SYMBOL	AMPLIFIER BIAS CURRENT									UNITS
		I_{ABC} = 1μA			I_{ABC} = 10μA			I_{ABC} = 100μA			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Impedance Components											
Resistance (See Figure 14)	R_I	-	1600	-	-	170	-	10	20	-	kΩ
Capacitance at 1MHz	C_I	-	2.7	-	-	2.7	-	-	2.7	-	pF
Output Impedance Components											
Resistance (See Figure 15)	R_O	-	200	-	-	20	-	-	2	-	MΩ
Capacitance at 1MHz	C_O	-	4.5	-	-	4.5	-	-	4.5	-	pF
ZENER BIAS REGULATOR CHARACTERISTICS I_2 = 0.1mA											
Voltage (See Figure 16)	V_Z	Temperature Coefficient = 3mV/^{o}C			6.2	6.7	7.9				V
Impedance	Z_Z				-	200	300				Ω

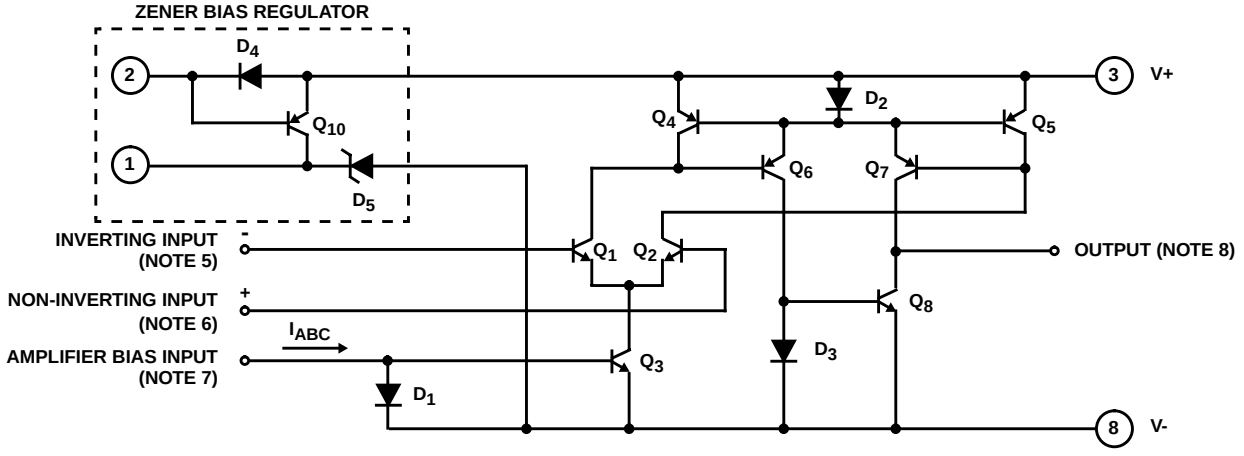
NOTES:

3. Conditions for Input Offset Voltage Sensitivity:
   a. Bias current derived from the regulator with an appropriate resistor connected from Terminal 1 to the bias terminal on the amplifier under test V+ is reduced to +13V for V+ sensitivity and V- is reduced to -13V for V- sensitivity.
   b. V+ Sensitivity in $\mu V/V = \frac{V_{Offset} - V_{Offset} \text{ for +13V and -15V Supplies}}{1V}$,

      V- Sensitivity in $\mu V/V = \frac{V_{Offset} - V_{Offset} \text{ for -13V and +15V Supplies}}{1V}$.
4. Temperature Coefficient; -2.2mV/^{o}C (at V_{ABC} = 0.54, I_{ABC} = 1μA); -2.1mV/^{o}C (at V_{ABC} = 0.060V, I_{ABC} = 10μA); -1.9mV/^{o}C (at V_{ABC} = 0.66V, I_{ABC} = 100μA)

Schematic Diagram

BIAS REGULATOR AND ONE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER



NOTES:

5. Inverting Input of Amplifiers 1, 2 and 3 is on Terminals 13, 12 and 4, respectively.
6. Non-inverting Input of Amplifiers 1, 2 and 3 is Terminals 14, 11 and 5, respectively.
7. Amplifier Bias Current of Amplifiers 1, 2 and 3 is on Terminals 15, 10 and 6, respectively.
8. Output of Amplifiers 1, 2 and 3 is on Terminals 16, 9 and 7, respectively.

Typical Performance Curves

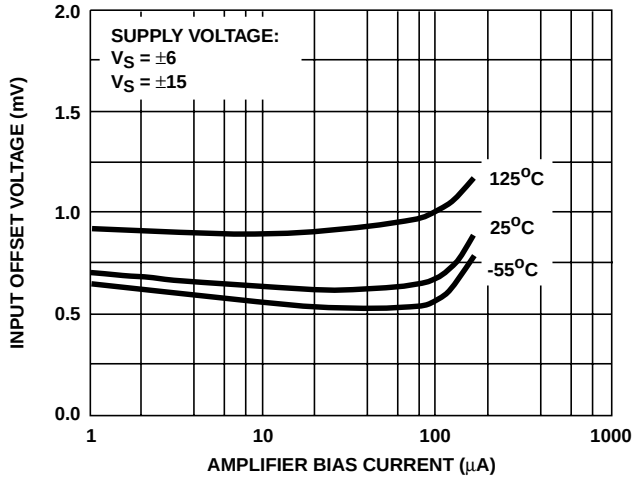


FIGURE 1. INPUT OFFSET VOLTAGE vs AMPLIFIER BIAS CURRENT

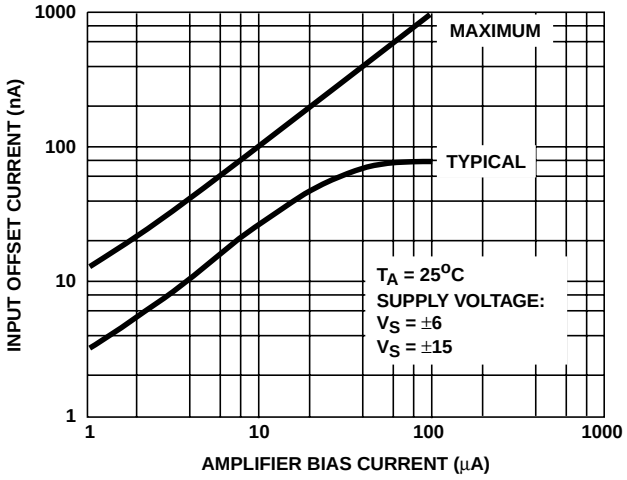


FIGURE 2. INPUT OFFSET CURRENT vs AMPLIFIER BIAS CURRENT

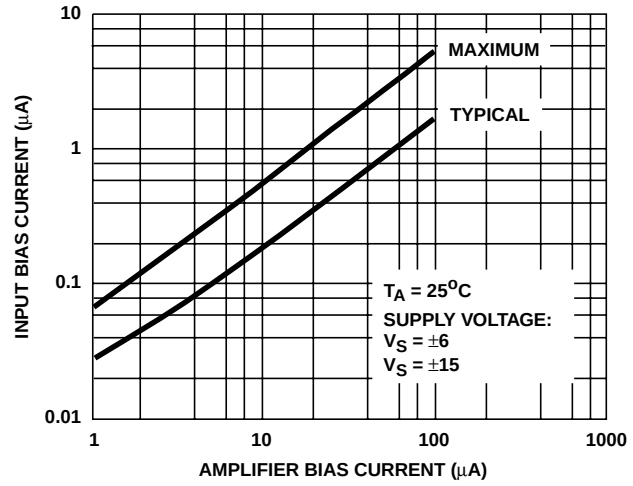


FIGURE 3. INPUT BIAS CURRENT vs AMPLIFIER BIAS CURRENT

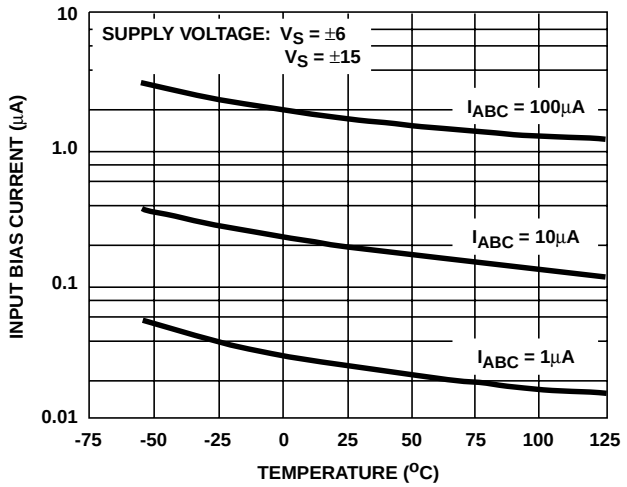


FIGURE 4. INPUT BIAS CURRENT vs TEMPERATURE

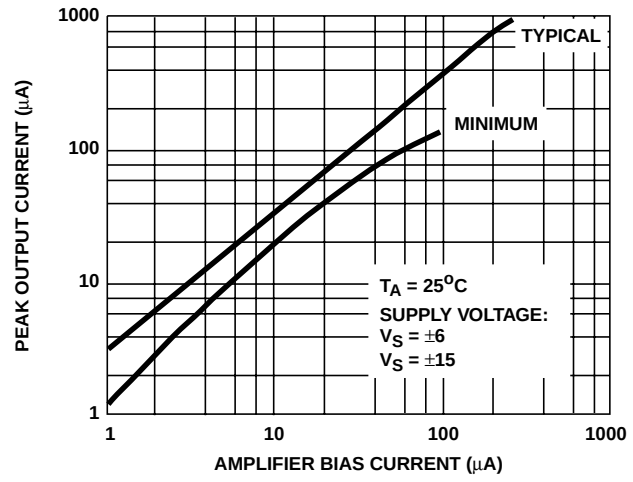


FIGURE 5. PEAK OUTPUT CURRENT vs AMPLIFIER BIAS CURRENT

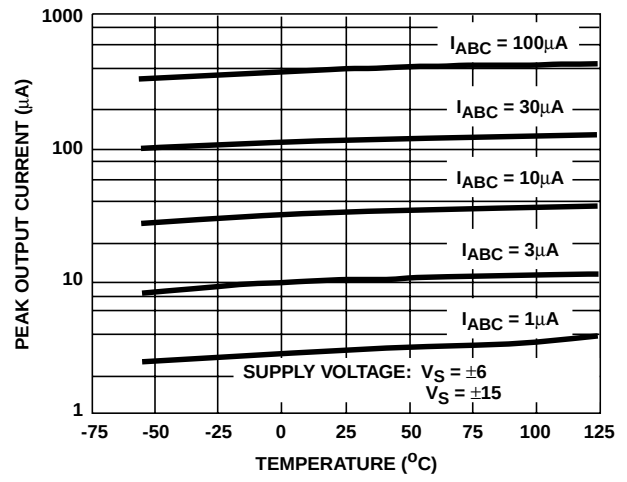


FIGURE 6. PEAK OUTPUT CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

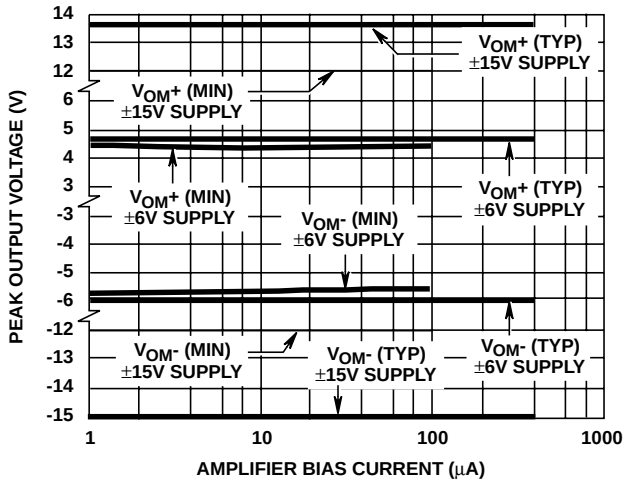


FIGURE 7. PEAK OUTPUT VOLTAGE vs AMPLIFIER BIAS CURRENT

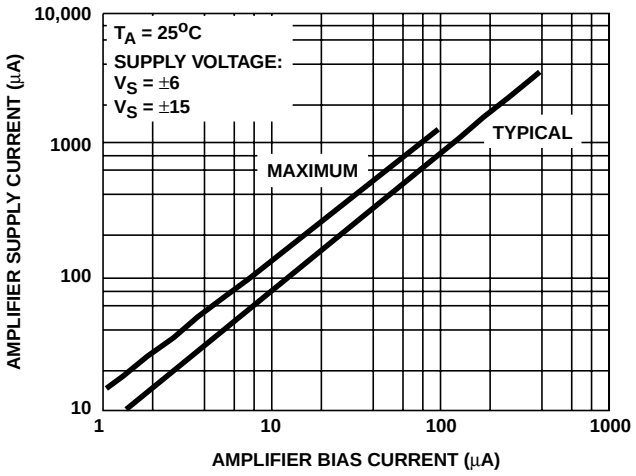


FIGURE 8. AMPLIFIER SUPPLY CURRENT (EACH AMPLIFIER) vs AMPLIFIER BIAS CURRENT

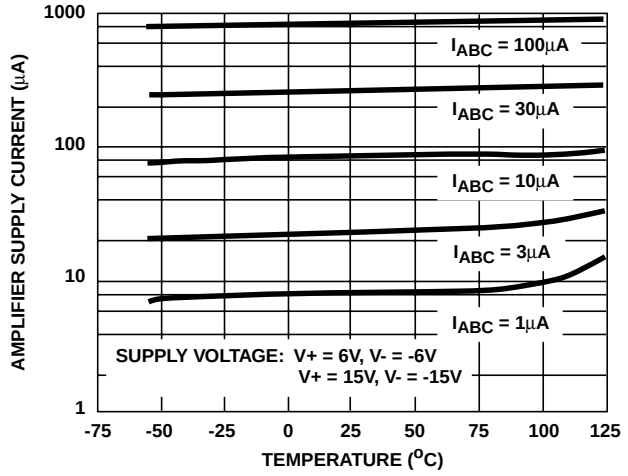


FIGURE 9. AMPLIFIER SUPPLY CURRENT (EACH AMPLIFIER) vs TEMPERATURE

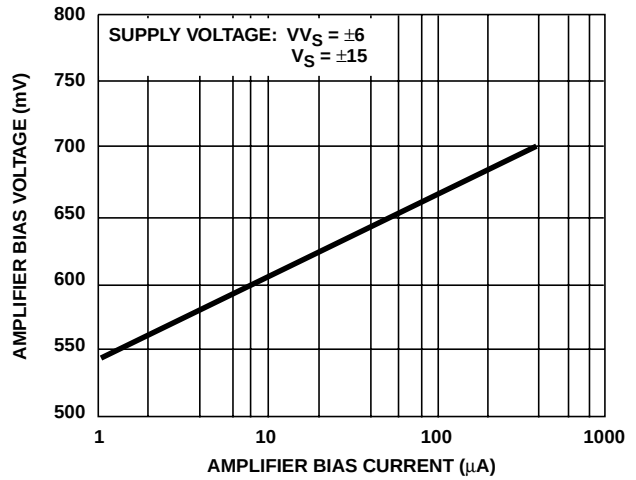


FIGURE 10. AMPLIFIER BIAS VOLTAGE vs AMPLIFIER BIAS CURRENT

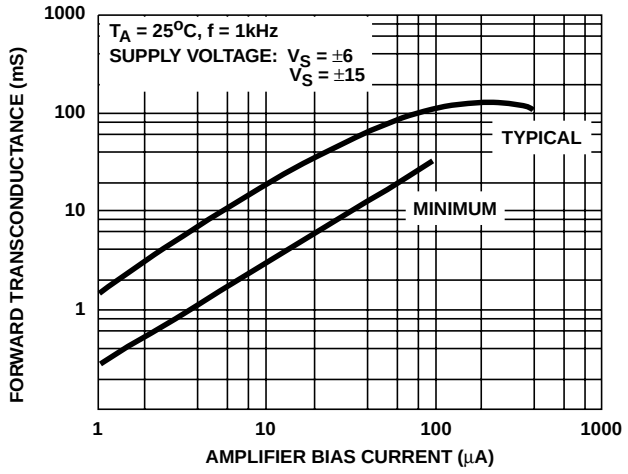


FIGURE 11. FORWARD TRANSCONDUCTANCE vs AMPLIFIER BIAS CURRENT

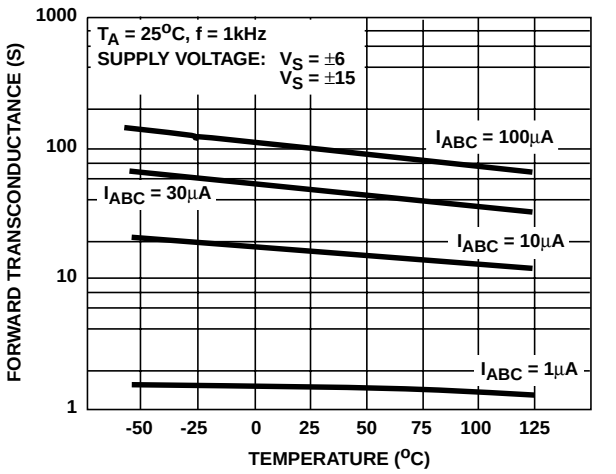


FIGURE 12. FORWARD TRANSCONDUCTANCE vs TEMPERATURE

Typical Performance Curves (Continued)

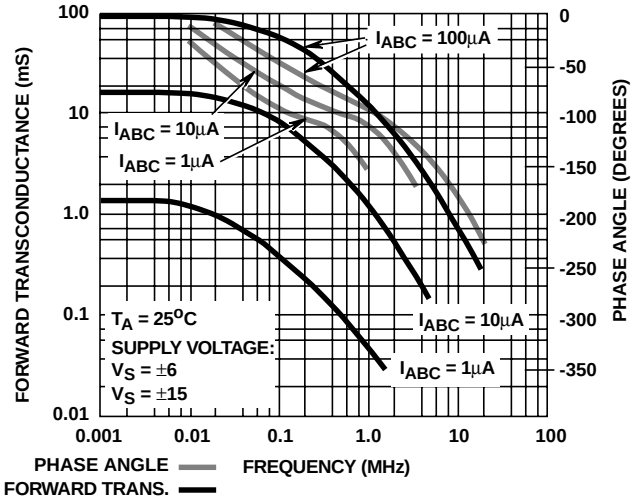


FIGURE 13. FORWARD TRANSCONDUCTANCE vs FREQUENCY

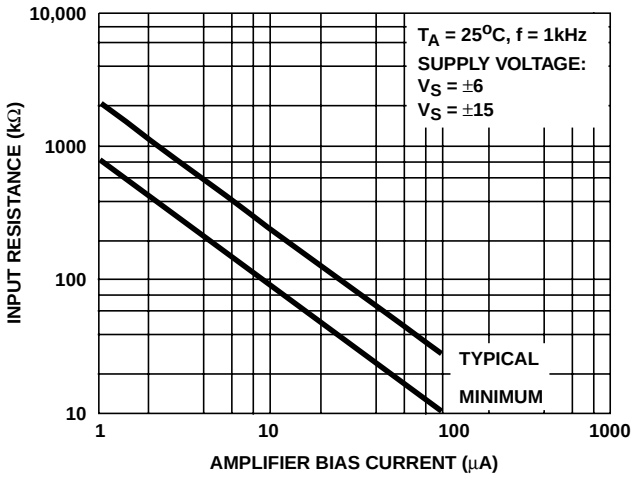


FIGURE 14. INPUT RESISTANCE vs AMPLIFIER BIAS CURRENT

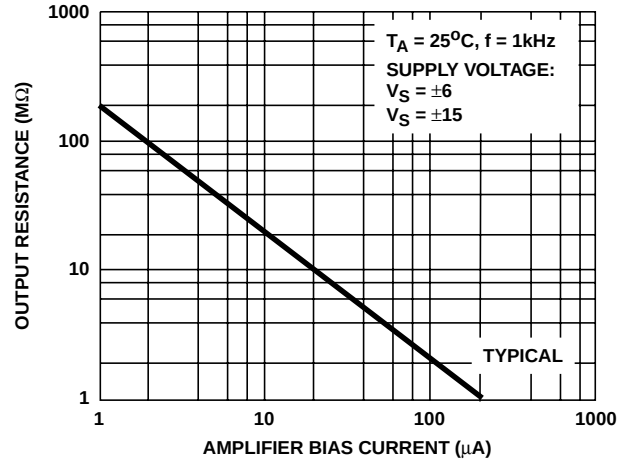


FIGURE 15. OUTPUT RESISTANCE vs AMPLIFIER BIAS CURRENT

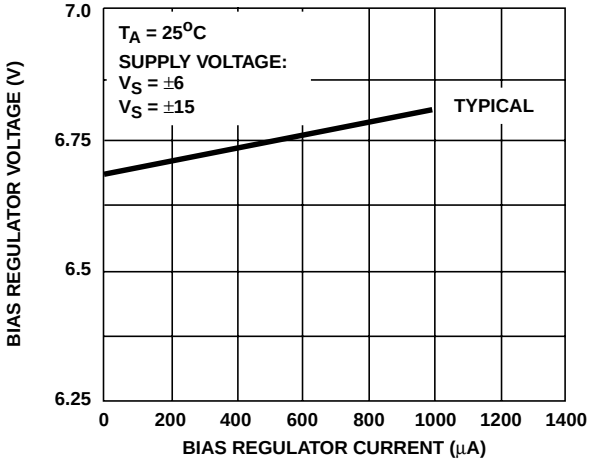
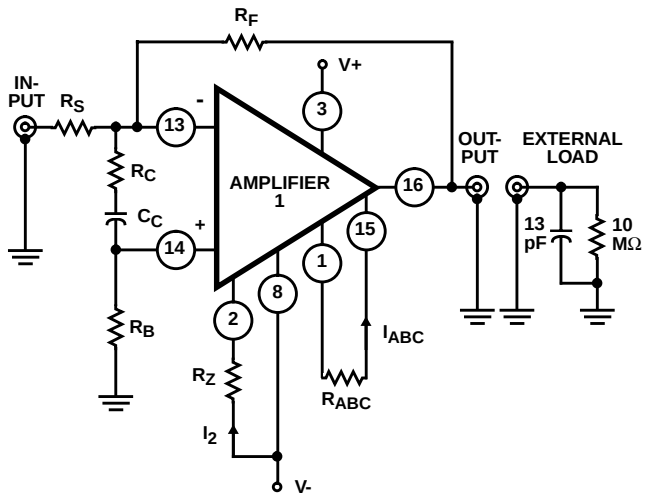


FIGURE 16. BIAS REGULATOR VOLTAGE vs BIAS REGULATOR CURRENT

Test Circuit



V_Z is measured between Terminal 1 and 8
V_{ABC} is measured between Terminals 15 and 8

$$R_Z = \frac{[(V+)-(V-)-0.7]}{I_2},\ R_{ABC} = \frac{V_Z - V_{ABC}}{I_{ABC}}$$

Supply Voltage: For both ±6V and ±15V

TYPICAL SLEW RATE TEST CIRCUIT PARAMETERS

I_{ABC}	SLEW RATE	I_2	R_{ABC}	R_S	R_F	R_B	R_C	C_C
μA	V/μs	μA	Ω	Ω	Ω	Ω	Ω	μF
100	8	200	62K	100K	100K	51K	100	0.02
10	1	200	620K	1M	1M	510K	1K	0.005
1	0.1	2	6.2M	10M	10M	5.1M	∞	0

FIGURE 17. SLEW RATE TEST CIRCUIT FOR AMPLIFIER 1 OF CA3060

Application Information

The CA3060 consists of three operational amplifiers similar in form and application to conventional operational amplifiers but sufficiently different from the standard operational amplifier (op amp) to justify some explanation of their characteristics. The amplifiers incorporated in the CA3060 are best described by the term Operational Transconductance Amplifier (OTA). The characteristics of an ideal OTA are similar to those of an ideal op amp except that the OTA has an extremely high output impedance. Because of this inherent characteristics the output signal is best defined in terms of current which is proportional to the difference between the voltages of the two input terminals. Thus, the transfer characteristics is best described in terms of transconductance rather than voltage gain. Other than the difference given above, the characteristics tabulated are similar to those of any typical op amp.

The OTA circuitry incorporated in the CA3060 (Figure 18) provides the equipment designer with a wider variety of circuit arrangements than does the standard op amp; because as the curves indicate, the user may select the optimum circuit conditions for a specific application simply by varying the bias conditions of each amplifier. If low power consumption, low bias, and low offset current, or high input impedance are primary design requirements, then low current operating conditions may be selected. On the other hand, if operation into a moderate load impedance is the primary consideration, then higher levels of bias may be used.

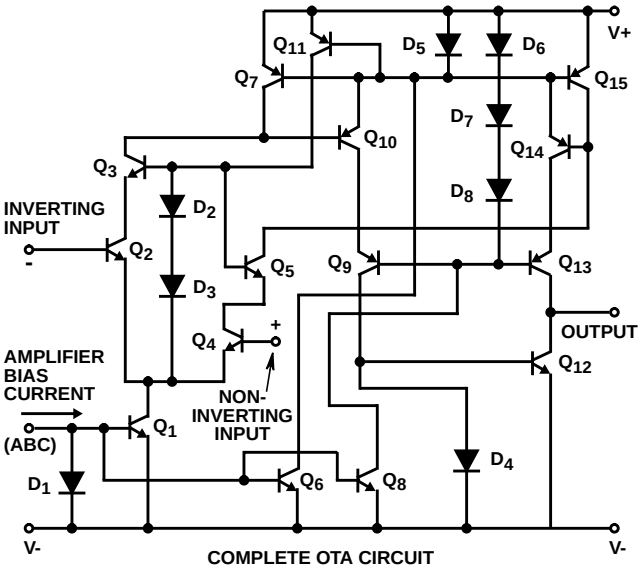


FIGURE 18. COMPLETE SCHEMATIC DIAGRAM SHOWING BIAS REGULATOR AND ONE OF THE THREE OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS

Bias Consideration for Op Amp Applications

The operational transconductance amplifiers allow the circuit designer to select and control the operating conditions of the circuit merely by the adjustment of the amplifier bias current I_{ABC}. This enables the designer to have complete control over transconductance, peak output current and total power consumption independent of supply voltage.

In addition, the high output impedance makes these amplifiers ideal for applications where current summing is involved.

The design of a typical operational amplifier circuit (Figure 19) would proceed as follows:

Circuit Requirements
Closed Loop Voltage Gain = 10 (20dB)
Offset Voltage Adjustable to Zero
Current Drain as Low as Possible
Supply Voltage = ±6V
Maximum Input Voltage = ±50mV
Input Resistance = 20kΩ
Load Resistance = 20kΩ
Device: CA3060

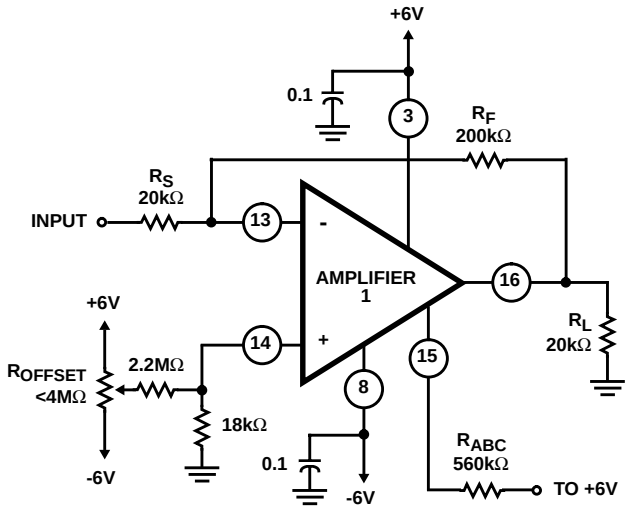


FIGURE 19. 20dB AMPLIFIER USING THE CA3060

Calculation

1. **Required Transconductance g_{21}.** Assume that the open loop gain A_{OL} must be at least ten times the closed loop gain. Therefore, the forward transconductance required is given by:

   $g_{21} = A_{OL}/R_L$
   $= 100/18k\Omega$
   $\cong 5.5mS$
   (R_L = 20kΩ in parallel with 200kΩ ≅ 18kΩ)

2. **Selection of Suitable Amplifier Bias Current.** The amplifier bias current is selected from the minimum value curve of transconductance (Figure 11) to assure that the amplifier will provide sufficient gain. For the required g_{21} of 5.5mS an amplifier bias current I_{ABC} of 20µA is suitable.

3. **Determination of Output Swing Capability.** For a closed loop gain of 10 the output swing is ±0.5V and the peak load current is 25µA. However, the amplifier must also supply the necessary current through the feedback resistor and if R_S = 20kΩ, then R_F = 200kΩ for A_{CL} = 10. Therefore, the feedback loading = 0.5V/200kΩ = 2.5µA.

   The total amplifier current output requirements are, therefore, ±27.5µA. Referring to the data given in Figure 5, we see that for an amplifier bias current of 20µA the amplifier output current is ±40µA. This is obviously adequate and it is not necessary to change the amplifier bias current I_{ABC}.

4. **Calculation of Bias Resistance.** For minimum supply current drain the amplifier bias current I_{ABC} should be fed directly from the supplies and not from the bias regulator. The value of the resistor R_{ABC} may be directly calculated using Ohm's law.

$$R_{ABC} = \frac{V_{SUP} - V_{ABC}}{I_{ABC}}$$

$$R_{ABC} = \frac{12 - 0.63}{20 \times 10^{-6}}$$

$$R_{ABC} = 568.5k\Omega \text{ or } \cong 560k\Omega$$

5. **Calculation of Offset Adjustment Circuit.** In order to reduce the loading effect of the offset adjustment circuit on the power supply, the offset control should be arranged to provide the necessary offset current. The source resistance of the non-inverting input is made equal to the source resistance of the inverting input,

$$\text{i.e., } \frac{20k\Omega \times 200k\Omega}{20k\Omega + 200k\Omega} \cong 18k\Omega$$

Because the maximum offset voltage is 5mV plus an additional increment due to the offset current (Figure 2) flowing through the source resistance (i.e., 200 x 10^{-9} x 18 x 10^{3}V), the Offset Voltage Range = 5mV + 3.6mV = ±8.6mV. The current necessary to provide this offset is:

$$\frac{8.6mV}{18k\Omega} \cong 0.48\mu A$$

With a supply voltage of ±6V, this current can be provided by a 10MΩ resistor. However, the stability of such a resistor is often questionable and a more realistic value of 2.2MΩ was used in the final circuit.

Capacitance Effects

The CA3060 is designed to operate at such low power levels that high impedance circuits must be employed. In designing such circuits, particularly feedback amplifiers, stray circuit capacitance must always be considered because of its adverse effect on frequency response and stability. For example a 10kΩ load with a stray capacitance of 15pF has a time constant of 1MHz. Figure 20 illustrates how a 10kΩ 15pF load modifies the frequency characteristic.

Capacitive loading also has an effect on slew rate; because the peak output current is established by the amplifier bias current, I_{ABC} (Figure 5), the maximum slew rate is limited to the maximum rate at which the capacitance can be charged by the I_{OM}. Therefore, SR = dv/dt = I_{OM}/C_L, where C_L is the total load capacitance including strays. This relationship is shown graphically in Figure 21. When measuring slew rate for this data sheet, care was taken to keep the total capacitive loading to 13pF.

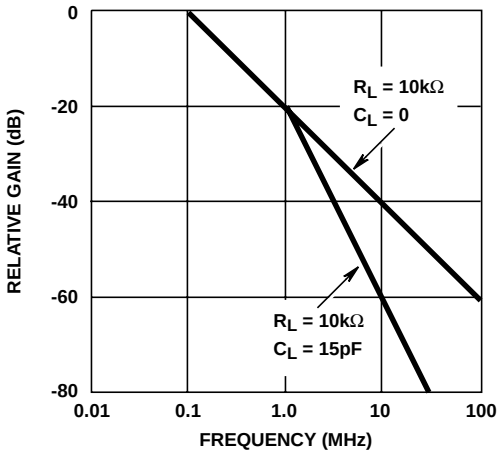
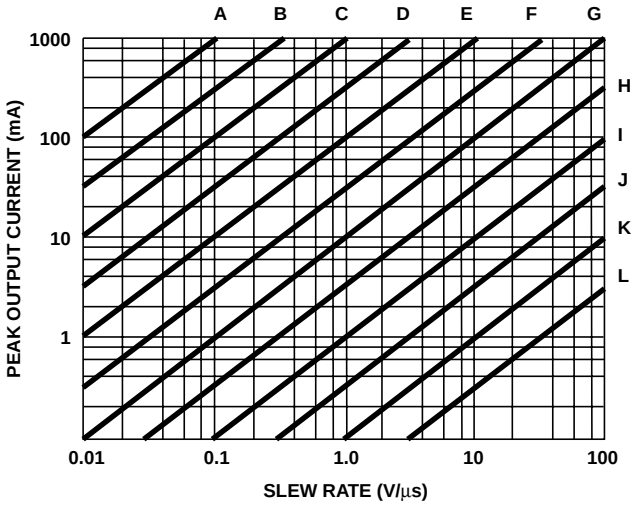


FIGURE 20. EFFECT OF CAPACITIVE LOADING ON FREQUENCY RESPONSE



A. C_L = 10,000pF
B. C_L = 3,000pF
C. C_L = 1000pF
D. C_L = 300pF
E. C_L = 100pF
F. C_L = 30pF
G. C_L = 10pF
H. C_L = 3pF
I. C_L = 1pF
J. C_L = 0.3pF
K. C_L = 0.1pF
L. C_L = 0.03pF

FIGURE 21. EFFECT OF LOAD CAPACITANCE ON SLEW RATE

Phase Compensation

In many applications phase compensation will not be required for the amplifiers of the CA3060. When needed, compensation may easily be accomplished by a simple RC network at the input of the amplifier as shown in Figure 17. The values given in Figure 17 provide stable operation for the critical unity gain condition, assuming that capacitive loading on the output is 13pF or less. Input phase compensation is recommended in order to maintain the highest possible slew rate.

In applications such as integrators, two OTAs may be cascaded to improve current gain. Compensation is best accomplished in this case with a shunt capacitor at the output of the first amplifier. The high gain following compensation assures a high slew rate.

Typical Applications

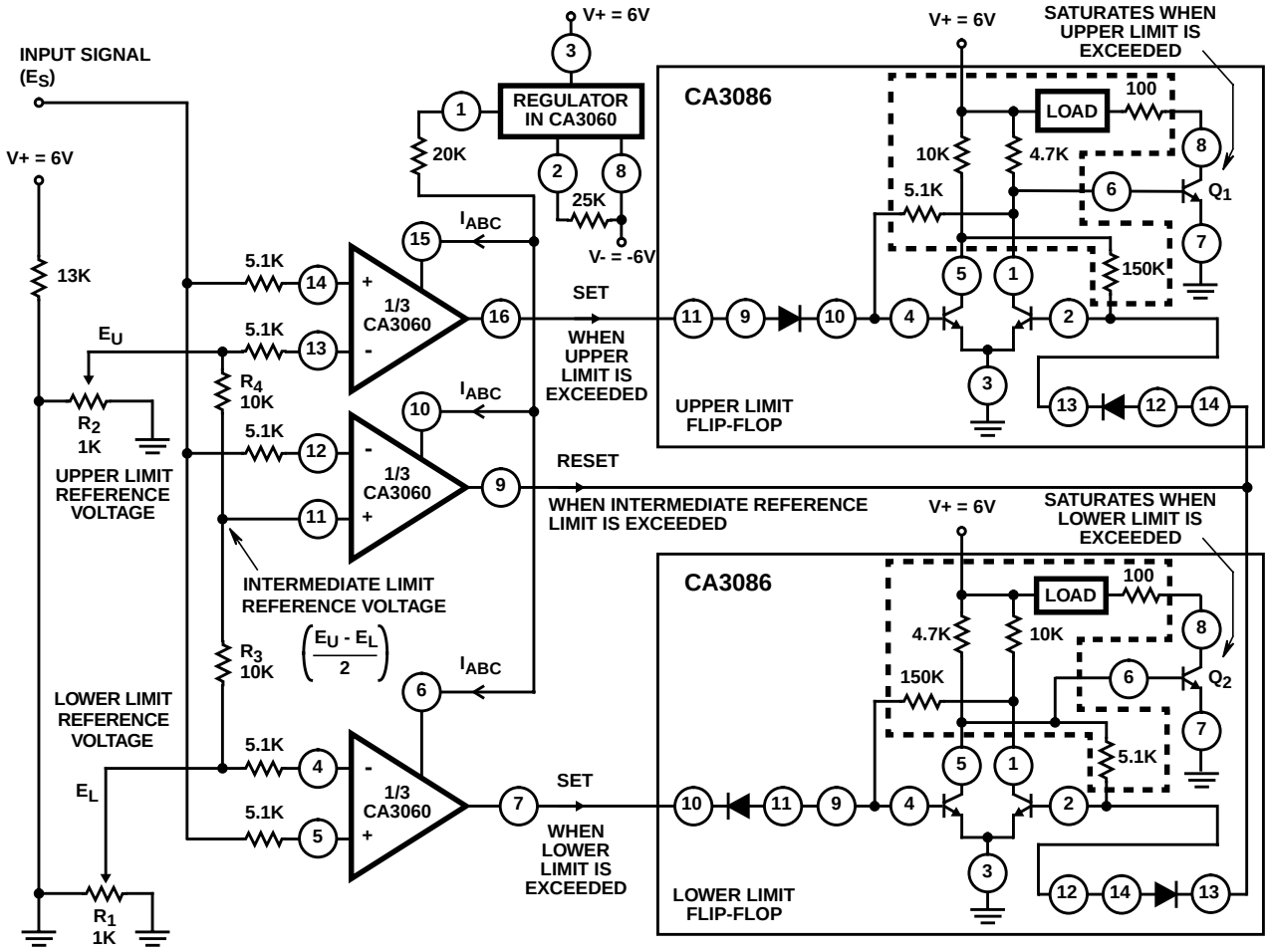
Having determined the operating points of the CA3060 amplifiers, they can now function in the same manner as conventional op amps, and thus, are well suited for most op amp applications, including inverting and non-inverting amplifiers, integrators, differentiators, summing amplifiers etc.

Tri-Level Comparator

Tri-level comparator circuits are an ideal application for the CA3060 since it contains the requisite three amplifiers. A tri-level comparator has three adjustable limits. If either the upper lower limit is exceeded, the appropriate output is activated until the input signal returns to a selected intermediate limit. Tri-level comparators are particularly suited to many industrial control applications.

Circuit Description

Figure 23 shows the block diagram of a tri-level comparator using the CA3060. Two of the three amplifiers are used to compare the input signal with the upper limit and lower limit reference voltages. The third amplifier is used to compare the input signal with a selected value of intermediate limit reference voltage. By appropriate selection of resistance ratios this intermediate limit may be set to any voltage between the upper limit and lower limit values. The output of the upper limit and lower limit comparator sets the corresponding upper or lower limit flip-flop. The activated flip-flop retains its state until the third comparator (intermediate limit) in the CA3060 initiates a reset function, thereby indicating that the signal voltage has returned to the intermediate limit selected. The flip-flops employ two CA3086 transistor array ICs, with circuitry to provide separate “SET” and “POSITIVE OUTPUT” terminals.



NOTES:

9. Items in dashed boxes are external to the CA3086. All resistance values are in ohms.

10. $E_S > E_U = Q_1(ON), Q_2(OFF)$

$E_L < E_U = Q_2(ON), Q_1(OFF)$

$E_S < \frac{E_U - E_L}{2} = Q_1(OFF), Q_2(OFF)$

FIGURE 22. TRI-LEVEL COMPARATOR CIRCUIT

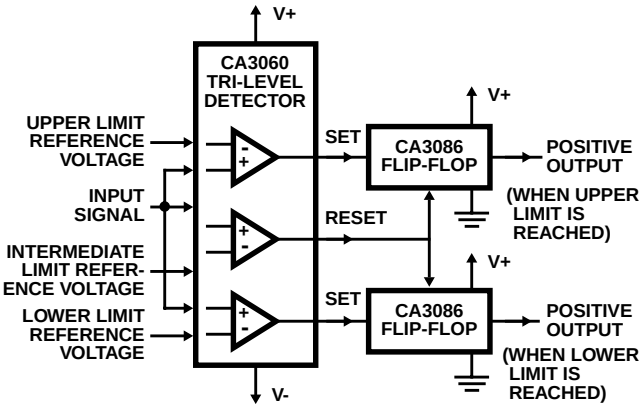


FIGURE 23. FUNCTIONAL BLOCK DIAGRAM OF A TRI-LEVEL COMPARATOR

The circuit diagram of a tri-level comparator appears in Figure 22. Power is provided for the CA3060 via terminal 3 and 8 by ±6V supplies and the built-in regulator provides amplifier bias current (I_{ABC}) to the three amplifiers via terminal 1. Lower limit and upper limit reference voltages are selected by appropriate adjustment of potentiometers R_1 and R_2, respectively. When resistors R_3 and R_4 are equal in value (as shown), the intermediate limit reference voltage is automatically established at a value midway between the lower limit and upper limit values. Appropriate variation of resistors R_3 and R_4 permits selection of other values of intermediate limit voltage. Input signal (E_S) is applied to the three comparators via terminals 5, 12 and 14. The "SET" output lines trigger the appropriate flip-flop whenever the input signal reaches a limit value. When the input signal returns to an intermediate value, the common flip-flop "RESET" line is energized. The loads in the circuits, shown in Figure 22 are 5V, 25mA lamps.

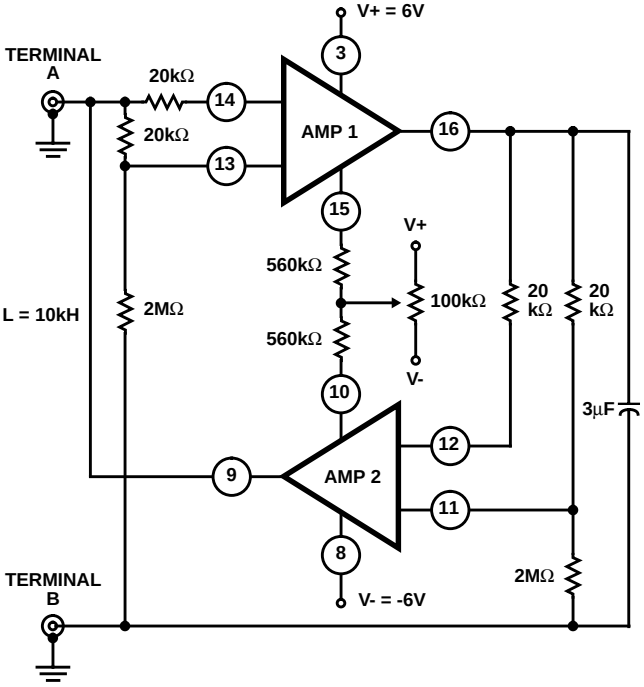


FIGURE 24. TWO OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS OF THE CA3060 CONNECTED AS A GYRATOR IN AN ACTIVE FILTER CIRCUIT

Active Filters - Using the CA3060 as a Gyrator

The high output impedance of the OTAs makes the CA3060 ideally suited for use as a gyrator in active filter applications. Figure 24 shows two OTAs of the CA3060 connected as a gyrator in an active filter circuit. The OTAs in this circuit can make a 3μF capacitor function as a floating 10kH inductor across Terminals A and B. The measured Q of 13 (at a frequency of 1Hz) of this inductor compares favorably with a calculated Q of 16. The 20kΩ to 2MΩ attenuators in this circuit extend the dynamic range of the OTA by a factor of 100. The 100kΩ potentiometer, across V+ and V-, tunes the inductor by varying the g_{21} of the OTAs, thereby changing the gyration resistance.

Three Channel Multiplexer

Figure 25 shows a schematic of a three channel multiplexer using a single CA3060 and a 3N153 MOSFET as a buffer and power amplifier.

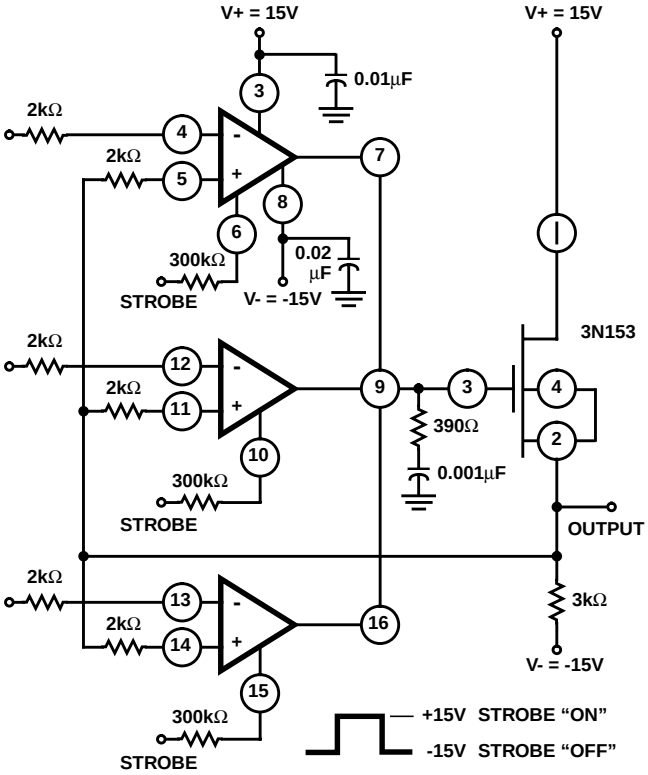


FIGURE 25. THREE CHANNEL MULTIPLEXER

When the CA3060 is connected as a high input impedance voltage follower, and strobe "ON", each amplifier is activated and the output swings to the level of the input of the amplifier. The cascade arrangement of each CA3060 amplifier with the MOSFET provides an open loop voltage gain in excess of 100dB, thus assuring excellent accuracy in the voltage follower mode with 100% feedback. Operation at ±6V is also possible with several minor changes. First, the resistance in series with the amplifier bias current (I_{ABC}) terminal of each amplifier should be decreased to maintain 100μA of strobe "ON" current at this lower supply voltage. Second, the drain resistance for the MOSFET should be

decreased to maintain the same value of source current. The low cost dual gate protected MOSFET, 40841 type, may be used when operating at the low supply voltage.

The phase compensation network consists of a single 390Ω resistor and a 1000pF capacitor, located at the interface of the CA3060 output and the MOSFET gate. The bandwidth of the system is 1.5MHz and the slew rate is 0.3V/µs. The system slew rate is directly proportional to the value of the phase compensation capacitor. Thus, with higher gain settings where lower values of phase compensation capacitors are possible, the slew rate is proportionally increased.

Non-Linear Applications

AM Modulator (Two Quadrant Multiplier)

Figure 26 shows Amplifier 3 of the CA3060 used in an AM modulator or two quadrant multiplier circuit. When modulation is applied to the amplifier bias input, Terminal B, and the carrier frequency to the differential input, Terminal A, the waveform, shown in Figure 26 is obtained. Figure 26 is a result of adjusting the input offset control to balance the circuit so that no modulation can occur at the output without a carrier input. The linearity of the modulator is indicated by the solid trace of the superimposed modulating frequency. The maximum depth of modulation is determined by the ratio of the peak input modulating voltage to V-.

The two quadrant multiplier characteristic of this modulator is easily seen if modulation and carrier are reversed as shown in Figure 26. The polarity of the output must follow that of the differential input; therefore, the output is positive only during, the positive half cycle of the modulation and negative only in the second half cycle. Note, that both the input and output signals are referenced to ground. The output signal is zero when either the differential input or I_{ABC} are zero.

Four Quadrant Multiplier

The CA3060 is also useful as a four quadrant multiplier. A block diagram of such a multiplier, utilizing Amplifiers 1, 2 and 3 is shown in Figure 27 and a typical circuit is shown in Figure 28. The multiplier consists of a single CA3060 and, as in the two quadrant multiplier, exhibits no level shift between input and output. In Figure 27, Amplifier 1 is connected as an inverting amplifier for the X-input signal. The output current of Amplifier 1 is calculated as follows:

$$I_O(1) = [-V_X]\,[g_{21}(1)] \qquad \text{EQ. 1}$$

Amplifier 2 is a non-inverting amplifier so that

$$IO(2) = [+VX]\,[g_{21}(2)] \qquad \text{EQ. 2}$$

Because the amplifier output impedances are high, the load current is the sum of the two output currents, for an output voltage

$$V_O = V_X R_L\,[g_{21}(2) - g_{21}(1)] \qquad \text{EQ. 3}$$

The transconductance is approximately proportional to the amplifier bias current; therefore, by varying the bias current the g_{21} is also controlled. Amplifier 2 bias current is proportional to the Y-input signal and is expressed as

$$I_{ABC(2)} \approx \frac{(V-) + V_Y}{R_1} \qquad \text{EQ. 4}$$

Hence,

$$g_{21}(2) \approx k\,[(V-) + V_Y] \qquad \text{EQ. 5}$$

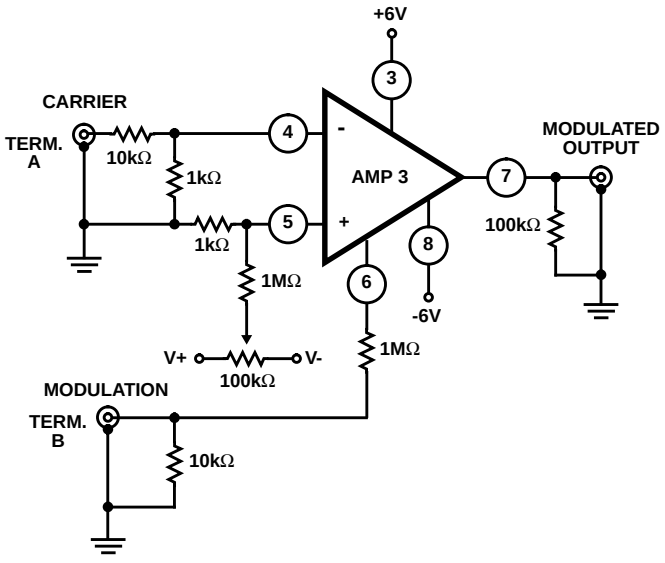
Bias for Amplifier 1 is derived from the output of Amplifier 3 which is connected as a unity gain inverting amplifier. $I_{ABC(1)}$, therefore, varies inversely with V_Y. And by the same reasoning as above

$$g_{21}(1) \approx k\,[(V-) - V_Y] \qquad \text{EQ. 6}$$

Combining Equations 3, 5 and 6 yields:

$$V_O \approx V_X \times k \times R_L\,\{[(V-) + V_Y] - [(V-) - V_Y]\} \text{ or}$$

$$V_O \approx 2kR_L V_X V_Y$$



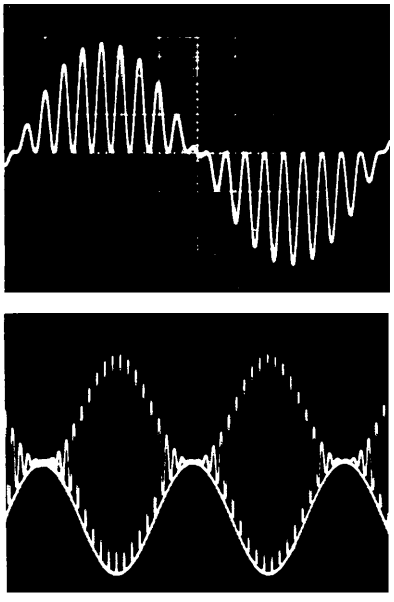


FIGURE 26. TWO QUADRANT MULTIPLIER CIRCUIT USING THE CA3060 WITH ASSOCIATED WAVEFORMS

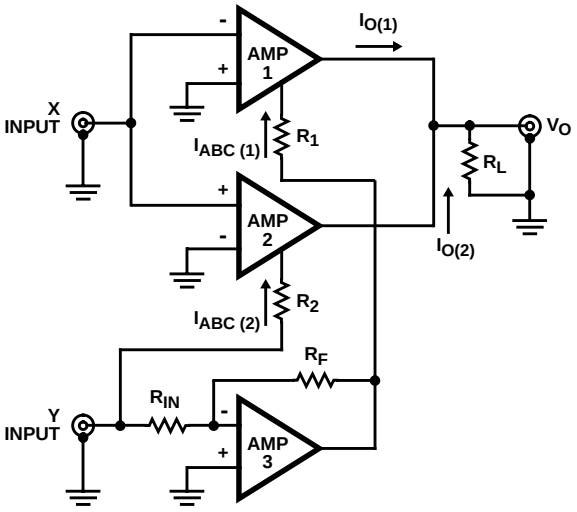


FIGURE 27. FOUR QUADRANT MULTIPLIER

Figure 28 shows the actual circuit including all the adjustments associated with differential input and an adjustment for equalizing the gains of Amplifiers 1 and 2. Adjustment of the circuit is quite simple. With both the X and Y voltages at zero, connect Terminal 10 to Terminal 8. This procedure disables Amplifier 2 and permits adjusting the offset voltage of Amplifier 1 to zero by means of the 100kΩ potentiometer. Next, remove the short between Terminal 10 and 8 and connect Terminal 15 to Terminal 8. This step disables Amplifier 1 and permits Amplifier 2 to be zeroed with the other potentiometer. With AC signals on both the X and Y inputs, R_3 and R_{11} are adjusted for symmetrical output signals. Figure 29 shows the output waveform with the multiplier adjusted. The voltage waveform in Figure 29A shows suppressed carrier modulation of 1kHz carrier with a triangular wave.

Figures 29B and 29C, respectively, show the squaring of a triangular wave and a sine wave. Notice that in both cases the output is always positive and returns to zero after each cycle.

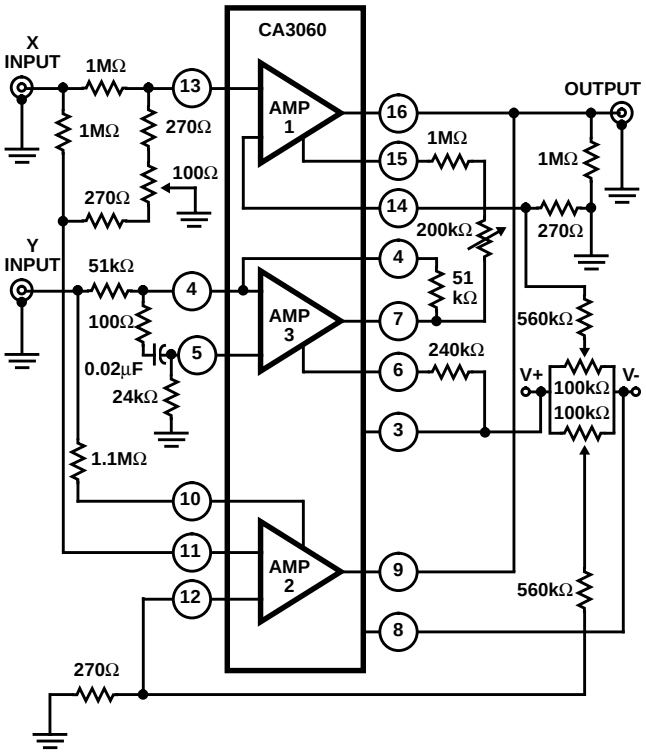


FIGURE 28. TYPICAL FOUR QUADRANT MULTIPLIER CIRCUIT

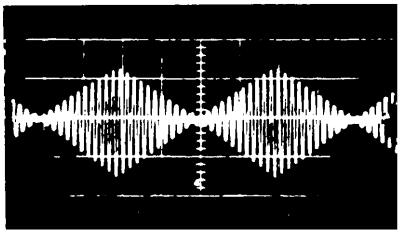


FIGURE 29A.

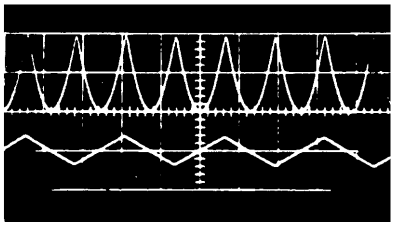


FIGURE 29B.

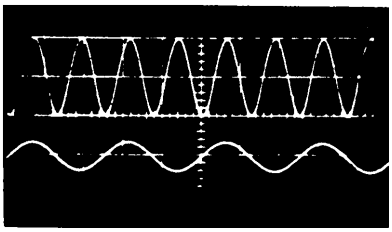


FIGURE 29C.

FIGURE 29. VOLTAGE WAVEFORMS OF FOUR QUADRANT MULTIPLIER CIRCUIT