

CA3141

High-Voltage Diode Array For Commercial, Industrial and Military Applications

January 1999

**OBSOLETE PRODUCT
 NO RECOMMENDED REPLACEMENT**
 Call Central Applications 1-800-442-7747
 or email: centapp@harris.com

Features

- Matched Monolithic Construction
 - V_F Match (Each Diode Pair) 0.55mV At $I_F = 1\text{mA}$
- Low Diode Capacitance. 0.3pF (Typ) at $V_R = 2\text{V}$
- High Diode-to-Substrate Breakdown. 30V (Min)
- Low Reverse (Leakage) Current 100nA (Max)

Applications

- Balanced Modulators or Demodulators
- Analog Switches
- High-Voltage Diode Gates
- Current Ratio Detectors

Part Number Information

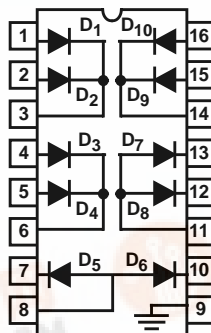
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3141E	-55 to 125	16 Ld PDIP	E16.3

Description

The CA3141E High Voltage Diode Array Consists of ten general purpose high reverse breakdown diodes. Six diodes are internally connected to form three common cathode diode pairs, and the remaining four diodes are internally connected to form two common anode diode pairs. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the CA3141 extremely useful for a wide variety of applications in communications and switching systems.

Pinout

CA3141
 (PDIP)
 TOP VIEW



CA3141

Absolute Maximum Ratings

Inverse Voltage (PIV)	30V
Peak Diode -to-Substrate Voltage	30V
Peak Forward Surge Current [I_F (Surge)]	100mA
DC Forward Current (I_F)	25mA

Operating Conditions

Temperature Range	-55°C to 125°C
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CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	90
Maximum Power Dissipation (Any One Diode)	50mW
Maximum Junction Temperature (Die)	175°C
Maximum Junction Temperature (Plastic Package)	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C

Electrical Specifications $T_A = 25^\circ\text{C}$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC Forward Voltage Drop	V_F	I_F (Anode) 100 μA	-	0.7	0.9	V
		1mA	-	0.78	1	V
		10mA	-	0.93	1.2	V
DC Reverse Breakdown Voltage	$V_{(BR)R}$	$I_F = -10\mu\text{A}$	30	50	-	V
DC Breakdown Voltage Between Any Diode and Substrate	$V_{(BR)DI}$	$I_{DI} = 10\mu\text{A}$	30	50	-	V
DC Reverse (Leakage) Current	I_R	$V_F = -20\text{V}$	-	-	100	nA
DC Reverse (Leakage) Current Between Any Diode and Substrate	I_{DI}	$V_{DI} = 20\text{V}$	-	-	100	nA
Magnitude of Diode Offset Voltage Between Diode Pairs		$V_{DI} = 20\text{V}, I_{FA} = 1\text{mA}$	-	0.55	-	mV
Temperature Coefficient of Forward Voltage Drop	$\Delta V_F/\Delta T$	$I_F = 1\text{mA}$	-	-1.5	-	mV/°C
Reverse Recovery Time	t_{RR}	$I_F = 2\text{mA}, I_R = 2\text{mA}$	-	50	-	ns
Diode Capacitance	C_D		See Figure 4			pF
Diode Anode-to-Substrate Capacitance	C_{DAI}		See Figure 5			pF
Diode Cathode-to-Substrate Capacitance	C_{DCI}		See Figure 6			pF
Magnitude of Cathode-to-Anode Current Ratio	$ I_{FC}/I_{FA} $	$I_{FA} = 1\text{mA}, V_{DS} = 10\text{V}$	0.9	0.96	-	-

Typical Performance Curves

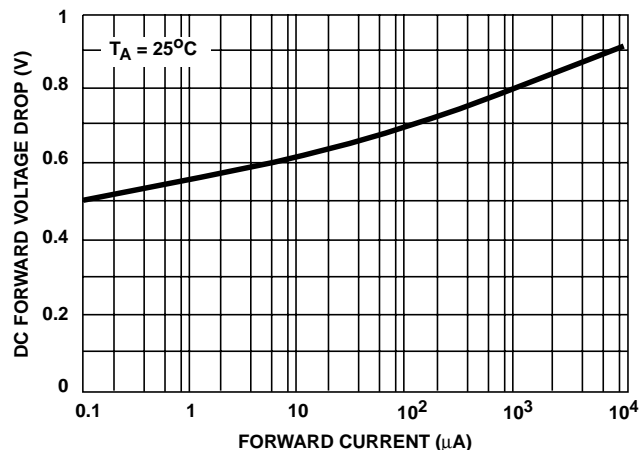


FIGURE 1. DC FORWARD VOLTAGE DROP vs FORWARD CURRENT

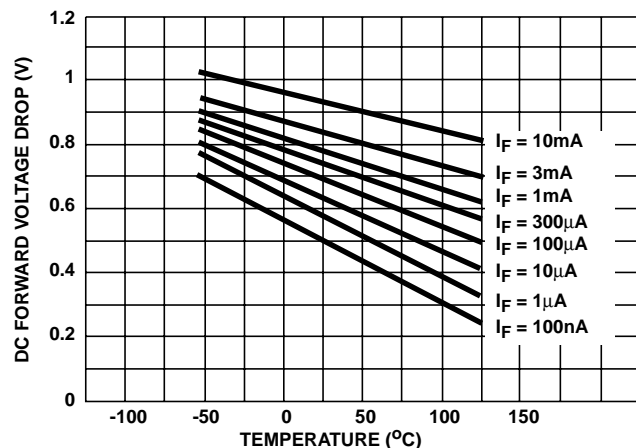


FIGURE 2. DC FORWARD VOLTAGE DROP vs TEMPERATURE

Typical Performance Curves (Continued)

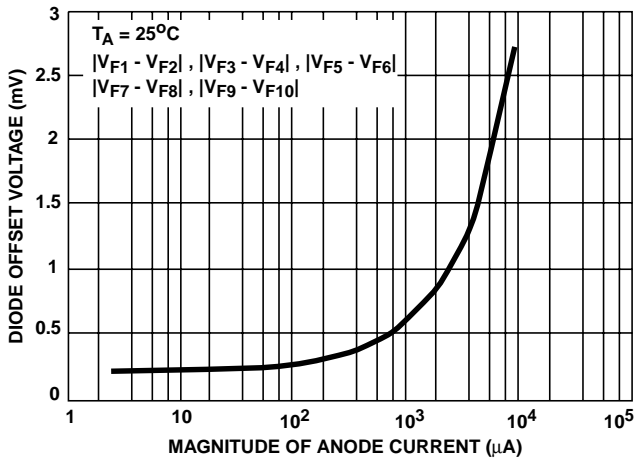


FIGURE 3. 3. DIODE OFFSET VOLTAGE vs MAGNITUDE OF ANODE CURRENT

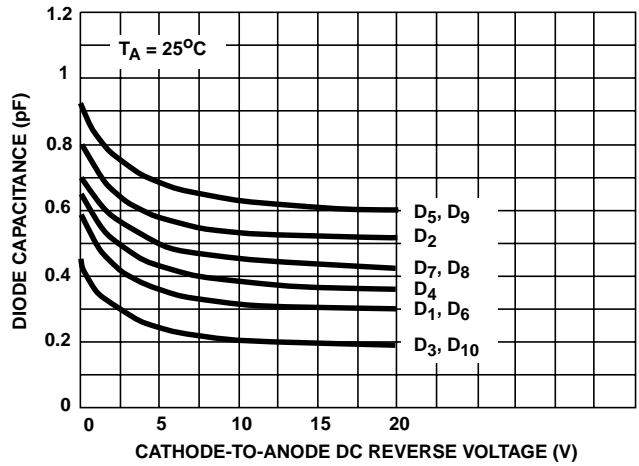


FIGURE 4. DIODE CAPACITANCE vs CATHODE-TO-ANODE REVERSE VOLTAGE

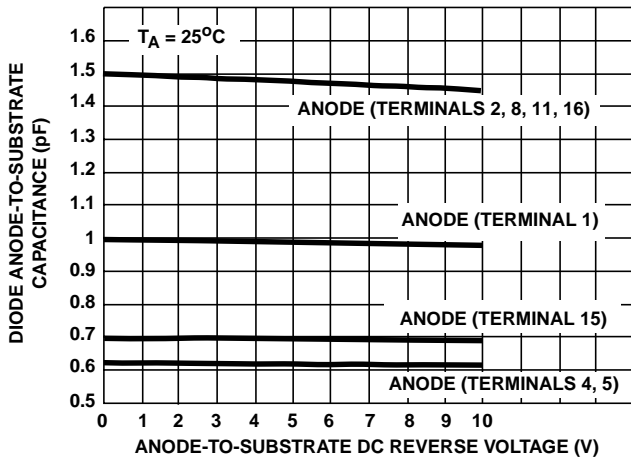


FIGURE 5. DIODE ANODE-TO-SUBSTRATE CAPACITANCE vs REVERSE VOLTAGE

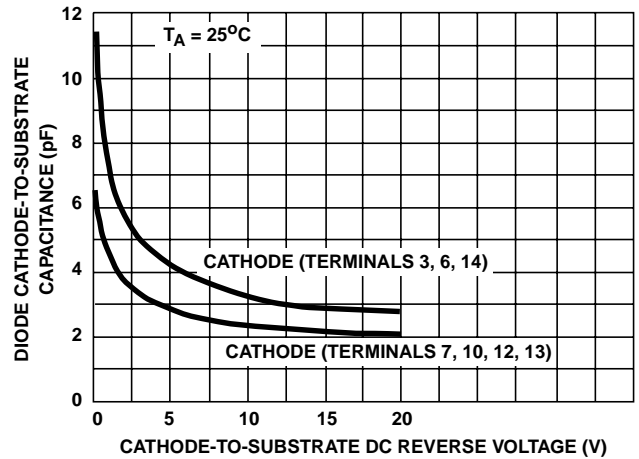


FIGURE 6. DIODE CATHODE-TO-SUBSTRATE CAPACITANCE vs CATHODE-TO-SUBSTRATE DC REVERSE VOLTAGE

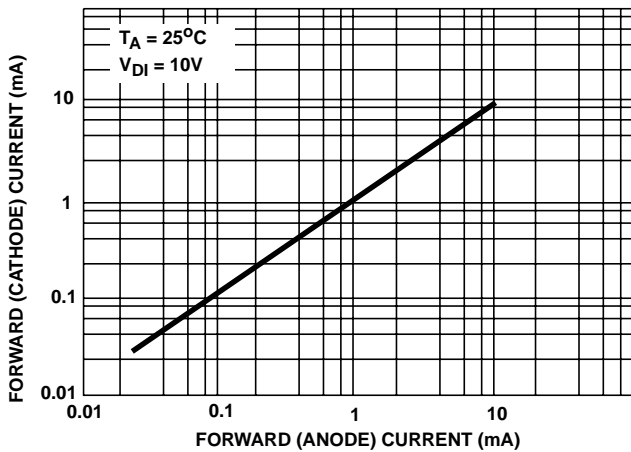


FIGURE 7. FORWARD (CATHODE) CURRENT vs FORWARD (ANODE) CURRENT

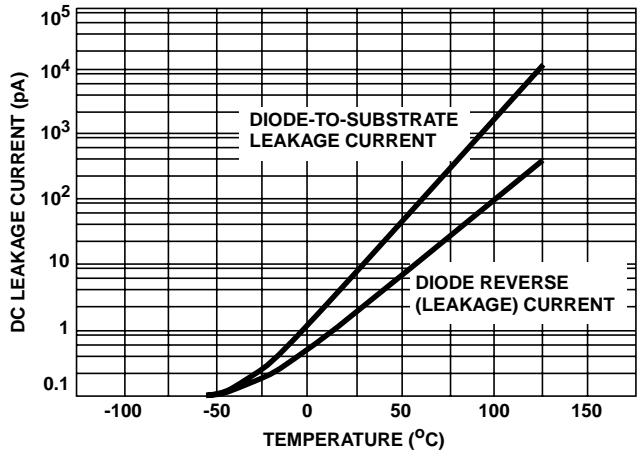
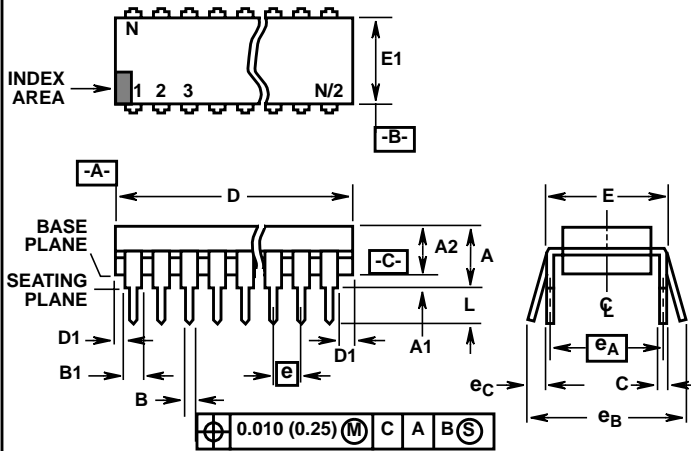


FIGURE 8. DC LEAKAGE CURRENT vs TEMPERATURE

CA3141

Dual-In-Line Plastic Packages (PDIP)



NOTES:

- Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- E and e_A are measured with the leads constrained to be perpendicular to datum $-C-$.
- e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
- B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- N is the maximum number of terminal positions.
- Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D) 16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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