HARRIS Semiconductor

CA3440

OBSOLETE PRODUCT
POSSIBLE SUBSTITUTE PRODUCT
ICL7611, ICL7612

January 1999

63kHz, Nanopower, BiMOS Operational Amplifiers

Features

- High Input Resistance . . . . . 2TΩ (Typ)
- Standby Power at V+ = 5V . . . . . 300nW (Typ)
- Supply Current, BW, Slew Rate Programmable Using External Resistor
- Input Current . . . . . 10pA (Typ)
- 5V to 15V Supply
- Output Drives Typical Bipolar Type Loads

Part Number Information

PART NUMBER (BRAND)	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
CA3440M (3440)	-55 to 125	8 Ld SOIC	M8.15

Description

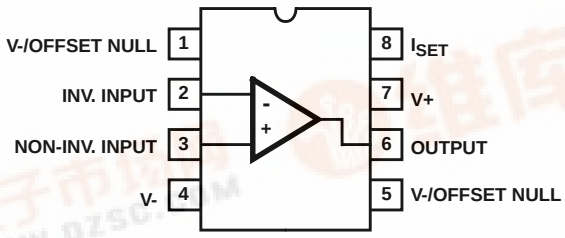
The CA3440 is an integrated circuit operational amplifier that combines the advantages of MOS and bipolar transistors on a single monolithic chip.

The CA3440 BiMOS op amp features gate protected PMOS transistors in the input circuit to provide very high input impedance, very low input currents (less than 10pA). This device operates at total supply voltages from 5V to 15V and can be operated over the temperature range from -55^{O}C to 125^{O}C. The virtues are programmability and very low standby power consumption (300nW). This operational amplifier is internally phase compensated to achieve stable operation in the unity gain follower configuration. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS in the input stage results in common mode input voltage capability down to 0.5V below the negative supply terminals, an important attribute for single supply applications. The output stage uses MOS complementary source follower form which permits moderate load driving capability (10kΩ) at very low standby currents (50nA).

The CA3440 has the same 8 lead pinout as the “741” and other industry standard op amps with two exceptions: terminals one and five must be connected to the negative supply or to a potentiometer if nulling is required. Terminal 8 must be programmed through an external resistor returned to the negative supply.

Pinout

CA3440
(SOIC)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage (V+ to V-) 25V
Differential Input Voltage. 9V
DC Input Voltage . . . . . (V+ +8V) to (V- -0.5V)
Input Current. 1mA
Output Short Circuit Duration (Note 1) . . . . . Indefinite

Operating Conditions

Temperature Range . . . . . -55^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
SOIC Package	165

Maximum Junction Temperature (Die) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Short circuit may be applied to ground or to either supply.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Typical Values Intended Only for Design Guidance, $V_{SUPPLY} = \pm5V$, $R_{SET} = 10M\Omega$, $T_A = 25^oC$

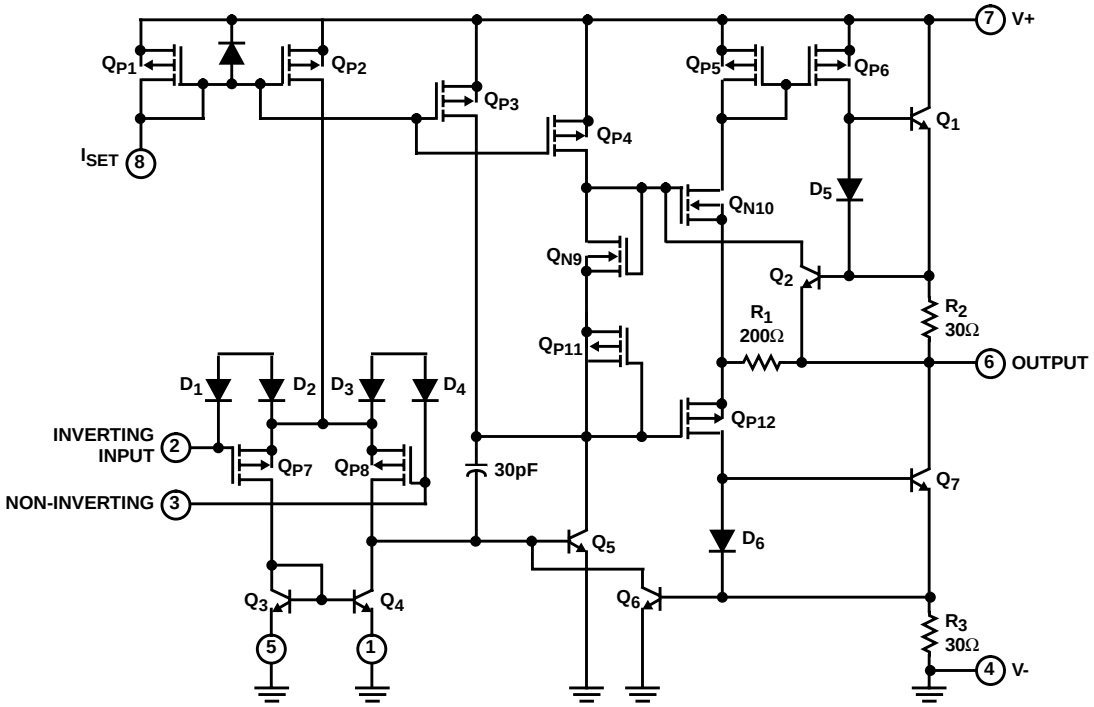
PARAMETER	SYMBOL	TEST CONDITIONS		CA3440	UNITS
Input Resistance	R_I			2	$T\Omega$
Input Capacitance	C_I			3.5	pF
Output Resistance	R_O			450	Ω
Equivalent Input Noise Voltage	e_N	f = 1kHz	$R_S = 100\Omega$	110	$nV/\sqrt{Hz}$
		f = 10kHz		110	$nV/\sqrt{Hz}$
Short-Circuit Current, Source	$I_{OM}+$			15	mA
To Opposite Supply, Sink	$I_{OM}-$			4.5	mA
Gain Bandwidth Product	f_T			63	kHz
Slew Rate	SR			0.03	V/µs
Transient Response, Rise Time	t_R	$R_L = 10k\Omega$, $C_L = 100pF$		5.6	µs
Overshoot	OS			10	%

Electrical Specifications

For Equipment Design, At $V_{SUPPLY} = \pm5V$; $R_{SET} = 10M\Omega$, $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA3440			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	$\|V_{IO}\|$		-	5	10	mV
Input Offset Current	$\| I_{IO} \|$		-	2.5	30	pA
Input Current	$\| I_I \|$		-	10	50	pA
Large Signal Voltage Gain	A_{OL}	$R_L = 10k\Omega$	10	100	-	kV/V
			80	100	-	dB
Common Mode Rejection Ratio	CMRR		-	100	320	µV/V
			70	80	-	dB
Common Mode Input Voltage Range	$V_{ICR}+$		+3.5	+3.7	-	V
	$V_{ICR}-$		-5.0	-5.3	-	V
Power Supply Rejection Ratio	PSRR		-	32	320	µV/V
			70	90	-	dB
Max Output Voltage	$V_{OM}+$		+3	+3.2	-	V
	$V_{OM}-$		-3	-3.2	-	V
Supply Current	I+		-	10	17	µA
Device Dissipation	P_D		-	100	170	µW
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$		-	4	-	$\mu V/^oC$

Schematic Diagram



Application Information

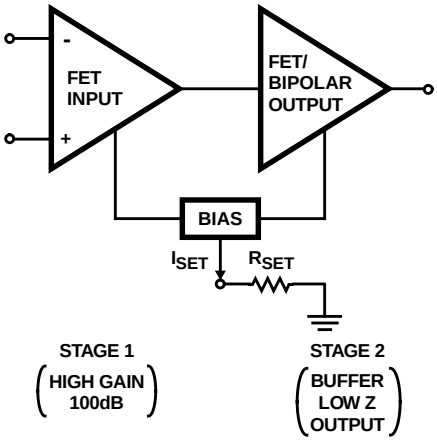


FIGURE 1. NANOPOWER OP AMP (SUPPLY CURRENT PROGRAMMABLE USING R_{SET}), 1pA TYPICAL INPUT BIAS CURRENT, 4.0V TO 15V SUPPLY

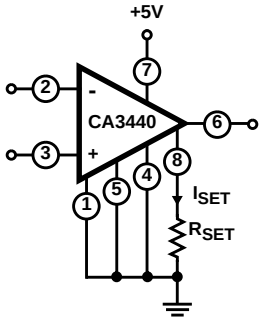


FIGURE 2. NANOPOWER OP AMP (USABLE STANDBY POWER vs PROGRAMMING RESISTOR R_{SET})

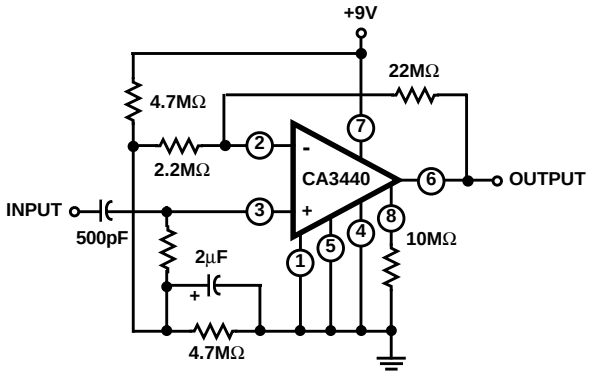
As R_{SET} is increased, I_{SET} and the standby power decrease while the BW/SR also decrease.

Operating at a +5V single supply, the CA3440 exhibits the following characteristics:

R_{SET}	STANDBY POWER	BW	SR
1MΩ	250µW	164kHz	0.17V/µs
10MΩ	25µW	27kHz	0.017V/µs
100MΩ	2.5µW	2.6kHz	0.0017V/µs
1GΩ	250nW	78kHz	0.00017V/µs

The CA3440 is pin compatible with the 741 except that pins 1 and 5 (typical negative nulling pins) must be connected either directly to pin 4 or to a negative nulling potentiometer. In addition, pin 8, the I_{SET} terminal, must be returned to either ground or -V via R_{SET}.

Typical Applications



R_{IN} >20MΩ
Standby Power = 90μW
Gain = 20dB
BW: 20Hz to 3kHz
SR = 0.016V/μs

FIGURE 3. HIGH INPUT IMPEDANCE AMPLIFIER

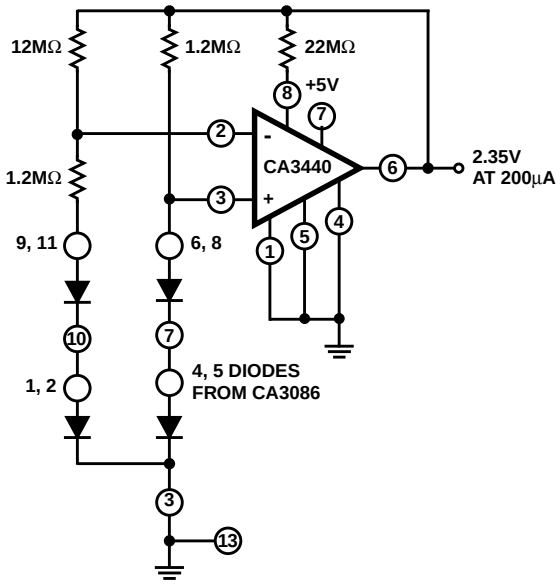


FIGURE 4. MICROPOWER BANDGAP REFERENCE

Typical Performance Curves

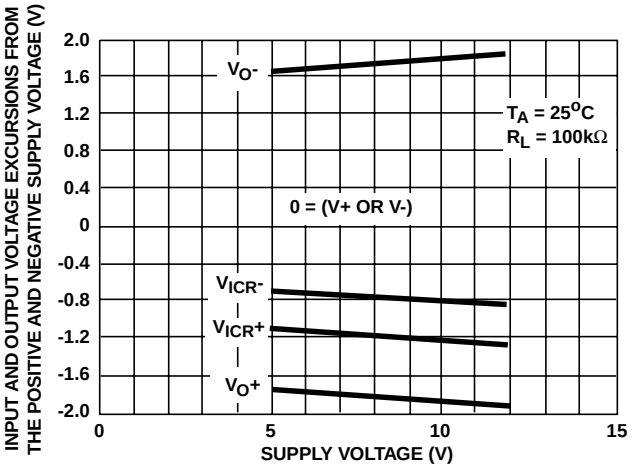


FIGURE 5. OUTPUT VOLTAGE SWING AND COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

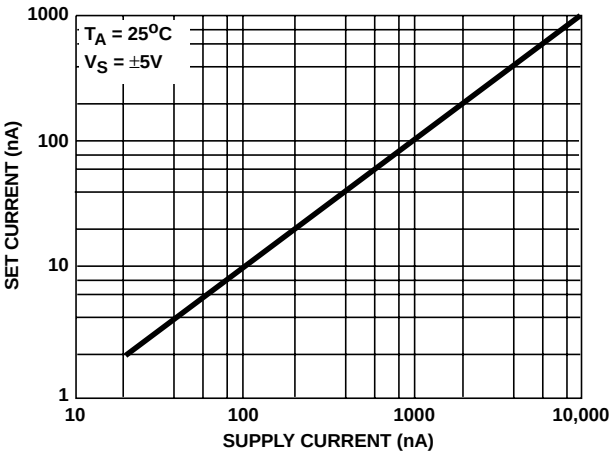


FIGURE 6. SET CURRENT vs SUPPLY CURRENT

Typical Performance Curves (Continued)

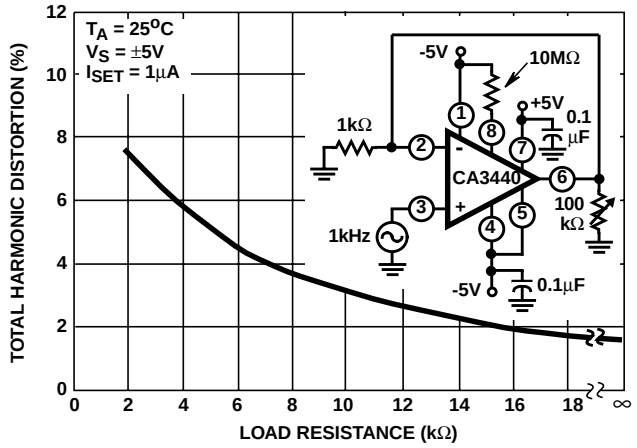


FIGURE 7. TOTAL HARMONIC DISTORTION vs LOAD RESISTANCE

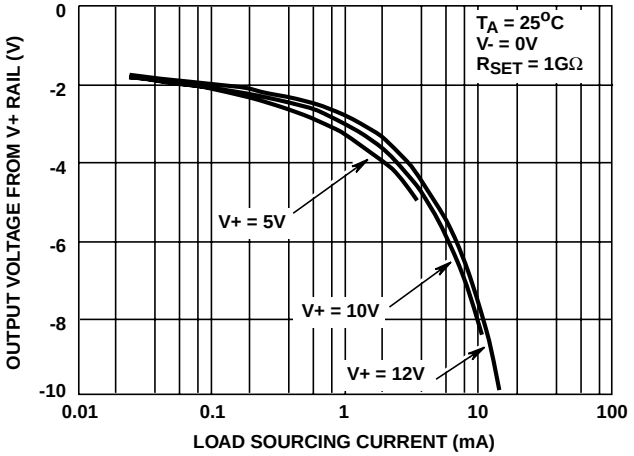


FIGURE 8. OUTPUT VOLTAGE vs SOURCING LOAD CURRENT

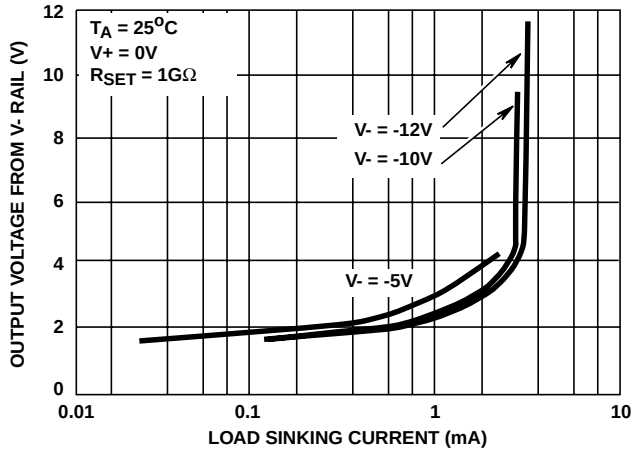


FIGURE 9. OUTPUT VOLTAGE vs SINKING LOAD CURRENT

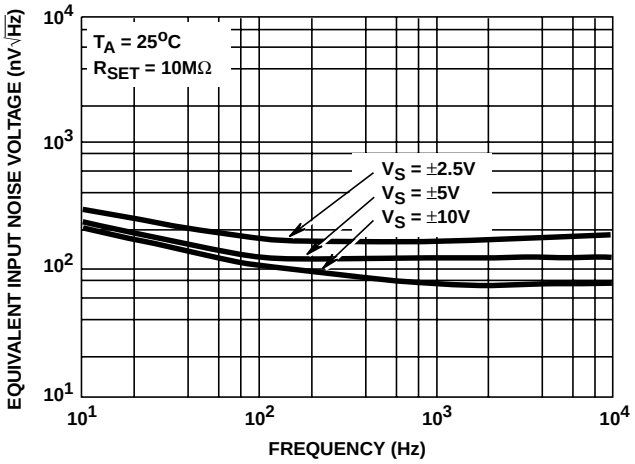


FIGURE 10. INPUT NOISE VOLTAGE vs FREQUENCY

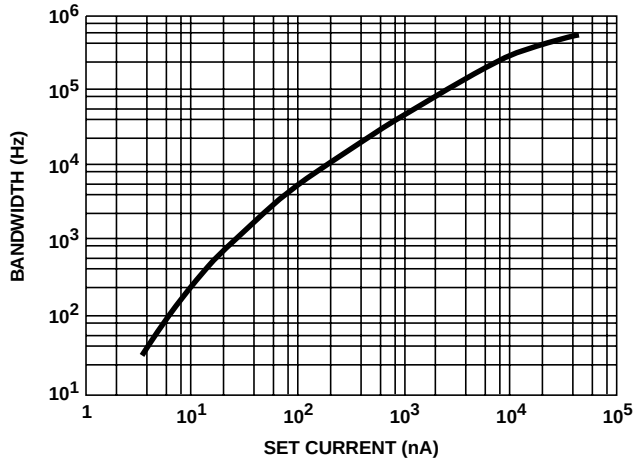


FIGURE 11. BANDWIDTH vs SET CURRENT

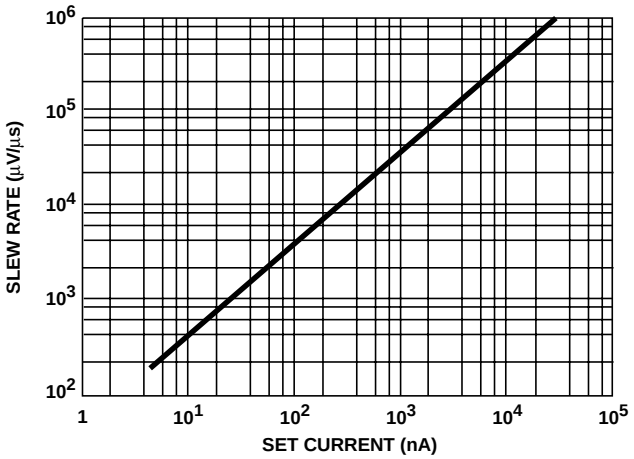


FIGURE 12. SLEW RATE vs SET CURRENT