intersil

# CA5470

## Quad, 14MHz, Microprocessor BiMOS-E Operational Amplifier with MOSFET Input/Bipolar Output

November 1996

### Features

- High Speed CMOS Input Stage Provides
  - Very High $Z_I$. . . . . 5TΩ (5 x $10^{12}$Ω) (Typ)
  - Very Low $I_I$. . . . . 0.5pA (Typ) at 5V Operation
  - Very Low $I_{IO}$ . . . . . 0.5pA (Typ) at 5V Operation
- ESD Protection to 2000V
- 3V to 16V Power Supply Operation
- Fully Guaranteed Specifications Over Full Military Range
- Wide BW (14MHz); High SR (5V/μs) at 5V Supply
- Wide $V_{ICR}$ Range From -0.5V to 3.7V (Typ) at 5V Supply
- Ideally Suited for CMOS and HCMOS Applications

### Applications

- Bar Code Readers
- Photodiode Amplifiers (IR)
- Microprocessor Buffering
- Ground Reference Single Supply Amplifiers
- Fast Sample and Hold
- Timers
- Voltage Controlled Oscillators
- Voltage Followers
- V to I Converters
- Peak Detectors
- Precision Rectifiers
- 5V Logic Systems
- 3V Logic Systems

### Description

The CA5470 is an operational amplifier that combines the advantages of both high speed CMOS and bipolar transistors on a single monolithic chip. It is constructed in the BiMOS-E process which adds drain-extension implants to 3μm polygate CMOS, enhancing both the voltage capability and providing vertical bipolar transistors for broadband analog/digital functions. This process lends itself easily to high speed operational amplifiers, comparators, analog switches and interface peripherals, resulting in twice the speed of the conventional CMOS transistors having similar feature size.

BiMOS-E are broadbased bipolar transistors that have high transconductance, gains more constant with current level, stable “precision” base-emitter offset voltages and superior drive capability. Excellent interface with environmental potentials enable use in 5V logic systems and future 3.3V logic systems. Refer to Application Note AN8811.

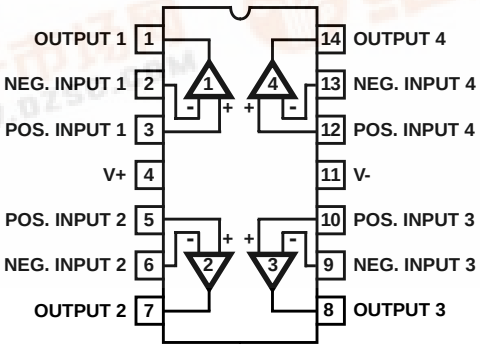
ESD capability exceeds the standard 2000V level. The CA5470 series can operate with single supply voltages from 3V to 16V or ±1.5V to ±8V. They have guaranteed specifications at both 5V and ±7.5V at room temperature as well as over the full -55°C to 125°C military range.

### Ordering Information

| PART NUMBER (BRAND) | TEMP. RANGE (°C) | PACKAGE | PKG. NO. |
|---|---|---|---|
| CA5470E | -55 to 125 | 14 Ld PDIP | E14.3 |
| CA5470M (5470) | -55 to 125 | 14 Ld SOIC | M14.15 |
| CA5470M96 (5470) | -55 to 125 | 14 Ld SOIC Tape and Reel | M14.15 |

### Pinout

**CA5470 (PDIP, SOIC)**
TOP VIEW



## Absolute Maximum Ratings

DC Supply Voltage (Between V+ And V- Terminals) . . . . . 16V
Differential Input Voltage. . . . . 8V
Input Voltage. . . . . (V+ +8V) to (V- -0.5V)
Input Current. . . . . 1mA
Output Short Circuit Duration (Note 1) . . . . . Indefinite

## Operating Conditions

Temperature Range . . . . . $-55^oC$ to $125^oC$

## Thermal Information

| Thermal Resistance (Typical, Note 1) | $\theta_{JA}$ ($^oC/W$) |
|---|---|
| PDIP Package | 80 |
| SOIC Package | 175 |

Maximum Junction Temperature (Die). . . . . $175^oC$
Maximum Junction Temperature (Plastic Package) . . . . . $150^oC$
Maximum Storage Temperature Range . . . . . $-65^oC$ to $150^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^oC$
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

1. Short circuit may be applied to ground or to either supply.
2. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications

Typical Values Intended Only for Design Guidance at V+ = 5V, V- = 0V, $T_A = 25^oC$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | TYPICAL VALUES | UNITS |
|---|---|---|---|---|
| Input Resistance | $R_I$ | | 5 | TΩ |
| Input Capacitance | $C_I$ | f = 1MHz | 3.1 | pF |
| Unity Gain Crossover Frequency | $f_T$ | | 14 | MHz |
| Slew Rate | SR | $V_{OUT} = 3.65V_{P-P}$ | 5 | V/µs |
| Transient Response: | | $C_L$ = 25pF, $R_L$= 2kΩ (Voltage Follower) | | |
| Rise Time/Fall Time | $t_r$ | | 27/25 | ns |
| Overshoot | OS | | 20 | % |
| Settling Time (To <0.1%, $V_{IN} = 4V_{P-P}$) | $t_S$ | $C_L$ = 25pF, $R_L$= 2kΩ (Voltage Follower) | 1 | µs |
| Full Power BW, SR = 5V/µs | FPBW | $A_V$ = 1, $V_{OUT} = 3.65V_{P-P}$ | 436 | kHz |

## Electrical Specifications

$T_A = 25^oC$, V+ = 5V, V- = GND

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input Offset Voltage | $\lvert V_{IO} \rvert$ | | - | 6 | 22 | mV |
| Input Offset Current | $\lvert I_{IO} \rvert$ | | - | 0.5 | 50 (Note 3) | pA |
| Input Current | $I_I$ | | - | 0.5 | 50 (Note 3) | pA |
| Common Mode Input Range | $V_{ICR}$ | | 3.5 | -0.5 to 3.7 | 0 | V |
| Common Mode Rejection Ratio | CMRR | $V_{ICR}$ = 0V to 3.5V | 55 | 70 | - | dB |
| Power Supply Rejection Ratio | PSRR | ΔV = 2V | 60 | 75 | - | dB |
| Positive Output Voltage Swing | $V_{OM}+$ | $R_L$ = 2kΩ to GND | 4 | 4.4 | - | V |
| Negative Output Voltage Swing | $V_{OM}-$ | $R_L$ = 2kΩ to GND | - | 0.06 | 0.10 | V |
| Total Supply Current | $I_{SUPPLY}$ | $V_{OUT}$ = 2.5V, $R_L = \infty$ | - | 6 | 7 | mA |
| Unity Gain Bandwidth Product | $f_T$ | | 10 | 14 | - | MHz |
| Slew Rate | SR | | 4 | 5 | - | V/µs |
| Output Current | | | | | | |
| Source to opposite supply | $I_{SOURCE}$ | | 4 | 5.5 | - | mA |
| Sink to opposite supply | $I_{SINK}$ | | 1.0 | 1.2 | - | mA |
| Open Loop Gain | $A_{OL}$ | 0.5V to 3.5V, $R_L$ = 10kΩ | 80 | 90 | - | dB |

NOTE:

3. This is the lowest value that can be tested reliably. Almost all devices will be <10pA.

**Electrical Specifications** $T_A = -55^oC$ to $125^oC$, V+ = 5V, V- = GND

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input Offset Voltage | $\|V_{IO}\|$ | | - | 6 | 25 | mV |
| Input Offset Current | $\|I_{IO}\|$ | | - | 550 | 5500 | pA |
| Input Current | $I_I$ | | - | 550 | 11000 | pA |
| Common Mode Input Range | $V_{ICR}$ | | 3.5 | -0.5 to 3.7 | 0 | V |
| Common Mode Rejection Ratio | CMRR | $V_{ICR}$ = 0V to 3.5V | 50 | 65 | - | dB |
| Power Supply Rejection Ratio | PSRR | $\Delta V$ = 2V | 58 | 75 | - | dB |
| Positive Output Voltage Swing | $V_{OM}+$ | $R_L$ = 2kΩ to GND | 3.8 | 4.2 | - | V |
| Negative Output Voltage Swing | $V_{OM}-$ | $R_L$ = 2kΩ to GND | - | 0.08 | 0.11 | V |
| Total Supply Current | $I_{SUPPLY}$ | $V_{OUT}$ = 2.5V | - | 9 | 11 | mA |
| Unity Gain Bandwidth Product | $f_T$ | | 8 | 12 | - | MHz |
| Slew Rate | SR | | 3 | 5 | - | V/µs |
| Output Current | | | | | | |
| Source to opposite supply | $I_{SOURCE}$ | | 4 | 5.5 | - | mA |
| Sink to opposite supply | $I_{SINK}$ | | 0.8 | 1.2 | - | mA |
| Open Loop Gain | $A_{OL}$ | 0.5V to 3.5V, $R_L$ = 10kΩ | 80 | 90 | - | dB |

**Electrical Specifications** $T_A = 25^oC$, $V_{SUPPLY} = \pm 7.5V$

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input Offset Voltage | $\|V_{IO}\|$ | | - | 5 | 25 | mV |
| Input Offset Current | $\|I_{IO}\|$ | | - | 0.5 | 50 (Note 4) | pA |
| Input Current | $I_I$ | | - | 1 | 50 (Note 4) | pA |
| Common Mode Input Range | $V_{ICR}$ | | 5.8 | -7.8 to 6.0 | -7.5 | V |
| Common Mode Rejection Ratio | CMRR | $V_{ICR}$ = 0V to 13.3V | 60 | 70 | - | dB |
| Power Supply Rejection Ratio | PSRR | $\Delta V$ = 1V | 60 | 76 | - | dB |
| Positive Output Voltage Swing | $V_{OM}+$ | | | | | |
| | | $R_L$ = 2kΩ to GND | 6.3 | 6.5 | - | V |
| | | $R_L$ = 10kΩ to GND | 6.4 | 6.6 | - | V |
| Negative Output Voltage Swing | $V_{OM}-$ | | | | | |
| | | $R_L$ = 2kΩ to GND | - | -2.6 | -2 | V |
| | | $R_L$ = 10kΩ to GND | - | -7.3 | -7.1 | V |
| Total Supply Current | $I_{SUPPLY}$ | $V_{OUT}$ = GND, $R_L$ = ∞ | - | 10 | 12 | mA |
| Unity Gain Bandwidth Product | $f_T$ | | 12 | 16 | - | MHz |
| Slew Rate | SR | | 4 | 7 | - | V/µs |
| Output Current | | | | | | |
| Source to opposite supply | $I_{SOURCE}$ | | 6.2 | 6.8 | - | mA |
| Sink to opposite supply | $I_{SINK}$ | | 1 | 1.4 | - | mA |
| Open Loop Gain | $A_{OL}$ | -5V to +5V, $R_L$ = 10kΩ | 80 | 90 | - | dB |

NOTE:

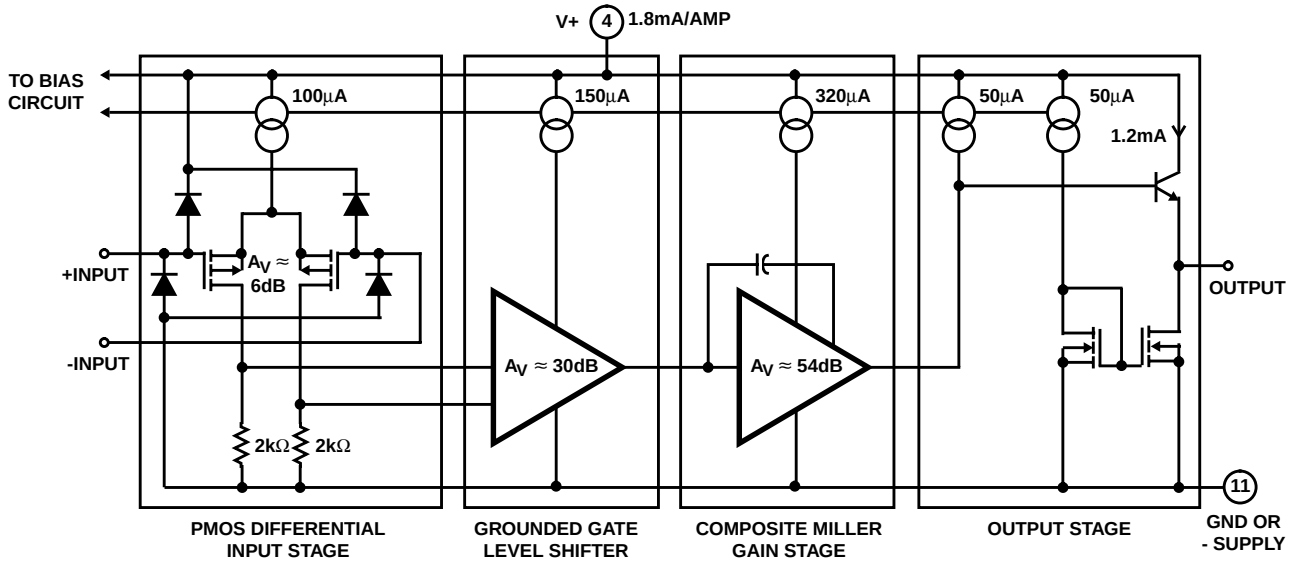
4. This is the lowest value that can be tested reliably. Almost all devices will be <10pA.

## Electrical Specifications

$T_A$ = -55°C to 125°C, $V_{SUPPLY}$ = ±7.5V

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input Offset Voltage | $\|V_{IO}\|$ | | - | 5 | 30 | mV |
| Input Offset Current | $\|I_{IO}\|$ | | - | 550 | 5500 | pA |
| Input Current | $I_I$ | | - | 1100 | 11000 | pA |
| Common Mode Input Range | $V_{ICR}$ | | 5.8 | -7.8 to 6.0 | -7.5 | V |
| Common Mode Rejection Ratio | CMRR | $V_{ICR}$ = 0V to 3.5V | 58 | 70 | - | dB |
| Power Supply Rejection Ratio | PSRR | ΔV = 1V | 60 | 76 | - | dB |
| Positive Output Voltage Swing | $V_{OM}+$ | | | | | |
| | | $R_L$ = 2kΩ to GND | 4.75 | 5.5 | - | V |
| | | $R_L$ = 10kΩ to GND | 6.1 | 6.4 | - | V |
| Negative Output Voltage Swing | $V_{OM}-$ | | | | | |
| | | $R_L$ = 2kΩ to GND | - | -2.6 | -2 | V |
| | | $R_L$ = 10kΩ to GND | - | -7.3 | -7.1 | V |
| Total Supply Current | $I_{SUPPLY}$ | $V_{OUT}$ = GND, $R_L$ = ∞ | - | 12 | 18 | mA |
| Unity Gain Bandwidth Product | $f_T$ | | 10 | 15 | - | MHz |
| Slew Rate | SR | | 3 | 7 | - | V/µs |
| Output Current | | | | | | |
| Source to opposite supply | $I_{SOURCE}$ | | 6.2 | 6.8 | - | mA |
| Sink to opposite supply | $I_{SINK}$ | | 1 | 1.4 | - | mA |
| Open Loop Gain | $A_{OL}$ | -5V to +5V, $R_L$ = 10kΩ | 80 | 90 | - | dB |

## *Block Diagram* ($^1/_4$ of CA5470)



## Typical Performance Curve

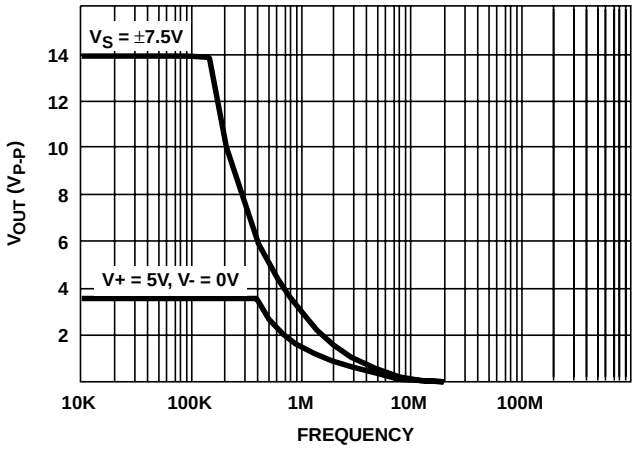



**FIGURE 1. MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY**

## Metallization Mask Layout

Dimensions in parentheses are in millimeters and derived from the basic inch dimensions as indicated. Grid graduations are in mils ($10^{-3}$ inch).

The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are $57^{o}$ instead of $90^{o}$ with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.