HARRIS SEMICONDUCTOR

CA723, CA723C

Voltage Regulators Adjustable from 2V to 37V at Output Currents Up to 150mA Without External Pass Transistors

April 1994

Features

- Up to 150mA Output Current
- Positive and Negative Voltage Regulation
- Regulation in Excess of 10A with Suitable Pass Transistors
- Input and Output Short-Circuit Protection
- Load and Line Regulation 0.03%
- Direct Replacement for 723 and 723C Industry Types
- Adjustable Output Voltage . . . . . 2V to 37V

Applications

- Series and Shunt Voltage Regulator
- Floating Regulator
- Switching Voltage Regulator
- High-Current Voltage Regulator
- Temperature Controller

Ordering Information

PART	TEMPERATURE	PACKAGE
CA723E	-55°C to +125°C	14Lead Plastic DIP
CA723T	-55°C to +125°C	10 Pin Metal Can
CA723CE	0°C to +70°C	14 Lead Plastic DIP
CA723CT	0°C to +70°C	10 Pin Metal Can

Description

The CA723 and CA723C are silicon monolithic integrated circuits designed for service as voltage regulators at output voltages ranging from 2V to 37V at currents up to 150mA.

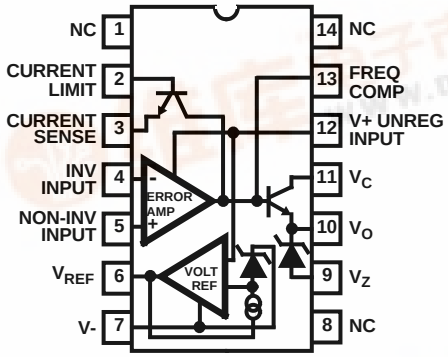
Each type includes a temperature-compensated reference amplifier, an error amplifier, a power series pass transistor, and a current-limiting circuit. They also provide independently accessible inputs for adjustable current limiting and remote shutdown and, in addition, feature low standby current drain, low temperature drift, and high ripple rejection.

The CA723 and CA723C may be used with positive and negative power supplies in a wide variety of series, shunt, switching, and floating regulator applications. They can provide regulation at load currents greater than 150mA and in excess of 10A with the use of suitable n-p-n or p-n-p external pass transistors.

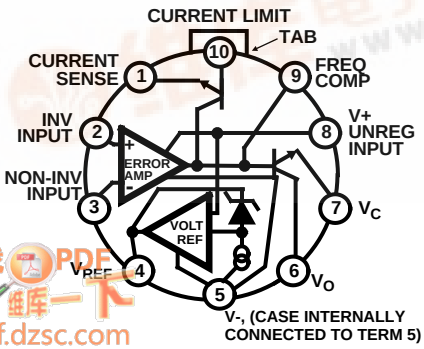
The CA723 and CA723C are supplied in the 10 lead TO-100 metal can(T suffix), and the 14 lead dual-in-line plastic package (E suffix), and are direct replacements for industry types LM723, LM723C in packages with similar terminal arrangements.

Pinouts

CA723 (PDIP)
TOP VIEW

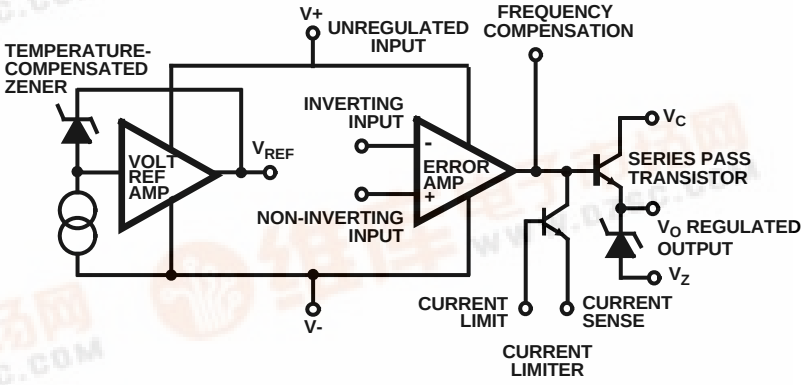


CA723C (CAN)
TOP VIEW



V-, (CASE INTERNALLY CONNECTED TO TERM 5)

Functional Block Diagram



Specifications CA723, CA723C

Absolute Maximum Ratings

DC Supply Voltage 40V
(Between V+ and V- Terminals)
Pulse Voltage for 50ms
Pulse Width (Between V+ and V- Terminals) 50V
Differential Input-Output Voltage 40V
Differential Input Voltage
Between Inverting and Noninverting Inputs . . . . . ±5V
Between Noninverting Input and V- 8V
Current From Zener Diode Terminal (V_Z) 25mA

Operating Conditions

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic DIP Package	$120^oC/W$	-
Metal Can	$136^oC/W$	$65^oC/W$

Device Dissipation
CA723T, CA723CT, Up to $T_A = +25^oC$ 900mW
CA723E, CA723CE, Up to $T_A = +25^oC$ 1000mW
CA723T, CA723CT, Above $T_A = +25^oC$ . . . . . $7.4mW/^oC$
CA723E, CA723CE, Above $T_A = +25^oC$ . . . . . $8.3mW/^oC$
Ambient Temperature Range
Operating Temperature Range . . . . . -55^oC to $+125^oC$
Storage Temperature Range . . . . . -65^oC to $+150^oC$
Lead Temperature, During Soldering . . . . . $+265^oC$
At a distance 1/16" ± 1/32" (1.59mm ± 0.79mm) from case for 10s max

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

$T_A = +25^oC$, $V+ = V_C = V_I = 12V$, $V- = 0$, $V_O = 5V$, $I_L = 1mA$, $C_1 = 100pF$, $C_{REF} = 0$, $R_{SCP} = 0$, Unless Otherwise Specified. Divider impedance $R_1 R_2 \div R_1 + R_2$ at noninverting input, Terminal 5 = 10kΩ. (Figure 20)

PARAMETERS	TEST CONDITION	CA723			CA723C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DC CHARACTERISTICS								
Quiescent Regulator Current, I_Q	$I_L = 0$, $V_I = 30V$	-	2.3	3.5	-	2.3	4	mA
Input Voltage Range, V_I		9.5	-	40	9.5	-	40	V
Output Voltage Range, V_O		2	-	37	2	-	37	V
Differential Input-Output Voltage, $V_I - V_O$		3	-	38	3	-	38	V
Reference Voltage, V_{REF}		6.95	7.15	7.35	6.8	7.15	7.5	V
Line Regulation (Note 1)	$V_I = 12V$ to 40V	-	0.02	0.2	-	0.1	0.5	% V_O
	$V_I = 12V$ to 15V	-	0.01	0.1	-	0.01	0.1	% V_O
	$V_I = 12V$ to 15V, $T_A = -55^oC$ to $+125^oC$	-	-	0.3	-	-	-	% V_O
	$V_I = 12V$ to 15V, $T_A = 0^oC$ to $+70^oC$	-	-	-	-	-	0.3	% V_O
Load Regulation (Note 1)	$I_L = 1mA$ to 50mA	-	0.03	0.15	-	0.03	0.2	% V_O
	$I_L = 1mA$ to 50mA, $T_A = -55^oC$ to $+125^oC$	-	-	0.6	-	-	-	% V_O
	$I_L = 1mA$ to 50mA, $T_A = 0^oC$ to $+70^oC$	-	-	-	-	-	0.6	% V_O
Output-Voltage Temperature Coefficient, ΔV_O	$T_A = -55^oC$ to $+125^oC$	-	0.002	0.015	-	-	-	$\%/^oC$
	$T_A = 0^oC$ to $+70^oC$	-	-	-	-	0.003	0.015	$\%/^oC$
Ripple Rejection (Note 2)	f = 50Hz to 10kHz	-	74	-	-	74	-	dB
	f = 50Hz to 10kHz, $C_{REF} = 5\mu F$	-	86	-	-	86	-	dB
Short Circuit Limiting Current, I_{LIM}	$R_{SCP} = 10\Omega$, $V_O = 0$	-	65	-	-	65	-	mA
Equivalent Noise RMS Output Voltage, V_N (Note 2)	BW = 100Hz to 10kHz, $C_{REF} = 0$	-	-20	-	-	20	-	µV
	BW = 100Hz to 10kHz, $C_{REF} = 5\mu F$	-	2.5	-	-	2.5	-	µV

NOTES:

1. Line and load regulation specifications are given for condition of a constant chip temperature. For high dissipation condition, temperature drifts must be separately taken into account.
2. For C_{REF} (See Figure 20)

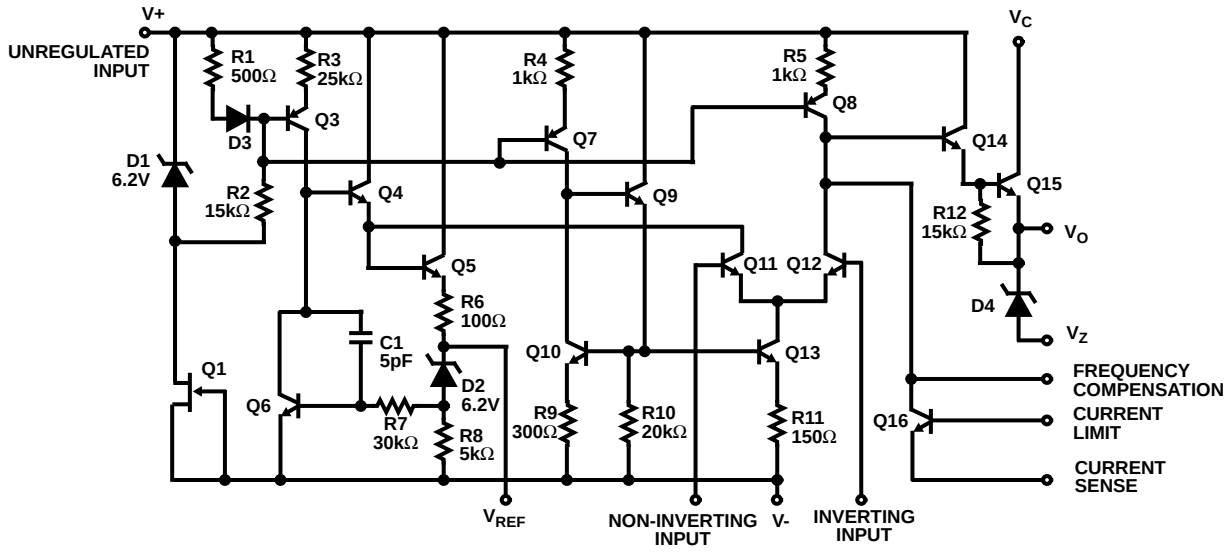


FIGURE 1. EQUIVALENT SCHEMATIC DIAGRAM OF THE CA723 AND CA723C

Typical Performance Curves (CA723)

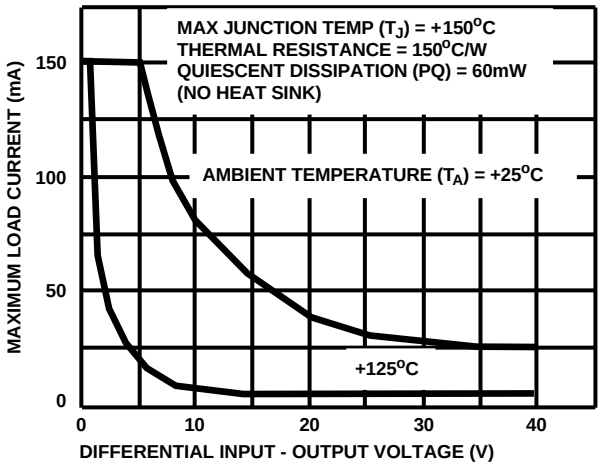


FIGURE 2. MAX LOAD CURRENT vs DIFFERENTIAL INPUT-OUTPUT VOLTAGE

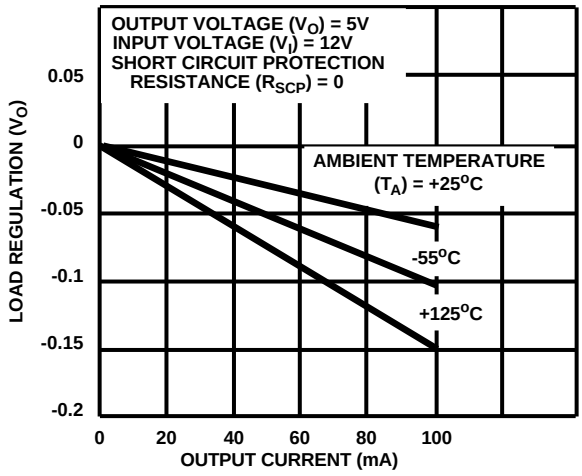


FIGURE 3. LOAD REGULATION WITHOUT CURRENT LIMITING

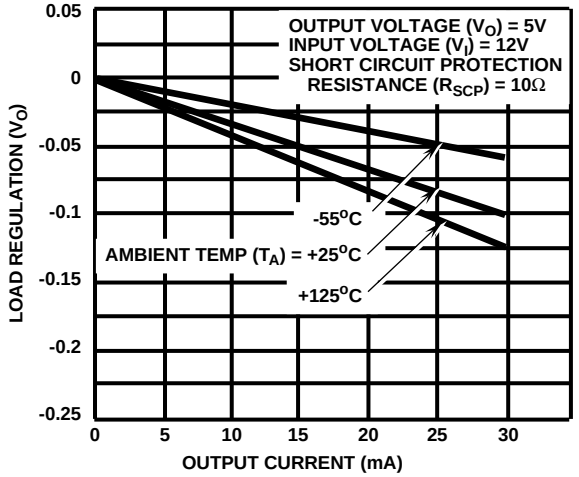


FIGURE 4. LOAD REGULATION WITH CURRENT LIMITING

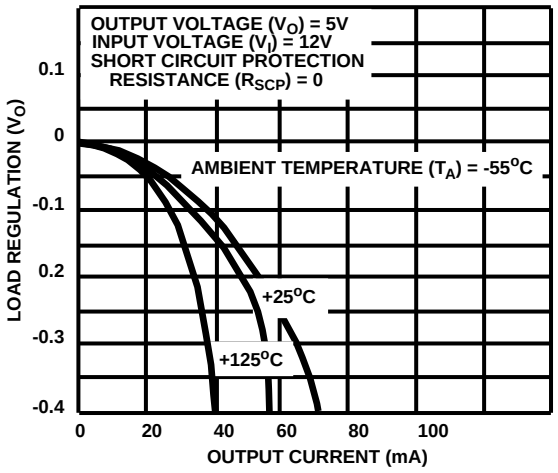


FIGURE 5. LOAD REGULATION WITH CURRENT LIMITING

Typical Performance Curves (CA723) (Continued)

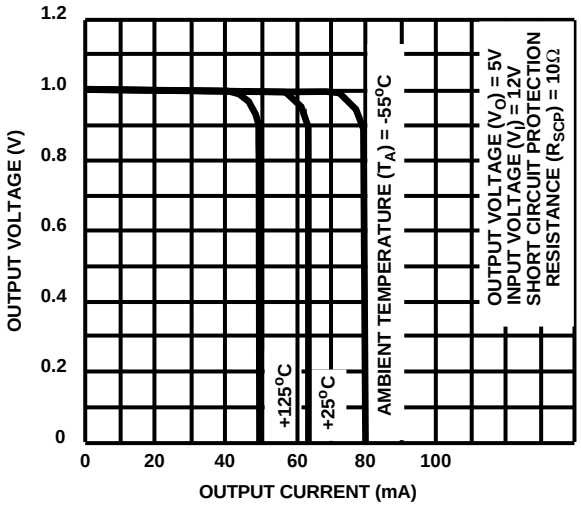


FIGURE 6. CURRENT LIMITING CHARACTERISTICS

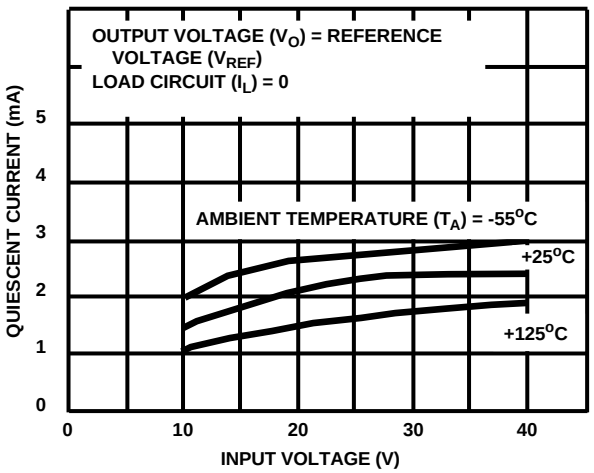


FIGURE 7. QUIESCENT CURRENT vs INPUT VOLTAGE

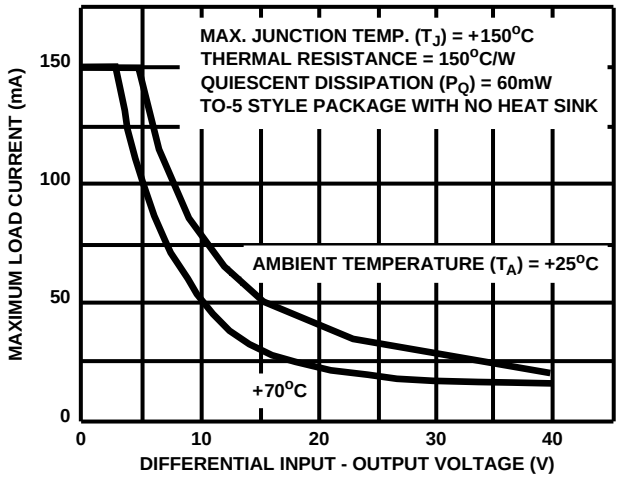


FIGURE 8. MAX LOAD CURRENT vs DIFFERENTIAL INPUT-OUTPUT VOLTAGE

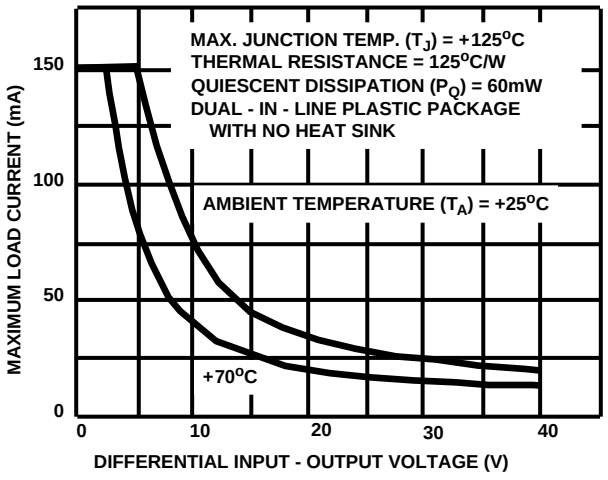


FIGURE 9. MAX LOAD CURRENT vs DIFFERENTIAL INPUT-OUTPUT VOLTAGE FOR CA723CE

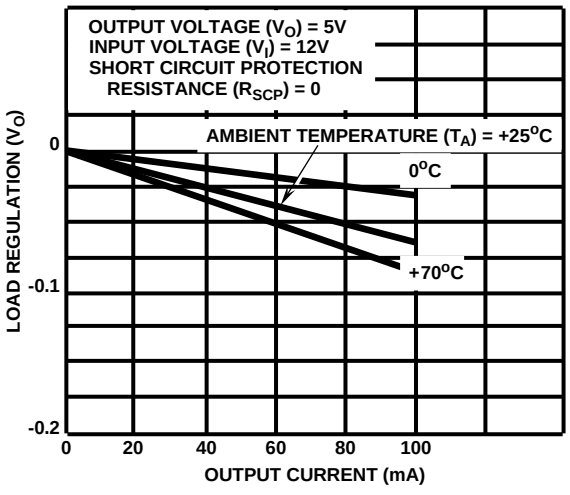


FIGURE 10. LOAD REGULATION WITHOUT CURRENT LIMITING

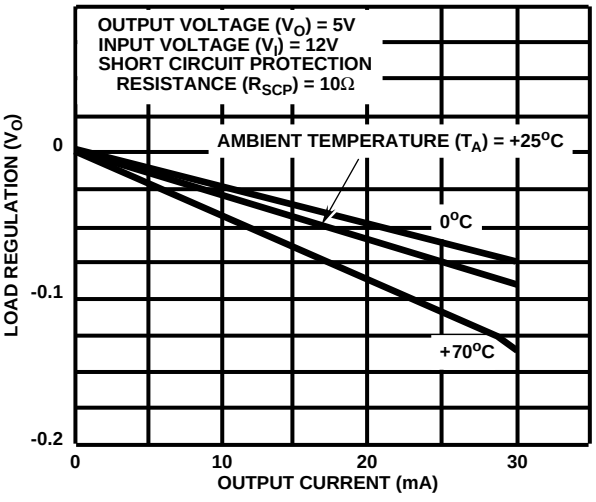


FIGURE 11. LOAD REGULATION WITH CURRENT LIMITING

Typical Performance Curves (CA723) (Continued)

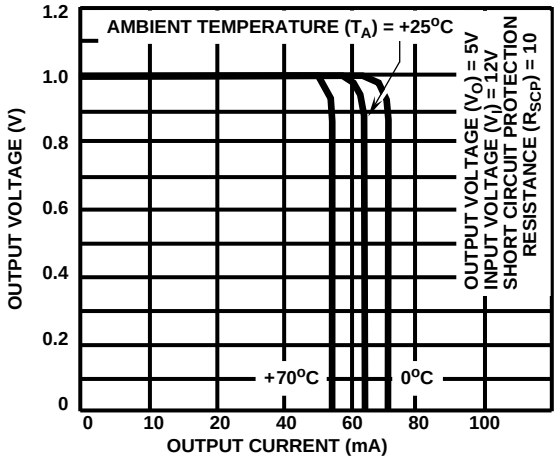


FIGURE 12. CURRENT LIMITING CHARACTERISTICS

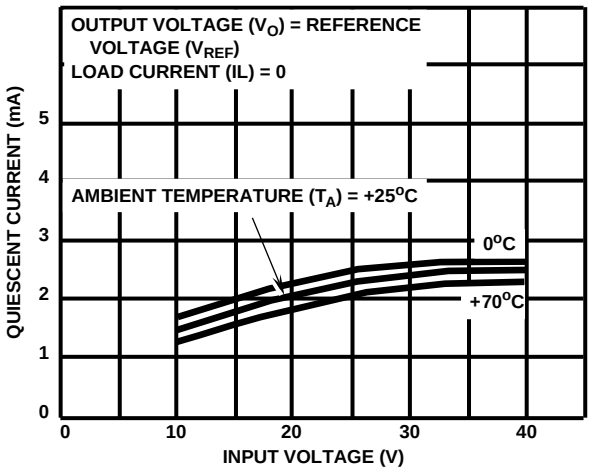


FIGURE 13. QUIESCENT CURRENT vs INPUT VOLTAGE

Typical Performance Curves (CA723 and CA723C)

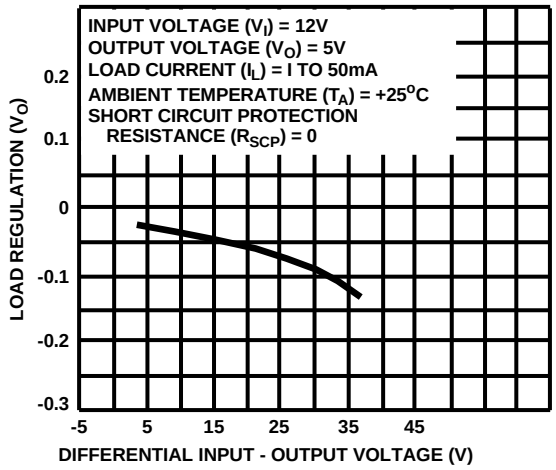


FIGURE 14. LOAD REGULATION vs DIFFERENTIAL INPUT-OUTPUT VOLTAGE

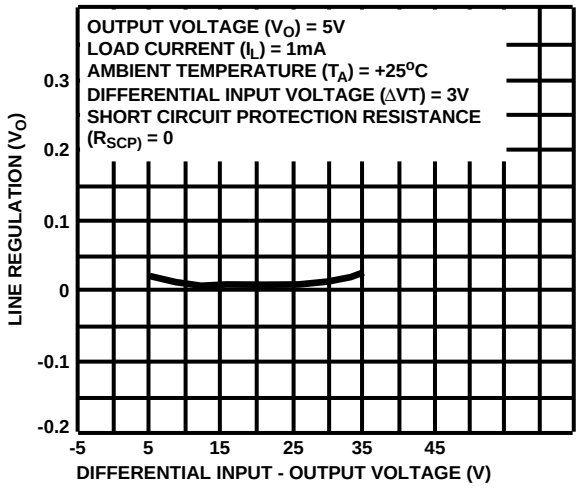


FIGURE 15. LINE REGULATION vs DIFFERENTIAL INPUT-OUTPUT VOLTAGE

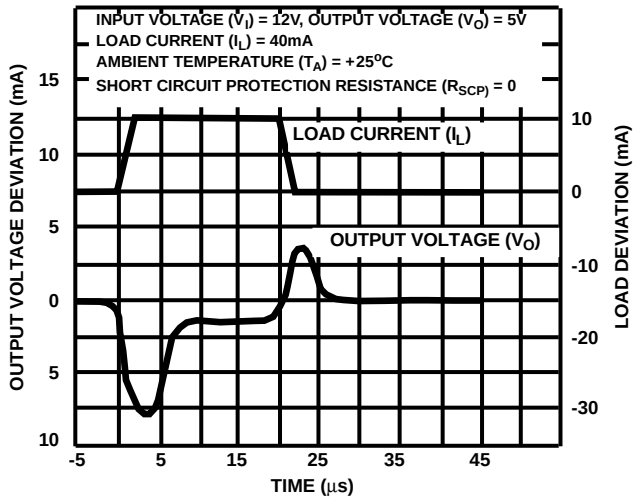


FIGURE 16. LINE TRANSIENT RESPONSE

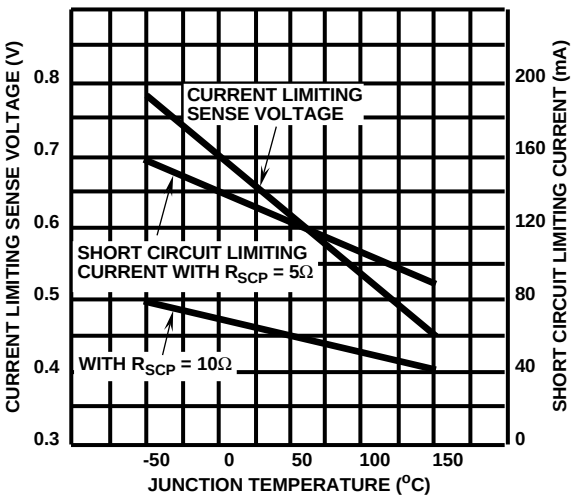


FIGURE 17. CURRENT LIMITING CHARACTERISTIC vs JUNCTION TEMPERATURE

Typical Performance Curves (CA723 and CA723C) (Continued)

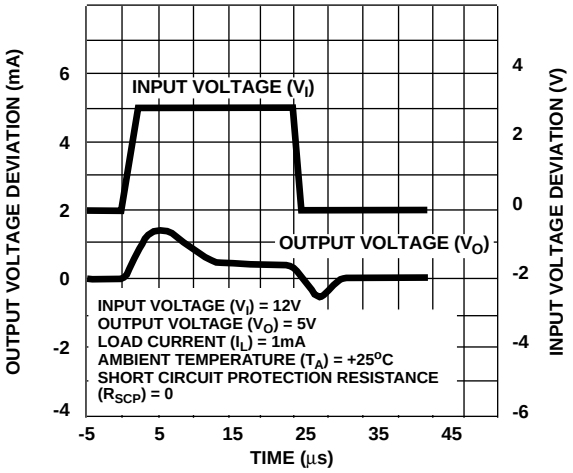


FIGURE 18. LOAD TRANSIENT RESPONSE

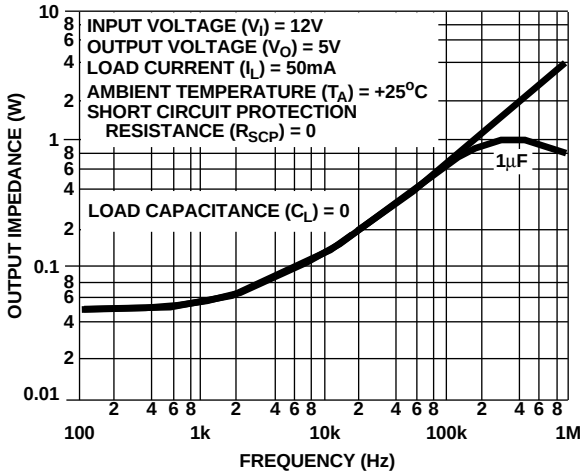
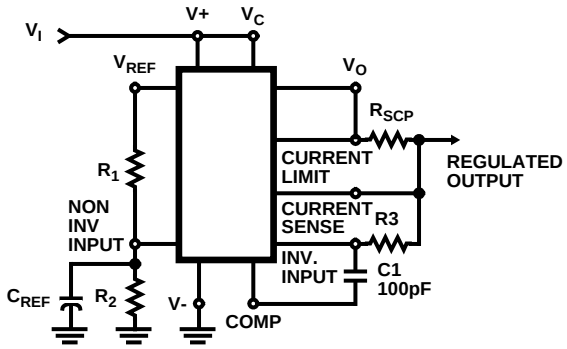


FIGURE 19. OUTPUT IMPEDANCE vs FREQUENCY

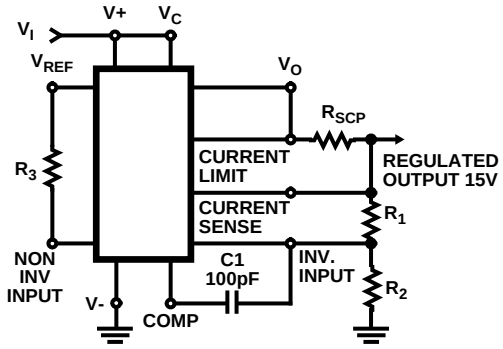
Typical Application Circuits



Circuit Performance Data:
Regulated Output Voltage 5V
Line Regulation (ΔV_I= 3V) 0.5mV
Load Regulation (ΔI_L = 50mA) 1.5mV

Note: R3 = $\frac{R1\ R2}{R1 + R2}$ For Minimum Temperature Drift

FIGURE 20. LOW VOLTAGE REGULATOR CIRCUIT (V_O = 2V TO 7V)

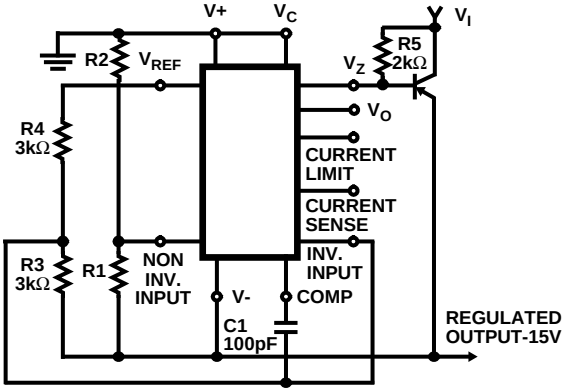


Circuit Performance Data:
Line Regulation (ΔV_I = 3V) 1.5mV
Load Regulation (ΔI_L = 50mA) 4.5mV

Note: R3 = $\frac{R1\ R2}{R1 + R2}$ For Minimum Temperature Drift
R3 May Be Eliminated For Minimum Component Count

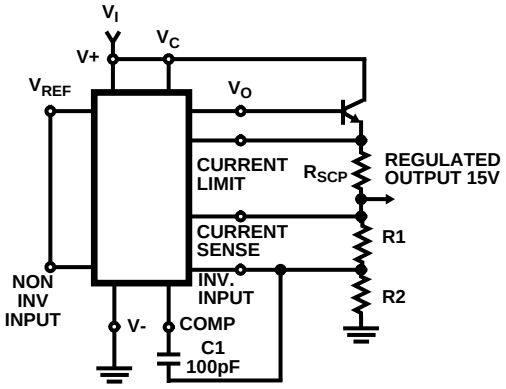
FIGURE 21. HIGH VOLTAGE REGULATOR CIRCUIT (V_O = 7V TO 37V)

Typical Application Circuits (Continued)



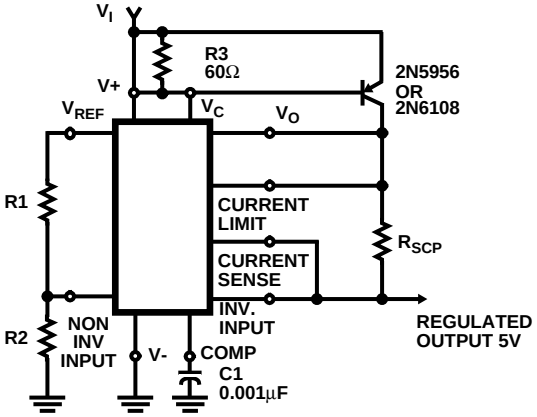
Circuit Performance Data:
Line Regulation (ΔV_I = 3V) 1mV
Load Regulation (ΔI_L = 100mA) 2mV
Note: For Applications Employing the TO-5 Style Package and Where V_Z Is Required, An External; 6.2V Zener Diode Should be Connected in Series with V_O (Terminal 6).

FIGURE 22. NEGATIVE VOLTAGE REGULATOR CIRCUIT



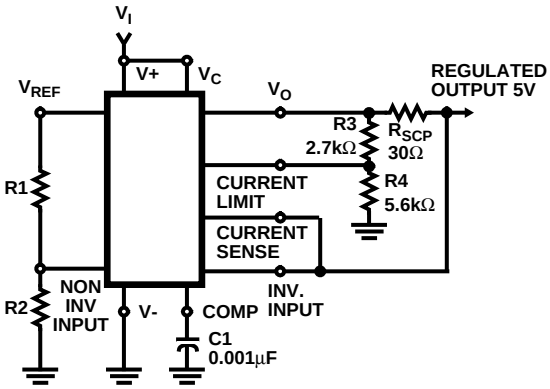
Circuit Performance Data:
Line Regulation (ΔV_I = 3V) 1.5mV
Load Regulation (ΔI_L = 1A) 15mV

FIGURE 23. POSITIVE VOLTAGE REGULATOR CIRCUIT (WITH EXTERNAL n-p-n PASS TRANSISTOR)



Circuit Performance Data:
Line Regulation (ΔV_I = 3V) 0.5mV
Load Regulation (ΔI_L = 1A) 5mV

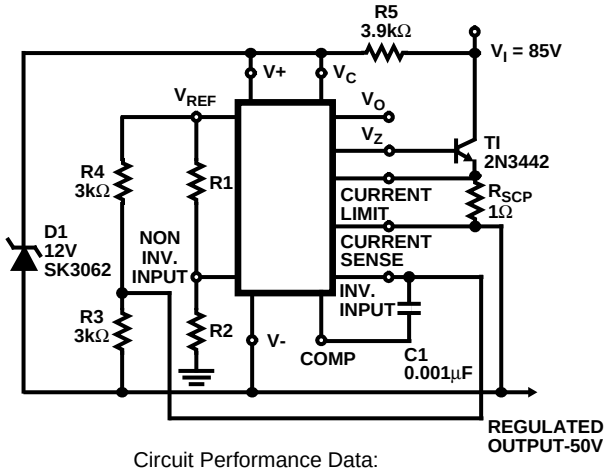
FIGURE 24. POSITIVE VOLTRAGE REGULATOR CIRCUIT (WITH EXTERNAL p-n-p PAS TRANSISTOR)



Circuit Performance Data:
Line Regulation (ΔV = 3V) 0.5mV
Load Regulation (ΔI_L = 10mA) 1mV
Short Circuit Current 20mA

FIGURE 25. FOLDBACK CURRENT LIMITING CIRCUIT

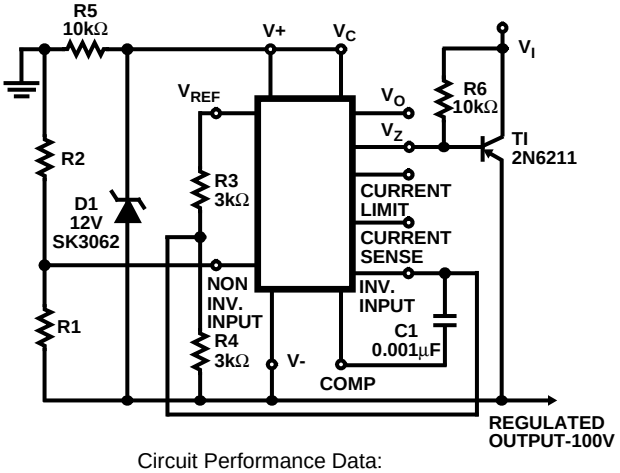
Typical Application Circuits (Continued)



Circuit Performance Data:
Line Regulation (ΔV = 20V) 15mV
Load Regulation (ΔI_L = 50mA) 20mV

NOTE: For applications employing the TO-5 Style Package and where V_Z is required, an external 6.2V zener diode should be connected in series with V_O (terminal 6)

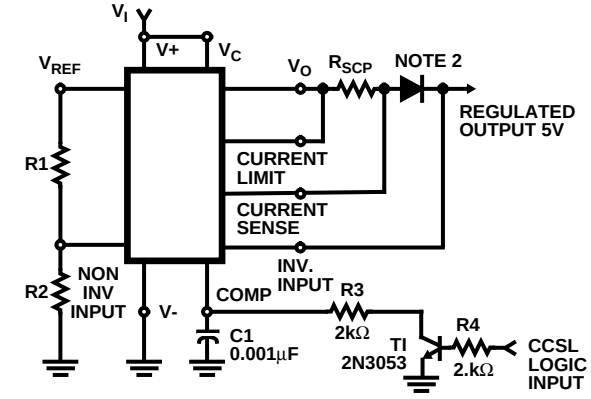
FIGURE 26. POSITIVE FLOATING REGULATOR CIRCUIT



Circuit Performance Data:
Line Regulation (ΔV_I = 20V) 30mV
Load Regulation (ΔI_L =100mA) 20mV

NOTE: For applications employing the TO-5 Style Package and where V_Z is required, an external 6.2V zener diode should be connected in series with V_O (terminal 6)

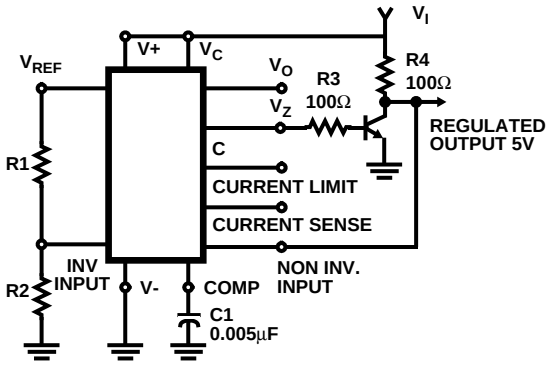
FIGURE 27. NEGATIVE FLOATING REGULATOR CIRCUIT



Circuit Performance Data:
Line Regulation (ΔV_I = 3V) 0.5mV
Load Regulation (ΔI_L = 50mA) 1.5mV
Short Circuit Current 20mA

NOTE: 1. A current limiting transistor may be used for shutdown if current limiting is not required.
2. Add a diode if V_O > 10V.

FIGURE 28. REMOTE SHUTDOWN REGULATOR CIRCUIT WITH CURRENT LIMITING



Circuit Performance Data:
Line Regulation (ΔV_I = 10V) 0.5mV
Load Regulation (ΔI_L = 100mA) 1.5mV

NOTE: For applications employing the TO-5 Style Package and where V_Z is required, an external 6.2V zener diode should be connected in series with V_O (terminal 6).

FIGURE 29. SHUNT REGULATOR CIRCUIT