UNITRODE

UCC2752
UCC3752

Resonant Ring Generator Controller

PRELIMINARY

FEATURES

- Novel Topology for Low-Cost, Efficient Generation of Ring Voltage
- Suitable for Multi-Line Operation
- Selectable 20, 25 and 50 Hz Ring Frequency
- Secondary (AC) Current Limiting Generates an Off-Hook Detect Signal
- Primary Current Limiting to Turn Power Stage Off Under Fault Conditions
- Operates from a Single 12V Supply

DESCRIPTION

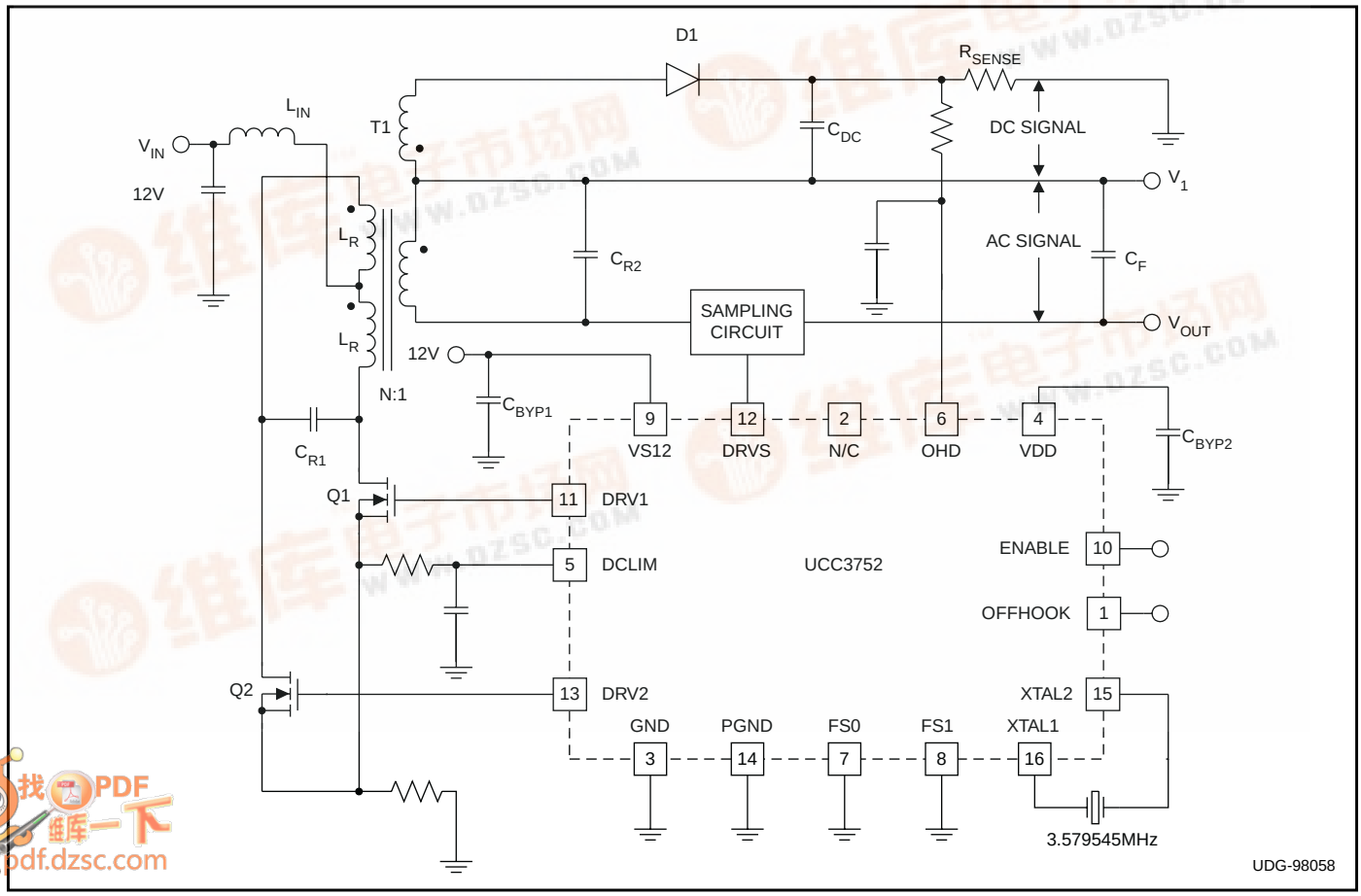
The UCC3752 controller is designed for driving a power stage that generates low frequency, high voltage sinusoidal signals for telephone ringing applications. The controller and the power stage are most suitable for up to 5 line applications where low cost, high efficiency and minimum parts count are critical. A semi-regulated DC voltage is added as an offset to the ringing signal. The ring generator operation is non-isolated and open loop.

The UCC3752 directly drives primary side switches used to implement a push-pull resonant converter topology and transformer coupled sampling switches located on the secondary of the converter. For normal ring signal generation, the primary switching frequency and secondary sampling frequency are precisely offset from each other by the ringing frequency to produce a high voltage low frequency alias signal at the output. The off-hook condition is detected by sensing the AC current and when AC limit is exceeded, a flag is generated on the OFFHOOK pin.

The drive signal frequencies are derived from a high frequency (3579545 Hz) crystal. The primary switching frequency is 89.489 kHz and the sampling frequency is 20, 25 or 50 Hz less depending on the status of frequency select pins FS0 and FS1.

The circuits described in this datasheet are covered under US Patent #5,663,878 and other patents pending.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage 13.2V
Analog Inputs (OHD, DCLIM, XTAL1, XTAL2)
  Maximum Forced Voltage. . . . . –0.3 to 5V
Logic Inputs
  Maximum Forced Voltage . . . . . –0.3 to 7.5V
Reference Output Current (V_{DD}) . . . . . Internally Limited
Output Current (DRV1, DRV2, DRVS) Pulsed 1.5A
Operating Junction Temperature . . . . . –40°C to +125°C
Storage Temperature . . . . . –65°C to +150°C

Note: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specific terminals. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500µS.

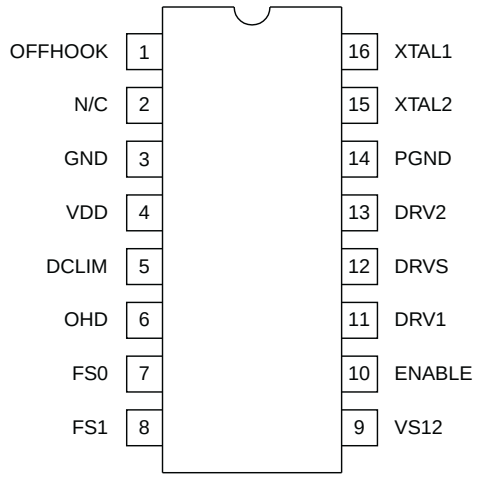
Table I. Frequency selectability decoding.

FS1	FS0	MODE	Sine Wave Frequency (Hz)
0	0	1	20
0	1	1	25
1	0	1	50
1	1	3	0

FS1	FS0	F_{DRVS}	FDRV – FDRVS
0	0	89.469kHz	20Hz
0	1	89.464kHz	25Hz
1	0	89.439kHz	50Hz

CONNECTION DIAGRAMS

(TOP VIEW) DIL-16, SOIC-16
N or D Packages



ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC3752 and –40°C to +85°C for the UCC2752, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V12 Supply Current Section					
Supply Current	ENABLE = 0V		0.5	3	mA
	ENABLE = 5V		0.5	3	mA
Internal Reference with External Bypass Section					
Output Voltage (V_{DD})		4.85	5	5.15	V
Load Regulation	0mA ≤I_{VDD} ≤2mA		5		mV
Line Regulation	10V < V_{S12} < 13V, I_{VDD} = 1mA		3		mV
Short Circuit Current	VDD = 0	5	10		mA
Output Drivers Section (DRV1, DRV2)					
Pull Up Resistance	I_{LOAD} = 10mA to 20mA		6	15	Ω
Pull Down Resistance	I_{LOAD} = 10mA to 20mA		6	15	Ω
Rise Time	C_{LOAD} = 1nF		50	100	nS
Fall Time	C_{LOAD} = 1nF		50	100	nS
Output Drivers Section (DRVS)					
Pull Up Resistance	I_{LOAD} = 10mA to 20mA		4	10	Ω
Pull Down Resistance	I_{LOAD} = 10mA to 20mA		4	10	Ω
Sample Pulse-Width	Mode 1 (Table 1)		280		nS
Rise Time	C_{LOAD} = 1nF		50	100	nS
Fall Time	C_{LOAD} = 1nF		50	100	nS

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC3752 and –40°C to +85°C for the UCC2752, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Limit Section					
DCLIM Threshold			300		mV
DCLIM Input Current	V_{DCLIM} = 0V		–100		nA
OffHook Detect Section					
OHD Threshold			300		mV
OHD Input Current	V_{OHD} = 0V		–100		nA
Offhook V_{OH}	$I_{OFFHOOK}$ = 1mA		4.0		V
Offhook V_{OL}	$I_{OFFHOOK}$ = –1mA		1.0		V
Offhook Pull-Up Impedance	I_{LOAD} = 0mA to 1mA		400		Ω
Offhook Pull-Down Impedance	I_{LOAD} = 0mA to 1mA		250		Ω
Frequency Section (Table 1)					
Primary Switching Frequency	All cases 3.579545 MHz Crystal		89489		Hz
Sampling Switching Frequency	FS0 = 0, FS1 = 0, Mode 1, (Table 1)		89469		Hz
	FS0 = 1, FS1 = 0, Mode 1		89464		Hz
	FS0 = 0, FS1 = 1, Mode 1		89439		Hz

PIN DESCRIPTIONS

DCLIM: Primary current sense input. Signal proportional to the primary switch current. All outputs are turned off when a threshold of 300mV is exceeded on this pin. This current-limit works on a cycle-by-cycle basis.

DRV1, DRV2: Low impedance driver outputs for the primary switches. DRV1 and DRV2 are complimentary and have 50% duty cycle.

DRVS: Low impedance driver output for the sampling switch(es). The pulse width of this output is 280ns. Typically, a pulse transformer is used to couple the short sampling pulses at DRVS to the floating sampling switch(es).

ENABLE: Logic input which turns off the outputs when low.

FS0, FS1: Frequency select pins for determining the difference frequency between primary and secondary pulses under normal operation. These pins can be hard-wired to GND or VDD to get one of the available output frequencies (20,25 and 50 Hz). See Table 1 in the spec table.

GND: Reference point for all the internal voltages and common return for the device.

OFFHOOK: Output indicating the off-hook condition. This signal can be used by an external circuit to switch to a line from the ring generator output to the DC voltage.

OHD: Off-Hook Detect. Voltage proportional to output current DC level is fed into this pin and compared to an internal threshold of 300mV. If the threshold is exceeded, the OFFHOOK output goes high.

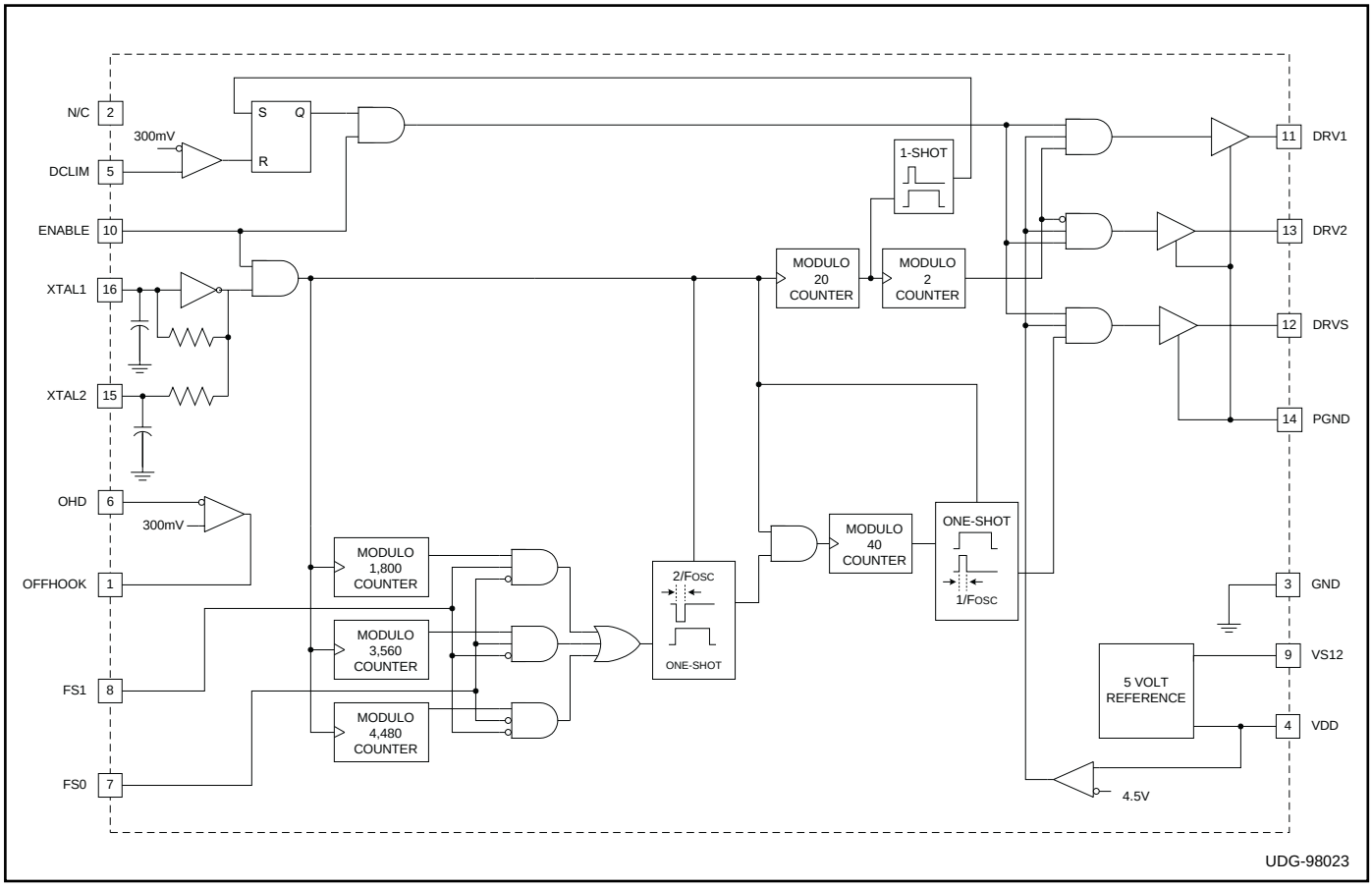
PGND: Return point for the output drivers. Connect to GND at a single point in the circuit.

VDD: Internal regulated 5V supply. This voltage is used to power all the internal precision circuits of the IC. This pin needs to be bypassed to GND with ceramic capacitor.

VS12: External 12V power supply for the IC. Powers VDD and provides voltage for the output drivers.

XTAL1, XTAL2: Pins for connecting precision Crystal to attain the accurate output frequencies. An external square-wave pulse can also be applied to XTAL2 if XTAL1 is tied to VDD/2.

BLOCK DIAGRAM



APPLICATION INFORMATION

Power Stage Operation

The power stage used for the UCC3752 application has two distinct switching circuits which together produce the required low frequency signal on the output. The primary side switching circuit consists of a current fed push-pull resonant circuit that generates the high frequency sinusoidal waveform across the transformer winding. The operation of this type of circuit is extensively covered in Unitrode Application notes U-141 and U-148. Resonant components C_{R1}, C_{R2}, L_R, N should be chosen so that the primary and secondary resonances are well matched. Also, for the UCC3752 operation, switching frequency is fixed by crystal selection. So, the resonant components must be selected to yield a resonant frequency close enough to the switching frequency to get a low distortion sine-wave. Practically, since it is impossible to get an exact match between the two frequencies, the switching frequency should always be higher than the resonant frequency to ensure low distortion and take advantage of ZVT operation. Switches Q1 and Q2 are pulsed at 50% duty cycle at the switching frequency (89.489 kHz) determined by a crystal (3.579545 MHz) connected to the UCC3752. The input voltage for the resonant stage (typically 12V) determines the voltage stress of Q1 and Q2. Transformer turns ratio is determined by the output voltage requirements. On the secondary side, the high frequency waveform is sampled at a predetermined frequency (e.g. 89.469 kHz) which differs from the primary switching frequency by the desired output frequency (e.g. 20 Hz). The sampling is accomplished using a bi-directional switching circuit as shown in Figure 1 and Figure 2. Figure 1 shows the sampling mechanism consisting of two back-to-back FET switches allowing current flow in both directions. The sampling can also be done with a single active switch and a full-bridge rectifier as shown in Fig. 2. The DRVS pin of the UCC3752 provides the drive signal for the sampling switch(es) and this signal is coupled through a pulse transformer. Typical pulsewidth of the sampling signal is 280nS. As a result of sampling, the resultant output signal matches the secondary voltage in amplitude and has a low output frequency desired for ring generation.

The secondary winding of the power transformer also has a tap (or a separate winding) to generate a loosely regulated DC voltage. This DC voltage can be used to offset the ring generator output. It an also be used as a power supply for supplying talk battery voltage in some applica-

APPLICATION INFORMATION (cont.)

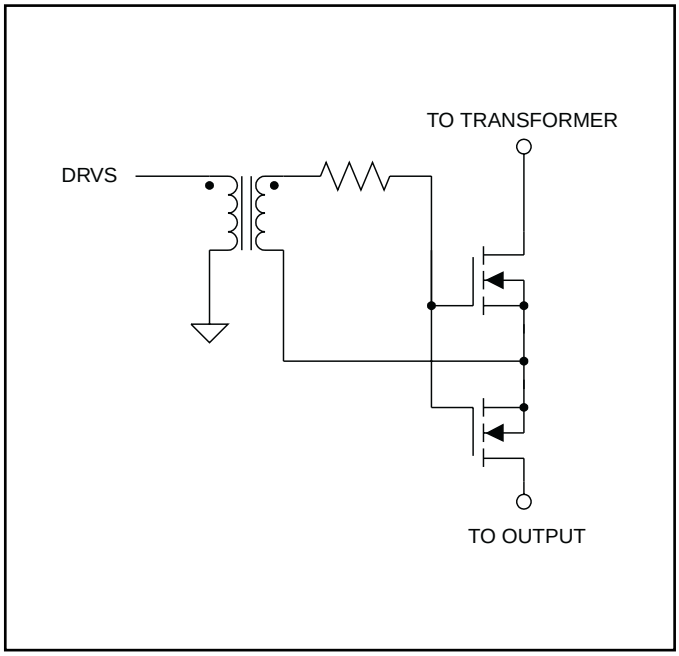


Figure 1. Sampling circuit with two FETs.

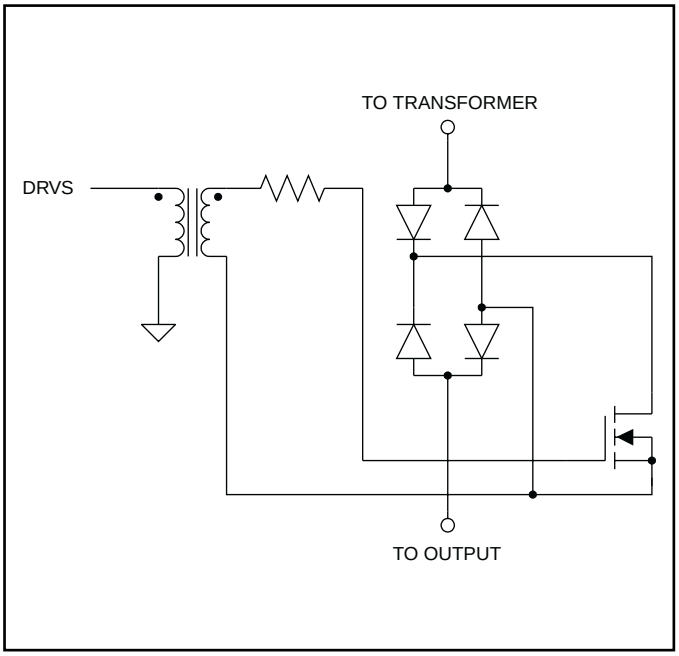


Figure 2. Sampling circuit with single FET and full-bridge rectifier.

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