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COMLINK™ SERIES

CY2CC910

1:10 Clock Fanout Buffer

Features

- Low-voltage operation
- Full-range support:
  - —3.3V
  - —2.5V
  - —1.8V
- Over voltage tolerant input hot swappable
- 1:10 fanout
- Drives either a 50-Ohm or 75-Ohm load
- Low-input capacitance
- Low-output skew
- Low-propagation delay
- Typical (tpd < 4 ns)
- High-speed operation:
  - —-200 MHz@1.8V
  - —650 MHz@2.5V/3.3V
- Industrial versions available
- Available packages include: SOIC, SSOP

Description

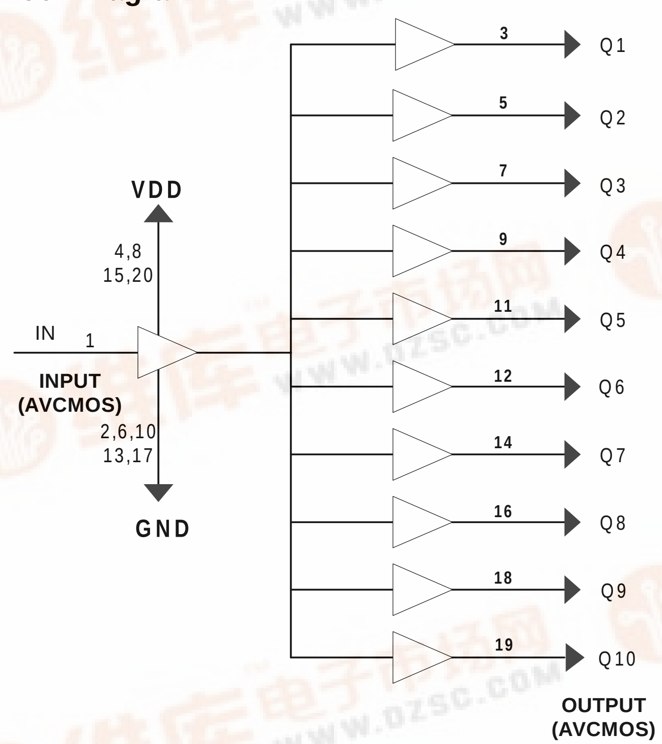
The Cypress series of network circuits are produced using advanced 0.35 micron CMOS technology, achieving the industries fastest logic and buffers.

The Cypress CY2CC910 fanout buffer features one input and ten outputs. Ideal for conversion from/to 3.3V/2.5V/1.8V

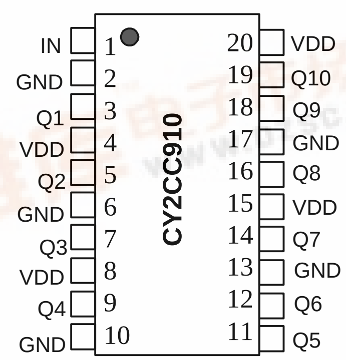
Designed for Data Communications clock management applications, the large fanout from a single input reduces loading on the input clock.

Cypress employs unique AVCMOS type outputs VOI™ (Variable Output Impedance) that dynamically adjust for variable impedance matching and eliminate the need for series damping resistors and reduce noise overall.

Block Diagram



Pin Configuration



20 pin SOIC/SSOP

Pin Description

Pin Number	Pin Name	Description
1	IN	Input
2,6,10,13,17	GND	Ground
4,8,15,20	V_{DD}	Power Supply
3,5,7,9,11,12,14,16,18,19	Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8,Q9,Q10	Output

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Maximum Ratings[1]

Storage Temperature: ....–65°C to +150°C
Ambient Temperature:...................................–40°C to +85°C
Supply Voltage to Ground Potential
V_{CC} .... –0.5V to 4.6V
Input .... –0.5V to 5.8V

Supply Voltage to Ground Potential
(Outputs only) .... –0.5V to V_{DD} + 1V
DC Output Voltage.................................... –0.5V to V_{DD} + 1V
Power Dissipation.. 0.75W

Variable Output Impedance Control (VOI™)

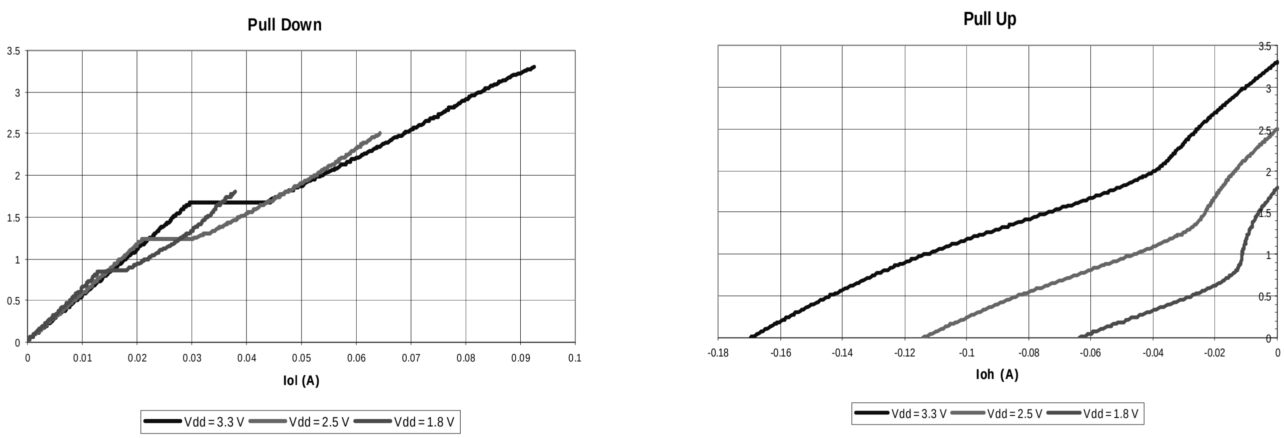


Figure 1. Output Voltage vs. Output Current (TA = 25°C)

DC Electrical Characteristics @ 3.3V (see *Figure 2*)

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output High Voltage	V_{DD} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12 mA	2.3	3.3		V
V_{OL}	Output Low Voltage	V_{DD} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12 mA		0.2	0.5	V
V_{IH}	Input High Voltage	Guaranteed Logic High Level		2		5.8	V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level				0.8	V
I_{IH}	Input High Current	V_{DD} = Max.	V_{IN} = 2.7V			1	uA
I_{IL}	Input Low Current	V_{DD} = Max.	V_{IN} = 0.5V			–1	uA
I_I	Input High Current	V_{DD} = Max., V_{IN} = V_{DD}(Max.)				20	uA
V_{IK}	Clamp Diode Voltage	V_{DD} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OK}	Continuous Clamp Current	V_{DD} = Max., V_{OUT} = GND				–50	mA
O_{OFF}	Power-down Disable	V_{DD} = GND, V_{OUT} = < 4.5V				100	uA
V_H	Input Hysteresis				80		mV

Note:

1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics @ 2.5V (see *Figure 2*)

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output High Voltage	V_{DD} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –7 mA	1.8			V
			I_{OH}= 12 mA	1.6			V
V_{OL}	Output Low Voltage	V_{DD} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12 mA			0.65	V
V_{IH}	Input High Voltage	Guaranteed Logic High Level		1.6		5.0	V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level				0.8	V
I_{IH}	Input High Current	V_{DD} = Max.	V_{IN} = 2.4V			1	uA
I_{IL}	Input Low Current	V_{DD} = Max.	V_{IN} = 0.5V			–1	uA
I_I	Input High Current	V_{DD} = Max., V_{IN} = V_{DD}(Max.)				20	uA
V_{IK}	Clamp Diode Voltage	V_{DD} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OK}	Continuous Clamp Current	V_{DD} = Max., V_{OUT} = GND				–50	mA
O_{OFF}	Power Down Disable	V_{DD} = GND, V_{OUT} = < 4.5V				100	uA
V_H	Input Hysteresis				80		mV

DC Electrical Characteristics @ 1.8V (see *Figure 6*)

Parameter	Description	Test Condition[2]	Min.	Max.	Unit
V_{DD}	Supply Voltage		1.71	1.89	V
V_{IH}	Input High Voltage		0.65V_{DD}[1.1]	4.3	V
V_{IL}	Input Low Voltage		–0.3	0.35 V_{DD}[0.6]	V
V_{OH}	Output High Voltage	I_{OH} = –2 mA	V_{DD} – 0.45[1.2]		V
V_{OL}	Output Low Voltage	I_{OH} = 2 mA		0.45	V

Capacitance

Parameter	Description	Test Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	2.5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	6.5		pF

Power Supply Characteristics (see *Figure 2*)

Parameter	Description	Test Conditions	Min.	Typ	Max	Unit
ΔI_{CC}	Delta I_{CC} Quiescent Power Supply Current	(I_{DD} @ V_{DD} = Max and V_{IN} = V_{DD}) – (I_{DD} @ V_{DD} = Max and V_{IN} = V_{DD} – 0.6V)			50	uA
I_{CCD}	Dynamic Power Supply Current	V_{DD} = Max Input toggling 50% Duty Cycle, Outputs Open			0.63	mA/ MHz
I_C	Total Power Supply Current	V_{DD} = Max Input toggling 50% Duty Cycle, Outputs Open fL = 40 MHZ			25	mA

Note:

2. Test load conditions: 500-Ohm to ground with approximately 6-pF total loading and 200-MHz maximum frequency.

High Frequency Parametrics

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
D_J	Jitter, Deterministic	50% duty cycle tW(50–50) The "point to point load circuit" | Output Jitter – Input Jitter |	See *Figure 4*			20	ps
F_{max} 3.3V	Maximum frequency V_{DD} = 3.3V	50% duty cycle tW(50–50) Standard Load Circuit.	See *Figure 2*			160	MHz
		50% duty cycle tW(50–50) The "point to point load circuit"	See *Figure 4*			650	
F_{max} 2.5V	Maximum frequency V_{DD} = 2.5 V	The "point to point load circuit" V_{IN} = 2.4V/0.0V V_{OUT} = 1.7V/0.7V	See *Figure 4*			200	MHz
F_{max} 1.8V	Maximum frequency V_{DD} = 1.8V	The "6-pF load circuit" V_{IN} = 1.7/0.0V V_{OUT} = 1.2V/0.4V	See *Figure 6*			200	MHz
$F_{max(20)}$	Maximum frequency V_{DD} = 3.3 V	20% duty cycle tW(20-80) The "point to point load circuit" V_{IN} = 3.0V/0.0V V_{OUT} = 2.3V/0.4V	See *Figure 5*			250	MHz
t_W 3.3V	Minimum pulse V_{DD} = 3.3 V	The "point to point load circuit" V_{IN} = 3.0V/0.0V F= 100 MHz V_{OUT} = 2.0V/0.8V	See *Figure 4*	1			ns
t_W 2.5V	Minimum pulse V_{DD} = 2.5 V	The "point to point load circuit" V_{IN} = 2.4V/0.0V F= 100 MHz V_{OUT} = 1.7V/0.7V	See *Figure 4*	1			
t_W 1.8V	Minimum pulse V_{DD} = 1.8V	The "6-pF load circuit" V_{IN} = 1.7V/0.0V V_{OUT} = 1.2V/0.4V	See *Figure 6*	1			

AC Switching Characteristics @ 3.3V V_{DD} = 3.3V ± 5%, Temperature = –40°C to +85°C

Parameter	Description		Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay – Low to High	See *Figure 3*	1.5	2.7	3.5	nS
t_{PHL}	Propagation Delay – High to Low		1.5	2.7	3.5	nS
t_R	Output Rise Time			0.8		V/nS
t_F	Output Fall Time			0.8		V/nS
$t_{SK(0)}$	Output Skew: Skew between outputs of the same package (in phase).	See *Figure 10*			0.2	nS
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output (t_{PHL} – t_{PLH}).	See *Figure 9*			0.2	nS
$t_{SK(t)}$	Package Skew: Skew b.etween outputs of different packages at the same power supply voltage, temperature and package type.	See *Figure 11*			0.4	nS

AC Switching Characteristics @ 2.5V V_{DD} = 2.5V ± 5%, Temperature = –40°C to +85°C

Parameter	Description		Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay – Low to High	See *Figure 3*	1.5	2.7	3.5	nS
t_{PHL}	Propagation Delay – High to Low		1.5	2.7	3.5	nS
t_R	Output Rise Time			0.8		V/nS
t_F	Output Fall Time			0.8		V/nS
$t_{SK(0)}$	Output Skew: Skew between outputs of the same package (in phase).	See *Figure 10*			0.2	nS
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output (t_{PHL} – t_{PLH}).	See *Figure 9*			0.2	nS
$t_{SK(t)}$	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type.	See *Figure 11*			0.4	nS

AC Switching Characteristics @ 1.8V V_{DD} = 1.8V ±5%, Temperature = –40°C to +85°C

Parameter	Description		Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay – Low to High	See *Figure 7*	1.5	2.7	3.5	nS
t_{PHL}	Propagation Delay – High to Low		1.5	2.7	3.5	nS
t_R	Output Rise Time 20 – 80%		0.2		1.5	nS
t_F	Output Fall Time 20 – 80%		0.2		1.5	nS
$t_{SK(0)}$	Output Skew: Skew between outputs of the same package (in phase).	See *Figure 10*			0.2	nS
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output (t_{PHL} – t_{PLH}).	See *Figure 9*			0.2	nS
$t_{SK(t)}$	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type.	See *Figure 11*			0.4	nS

Parameter Measurement Information: V_{DD}@3.3V–2.5V

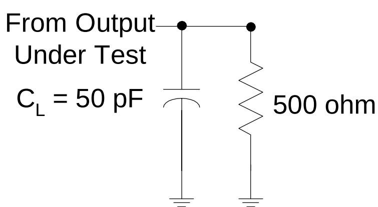


Figure 2. Load Circuit [3,4,5]

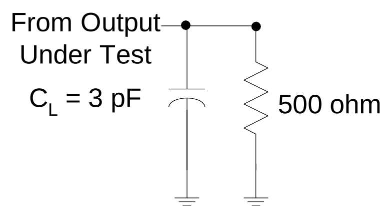


Figure 4. Point to Point Load Circuit[3,4,5]

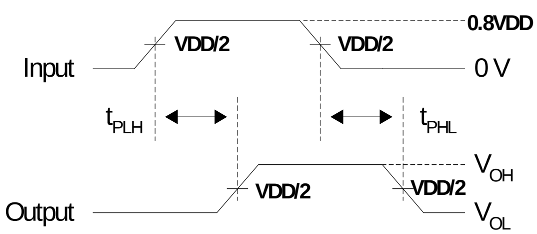


Figure 3. Voltage Waveforms Propagation Delay Times[6]

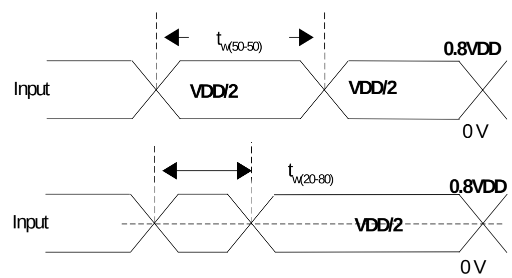


Figure 5. Voltage Waveforms–Pulse Duration[4]

Parameter Measurement Information: V_{DD}@1.8V

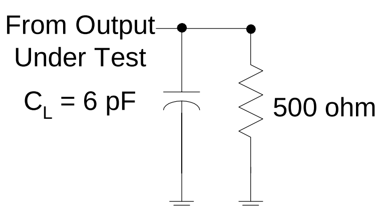


Figure 6. Load Circuit [3,4,5]

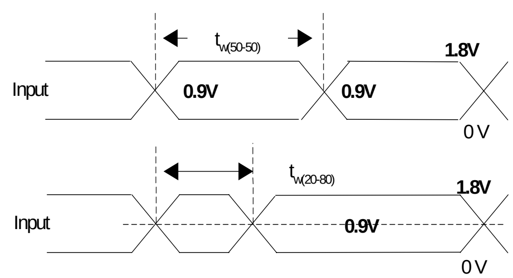


Figure 8. Voltage Waveforms–Pulse Duration[4]

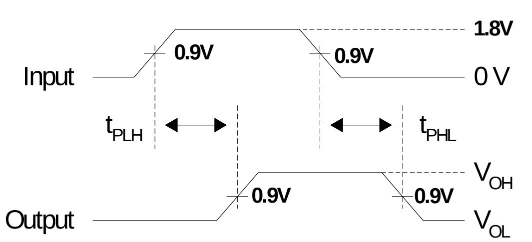
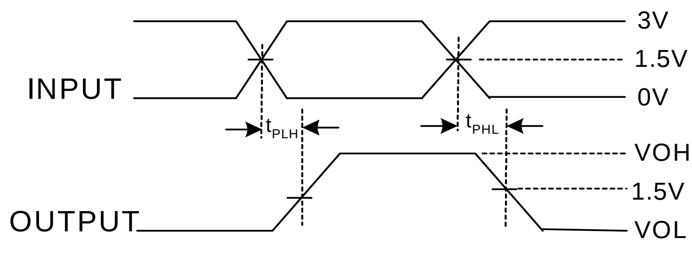


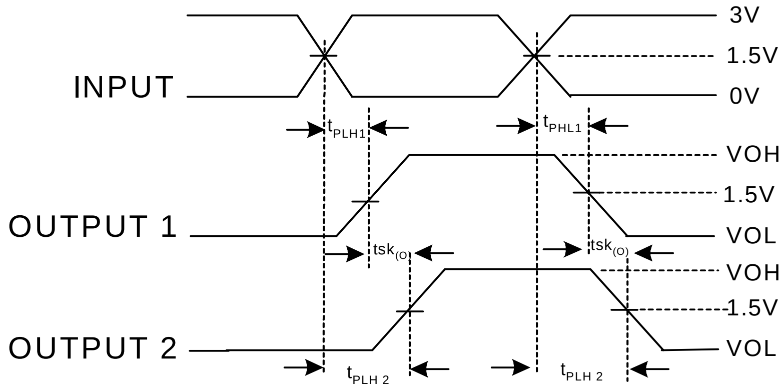
Figure 7. Voltage Waveforms Propagation Delay Times[6]

Notes:
3. C_L includes probe and jig capacitance.
4. All input pulses are supplied by generators having the following characteristics: PRR < 100 MHz, Z_0 = 50Ω, t_R < 2.5 nS, t_F < 2.5 nS.
5. The outputs are measured one at a time with one transition per measurement.
6. T_{PLH} and T_{PHL} are the same as t_{pd}.



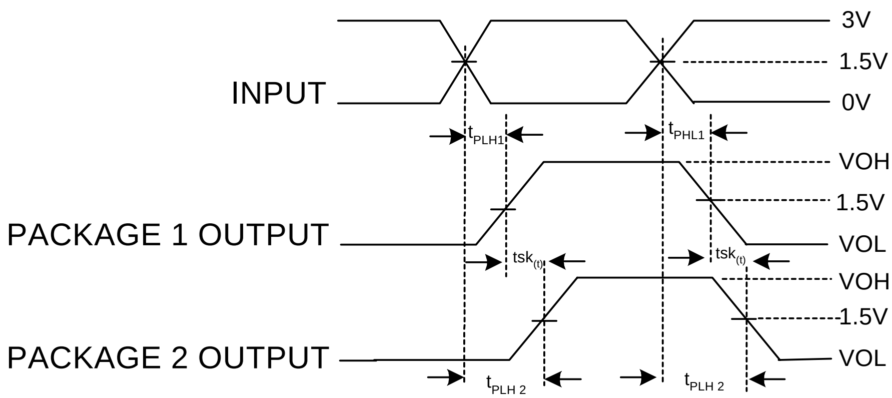
$tsk_{(P)} = | t_{PHL} - t_{PLH} |$

Figure 9. Pulse Skew–tsk$_{(p)}$



$tsk_{(P)} = | t_{PLH2} - t_{PLH1} |$ or $t_{PHL2} - t_{PHL1} |$

Figure 10. Output Skew–tsk$_{(0)}$



$tsk_{(t)} = | t_{PLH2} - t_{PLH1} |$ or $t_{PHL2} - t_{PHL1} |$

Figure 11. Package Skew - tsk$_{(t)}$

Ordering Information

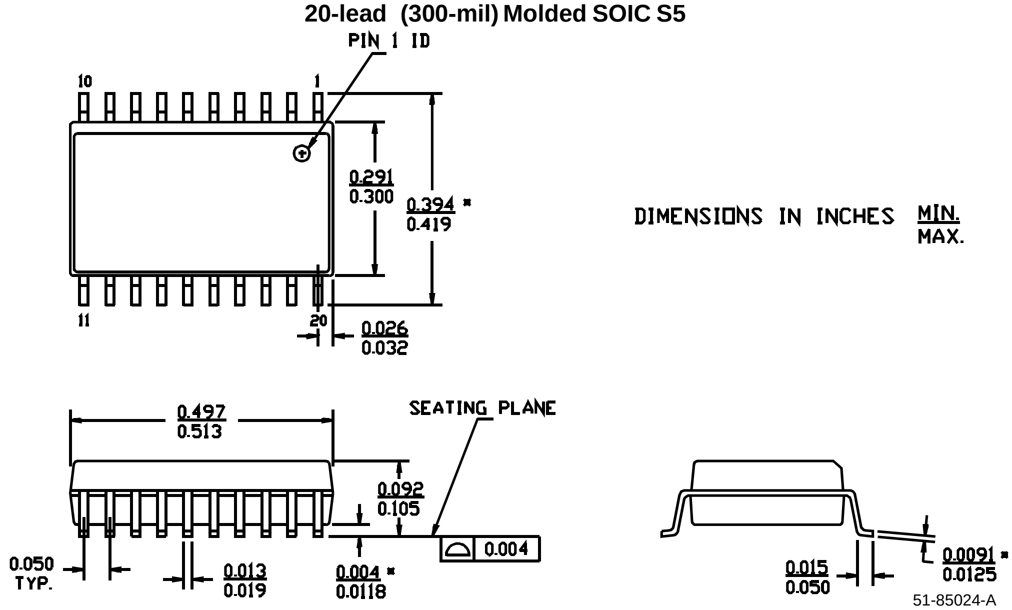
Part Number	Package Type	Product Flow
CY2CC910SI	20-pin SOIC	Industrial, –40° to 85°C
CY2CC910SIT	20-pin SOIC–Tape and Reel	Industrial, –40° to 85°C
CY2CC910OI	20-pin SSOP	Industrial, –40° to 85°C
CY2CC910OIT	20-pin SSOP–Tape and Reel	Industrial, –40° to 85°C
CY2CC910SC	20-pin SOIC	Commercial, 0°C to 70°C

Ordering Information (continued)

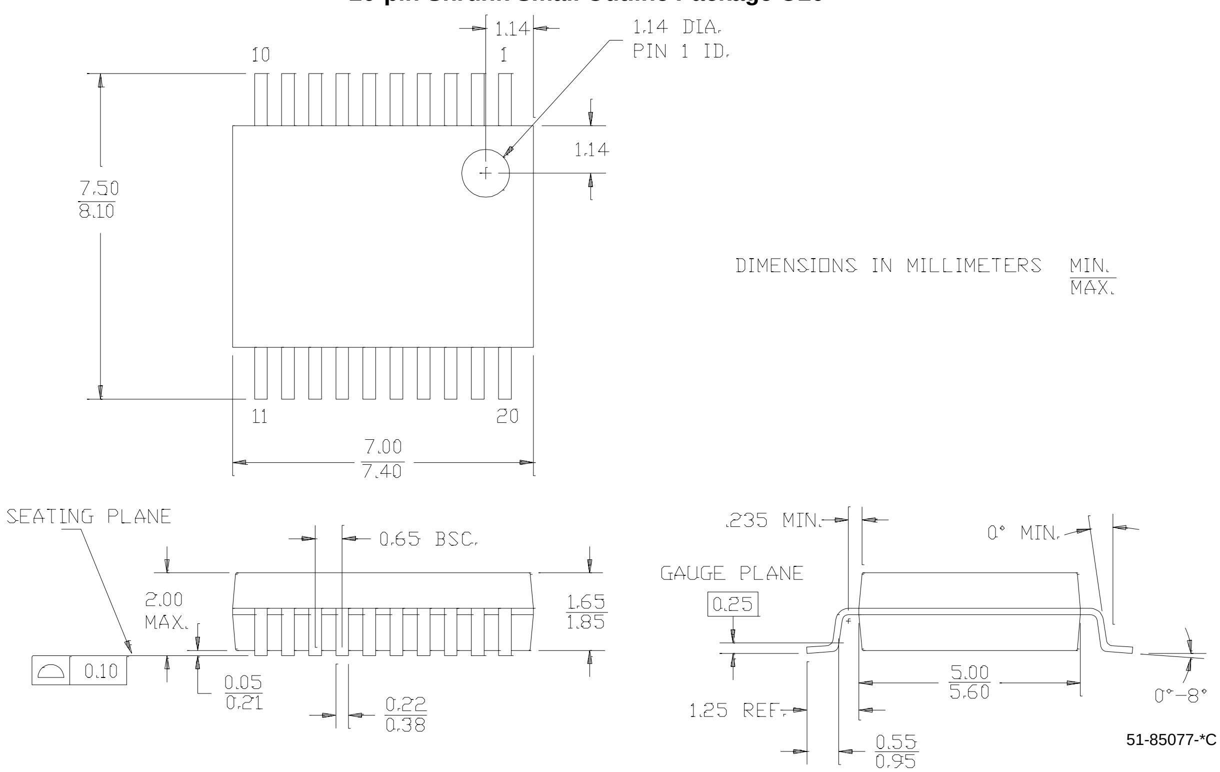
CY2CC910SCT	20-pin SOIC–Tape and Reel	Commercial, 0°C to 70°C
CY2CC910OC	20-pin SSOP	Commercial, 0°C to 70°C
CY2CC910OCT	20-pin SSOP–Tape and Reel	Commercial, 0°C to 70°C

Package Drawing and Dimensions

20-lead (300-mil) Molded SOIC S5



20-pin Shrunk Small Outline Package O20



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Document History Page

Document Title: CY2CC910 COMLINK™ SERIES 1:10 Clock Fanout Buffer Document #: 38-07348				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	114318	05/10/02	TSM	New Data Sheet
*A	119148	10/07/02	RGL	Added 5.8 as the Max. value for V_{IH} in the DC Electrical Characteristics @3.3V table. Changed the Max. value of V_{IH} from 5.8 to 5.0 in the DC Electrical Characteristics @2.5V table. Changed the value of V_{IH} from V_{DD}+0.3 [2.25] to 4.3 in the DC Electrical Characteristics @1.8V table.