

CD22100

CMOS 4 x 4 Crosspoint Switch with Control Memory High-Voltage Type (20V Rating)

February 1999

Features

- Low ON Resistance 75Ω (Typ) at $V_{DD} = 12V$
- "Built-In" Control Latches
- Large Analog Signal Capability $\pm V_{DD}/2$
- 10MHz Switch Bandwidth
- Matched Switch Characteristics $\Delta R_{ON} = 18\Omega$ (Typ) at $V_{DD} = 12V$
- High Linearity - 0.5% Distortion (Typ) at $f = 1kHz$, $V_{IN} = 5V_{P-P}$, $V_{DD} = 10V$, and $R_L = 1k\Omega$
- Standard CMOS Noise Immunity
- 100% Tested for Maximum Quiescent Current at 20V

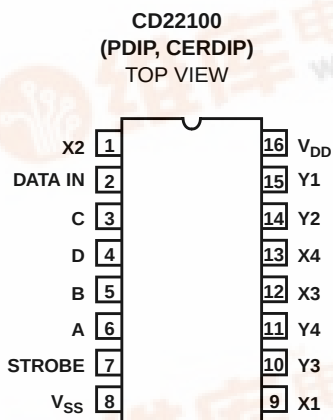
Description

CD22100 combines a 4 x 4 array of crosspoints (transmission gates) with a 4-line to 16-line decoder and 16 latch circuits. Any one of the sixteen transmission gates (crosspoints) can be selected by applying the appropriate four line address. The selected transmission gate can be turned on or off by applying a logic one or zero, respectively, to the data input and strobing the strobe input to a logic one. Any number of the transmission gates can be ON simultaneously. When the required operating power is applied to the CD22100, the states of the 16 switches are indeterminate. Therefore, all switches must be turned off by putting the strobe high and data in low, and then addressing all switches in succession.

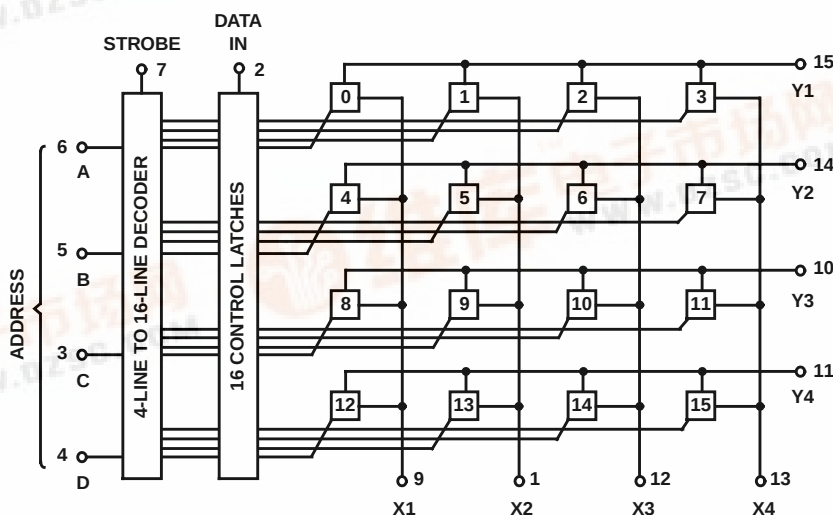
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD22100E	-40 to 85	16 Ld PDIP	E16.3
CD22100F	-55 to 125	16 Ld Cerdip	F16.3

Pinout



Functional Diagram



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Absolute Maximum Ratings

Supply Voltage (Referenced to VSS Terminal) -0.5 to 20V
 Input Voltage (All Inputs) -0.5 to V_{DD} 0.5V
 Input Current (Any one input (Note 1)) $\pm 10\text{mA}$
 Power Dissipation
 For $T_A = -40^\circ\text{C}$ to 60°C (Package Type E) 500mW
 For $T_A = 60^\circ\text{C}$ to 85°C
 (Package Type E) Derate Linearly 12mW/ $^\circ\text{C}$ to 200mW
 For $T_A = -55^\circ\text{C}$ to 100°C (Package Type F) 500mW
 For $T_A = 100^\circ\text{C}$ to 125°C
 (Package Type F) Derate Linearly 12mW/ $^\circ\text{C}$ to 200mW
 Device Dissipation per Transmission Gate
 For $T_A = \text{Full Package Temperature Range}$ (All Types) 100mW

Thermal Information

Maximum Junction Temperature 175°C
 Maximum Junction Temperature (Plastic Package) 150°C
 Storage Temperature Range $-65^\circ\text{C} \leq T_A \leq 150^\circ\text{C}$
 Maximum Lead Temperature (Soldering 10s) 300°C

Operating Conditions

Temperature Range
 Package Type F $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$
 Package Type E $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$
 Supply Voltage Range
 For $T_A = \text{Full Package Temperature Range}$ 3V to 18V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Values at -55°C , 25°C , 125°C Apply to F Package
 Values at -40°C , 25°C , 85°C Apply to E Package

PARAMETER	SYMBOL	TEST CONDITIONS			-55°C	-40°C	85°C	125°C	25°C			UNITS	
			FIG.	V _{DD} (V)	MAX	MAX	MAX	MAX	MIN	TYP	MAX		
STATIC CROSSPOINTS													
Quiescent Device Current	I _{DD} (Max)		1	5	5	5	150	150	-	0.04	5	μA	
			1	10	10	10	300	300	-	0.04	10	μA	
			1	15	20	20	600	600	-	0.04	20	μA	
			1	20	100	100	3000	3000	-	0.08	100	μA	
On Resistance	R _{ON} (Max)	Any Switch V _{IS} = 0 to V _{DD}	11	5	475	500	725	800	-	225	600	Ω	
			12	10	135	145	205	230	-	85	180	Ω	
			-	12	100	110	155	175	-	75	135	Ω	
			13	15	70	75	110	125	-	65	95	Ω	
ΔR _{ON} Resistance	ΔR _{ON}	Between any two switches	-	5	-	-	-	-	-	25	-	Ω	
			-	10	-	-	-	-	-	10	-	Ω	
			-	12	-	-	-	-	-	8	-	Ω	
			-	15	-	-	-	-	-	5	-	Ω	
OFF Switch Leakage Current	I _L (Max)	All switches OFF, V _{IS} = 18V	3	18	±100		±1000		-	±1	±100 (Note 2)	nA	
STATIC CONTROLS													
Input Low Voltage	V _{IL} (Max)	OFF switch I _L < 0.2μA	-	5	1.5					-	-	1.5	V
			-	10	3					-	-	3	V
			-	15	4					-	-	4	V
Input High Voltage	V _{IH} (Min)	ON switch see R _{ON} characteristic	-	5	3.5			3.5		-	-	V	
			-	10	7			7		-	-	V	
			-	15	11			11		-	-	V	
Input Current	I _{IN} (Max)	Any control V _{IN} = 0, 18V	2	18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	μA	

NOTES:

- Maximum current through transmission gates (switches) = 25mA.
- Determined by minimum feasible leakage measurement for automatic testing.

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Electrical Specifications $T_A = 25^\circ\text{C}$

PARAMETER	SYMBOL	TEST CONDITIONS					MIN	TYP	MAX	UNITS
		FIGURE	f _{IS} (kHz)	R _L (kΩ)	V _{IS} (V) (Note 3)	V _{DD} (V)				
DYNAMIC CROSSPOINTS										
Propagation Delay Time, (Switch ON) Signal Input to Output	t _{PHL} , t _{PLH}	5	-	10	5	5	-	30	60	ns
					10	10	-	15	30	ns
					15	15	-	10	20	ns
					C _L = 50pF; t _R , t _F = 20ns					
Frequency Response (Any Switch ON)	f _{3dB}	16	1	1	5	10	-	40	-	MHz
			Sine Wave Input, 20 log $\frac{V_{OS}}{V_{IS}}$ = -3dB							
Sine Wave Response (Distortion)	THD		1	1	5	10	-	0.5	-	%
Feedthrough (All switches OFF)	F _{DT}		1.6	1	5	10	-	-80	-	dB
			Sine Wave Input							
Frequency for Signal Crosstalk Attenuation of 40dB Attenuation of 110dB	F _{CT}	7	-	1	10	10	-	1.5	-	MHz
			Sine Wave Input				-	0.1	-	kHz
			-	-	-	-	-	0.1	-	kHz
Capacitance: Xn to Ground	C _{IS}		-	-	-	5 - 15	-	18	-	pF
Yn to Ground			-	-	-	5 - 15	-	30	-	pF
Feedthrough	C _{IOS}		-	-	-	-	-	0.4	-	pF
DYNAMIC CONTROLS										
Propagation Delay Time: Strobe to Output (Switch Turn-ON to High Level)	t _{PZH}	8	R _L = 1kΩ, C _L = 50pF, t _R , t _F = 20ns			5	-	300	600	ns
						10	-	125	250	ns
						15	-	80	160	ns
Propagation Delay Time: Data-In to Output (Turn-ON to High Level)	t _{PZH}	9	R _L = 1kΩ, C _L = 50pF, t _R , t _F = 20ns			5	-	110	220	ns
						10	-	40	80	ns
						15	-	25	50	ns
Propagation Delay Time: Address to Output (Turn-ON to High Level)	t _{PZH}	10	R _L = 1kΩ, C _L = 50pF, t _R , t _F = 20ns			5	-	350	700	ns
						10	-	135	270	ns
						15	-	90	180	ns
Propagation Delay Time: Strobe to Output (Switch Turn-OFF)	t _{PHZ}	8	R _L = 1kΩ, C _L = 50pF, t _R , t _F = 20ns			5	-	165	330	ns
						10	-	85	170	ns
						15	-	70	140	ns
Propagation Delay Time: Data-In to Output (Turn-ON to Low Level)	t _{PZL}	9	R _L = 1kΩ, C _L = 50pF, t _R , t _F = 20ns			5	-	210	420	ns
						10	-	110	220	ns
						15	-	100	200	ns
Propagation Delay Time: Address to Output (Turn-OFF)	t _{PHZ}	10	R _L = 1kΩ, C _L = 50pF, t _R , t _F = 20ns			5	-	435	870	ns
						10	-	210	420	ns
						15	-	160	320	ns

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Electrical Specifications $T_A = 25^\circ\text{C}$ (Continued)

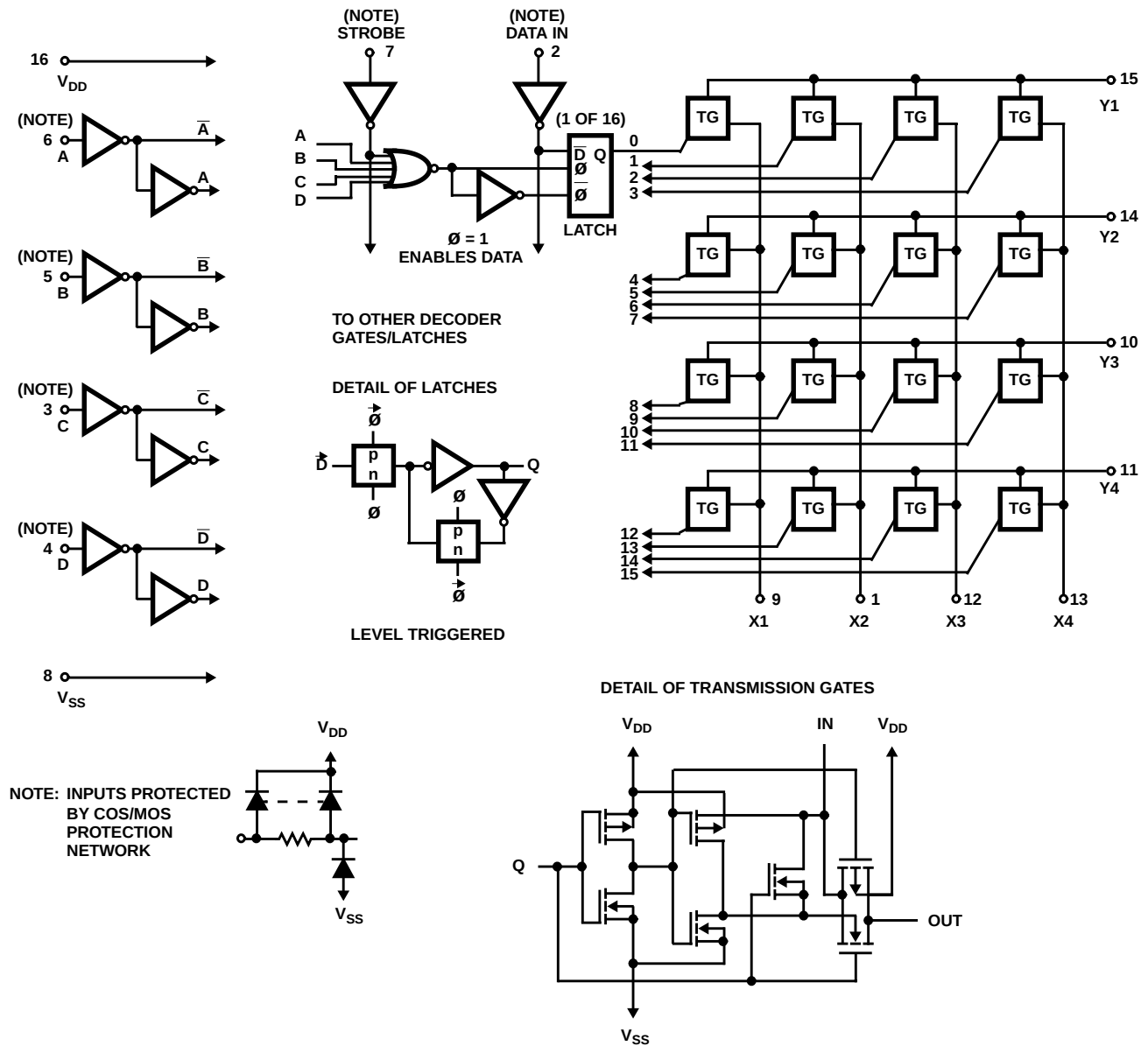
PARAMETER	SYMBOL	TEST CONDITIONS					MIN	TYP	MAX	UNITS
		FIGURE	f _{IS} (kHz)	R _L (kΩ)	V _{IS} (V) (Note 3)	V _{DD} (V)				
Minimum Setup Time Data-In to Strobe, Address	t _S	8, 10	R _L = 1kΩ, C _L = 50pF, t _R , t _F = 20ns			5	-	95	190	ns
						10	-	25	50	ns
						15	-	15	30	ns
Minimum Hold Time Data-In to Strobe, Address	t _H	8, 10	R _L = 1kΩ, C _L = 50pF, t _R , t _F = 20ns			5	-	180	360	ns
						10	-	110	220	ns
						15	-	35	70	ns
Maximum Switching Frequency	f _∅		R _L = 1kΩ, C _L = 50pF, t _R , t _F = 20ns			5	0.6	1.2	-	MHz
						10	1.6	3.2	-	MHz
						15	2.5	5	-	MHz
Minimum Strobe Pulse Width	t _W	8				5	-	300	600	ns
						10	-	120	240	ns
						15	-	90	180	ns
Control Crosstalk, Data-In, Address or Strobe to Output		6	Square Wave Input; t _R , t _F = 20ns			10	-	75	-	mV _{PEAK}
			-	10	10					
Input Capacitance	C _{IN}		Any Control Input			-	-	5	7.5	pF

NOTE:

3. Peak-to-peak voltage symmetrical about $\frac{V_{DD}}{2}$.

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Schematic Diagram

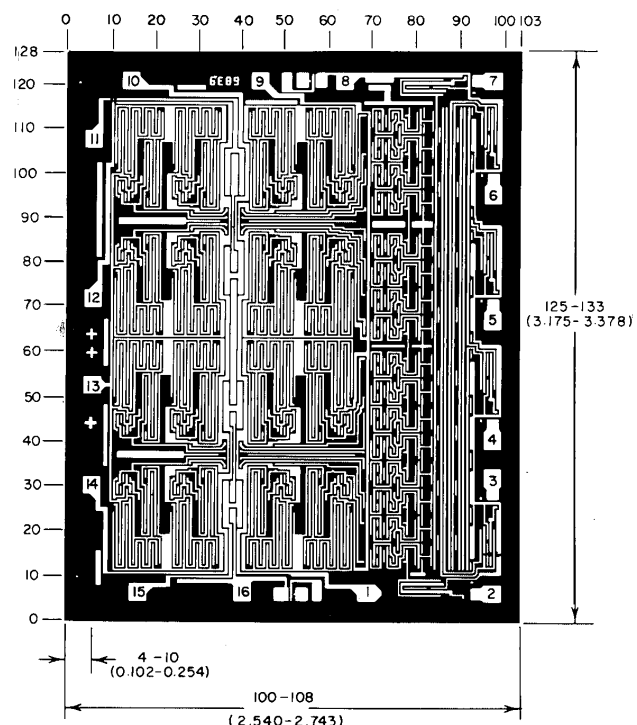


TRUTH TABLE

ADDRESS				SELECT	ADDRESS				SELECT
A	B	C	D		A	B	C	D	
0	0	0	0	X1Y1	0	0	0	1	X1Y3
1	0	0	0	X2Y1	1	0	0	1	X2Y3
0	1	0	0	X3Y1	0	1	0	1	X3Y3
1	1	0	0	X4Y1	1	1	0	1	X4Y3
0	0	1	0	X1Y2	0	0	1	1	X1Y4
1	0	1	0	X2Y2	1	0	1	1	X2Y4
0	1	1	0	X3Y2	0	1	1	1	X3Y4
1	1	1	0	X4Y2	1	1	1	1	X4Y4

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Metallization Mask Layout



Test Circuits and Waveforms

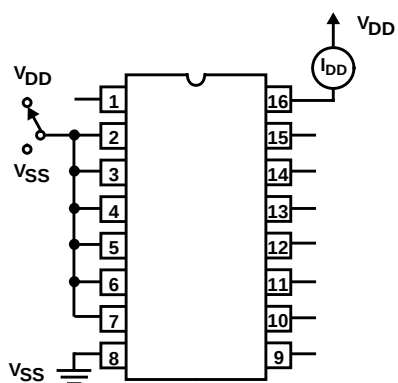


FIGURE 1. QUIESCENT CURRENT TEST CIRCUIT

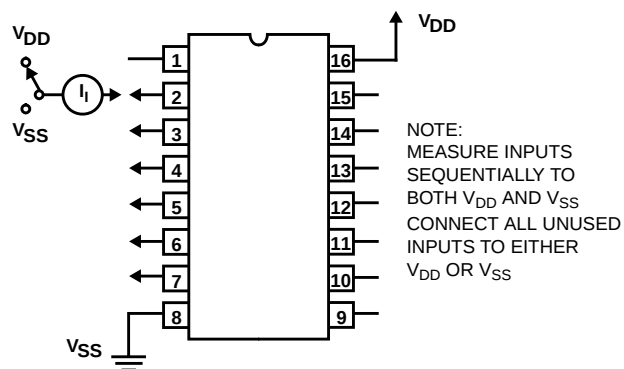


FIGURE 2. INPUT CURRENT TEST CIRCUIT

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Test Circuits and Waveforms (Continued)

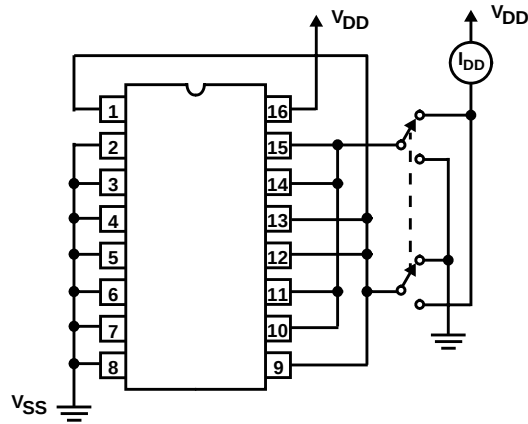
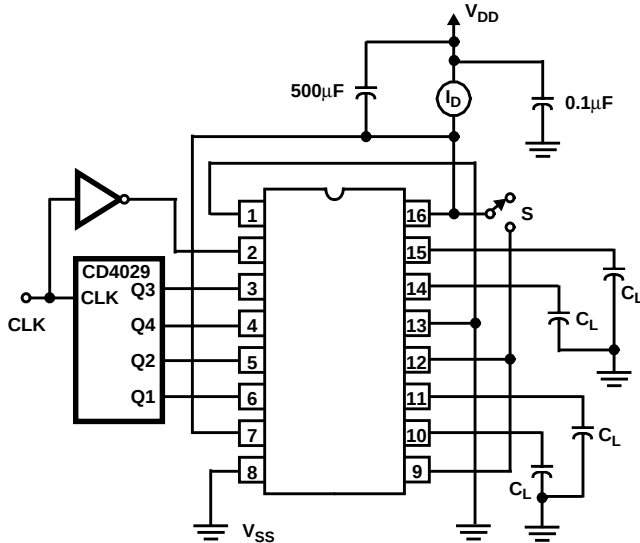


FIGURE 3. OFF SWITCH INPUT OR OUTPUT LEAKAGE CURRENT TEST CIRCUIT



NOTE:
CLOSE SWITCH S AFTER APPLYING V_{DD}

FIGURE 4. DYNAMIC POWER DISSIPATION TEST CIRCUIT AND TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF SWITCHING FREQUENCY

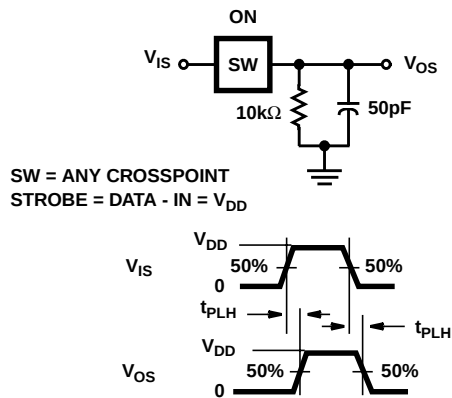


FIGURE 5. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (SIGNAL INPUT TO SIGNAL OUTPUT, SWITCH ON)

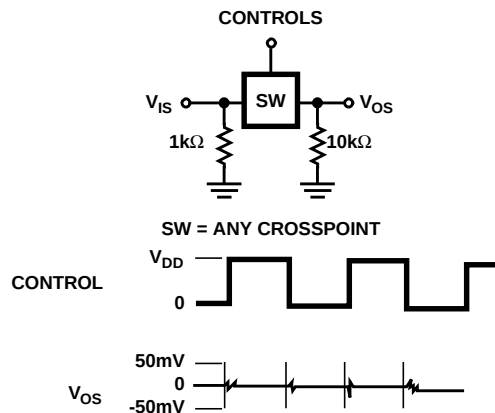


FIGURE 6. TEST CIRCUIT AND WAVEFORMS FOR CROSSTALK (CONTROL INPUT TO SIGNAL OUTPUT)

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Test Circuits and Waveforms (Continued)

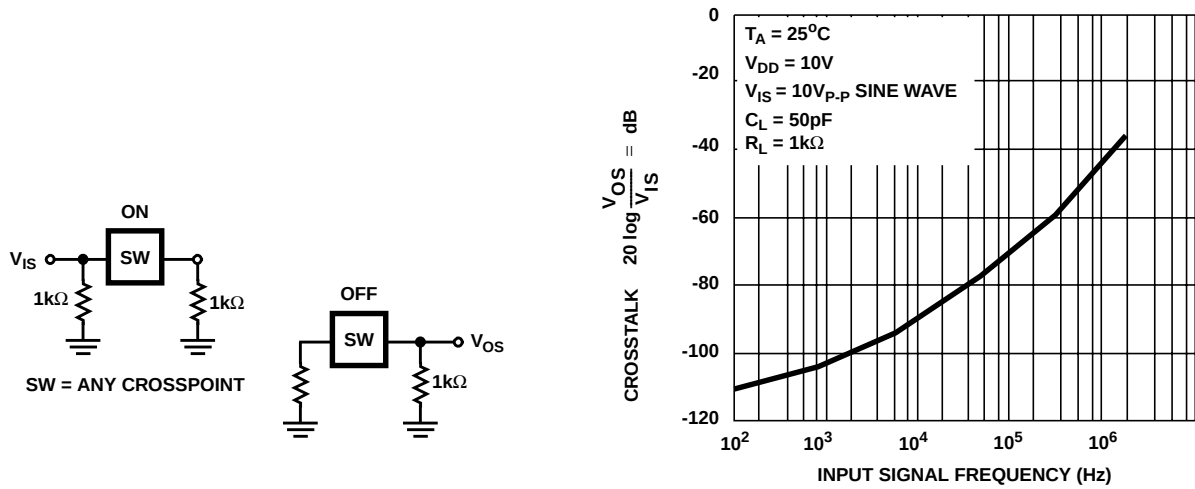


FIGURE 7. TEST CIRCUIT AND TYPICAL CROSSTALK BETWEEN SWITCH CIRCUITS IN THE SAME PACKAGE AS A FUNCTION OF SIGNAL FREQUENCY

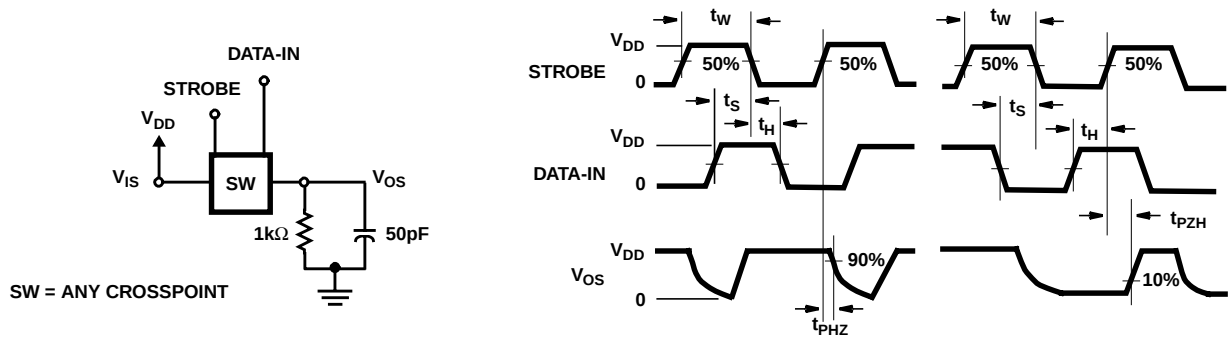


FIGURE 8. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (STROBE TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-OFF)

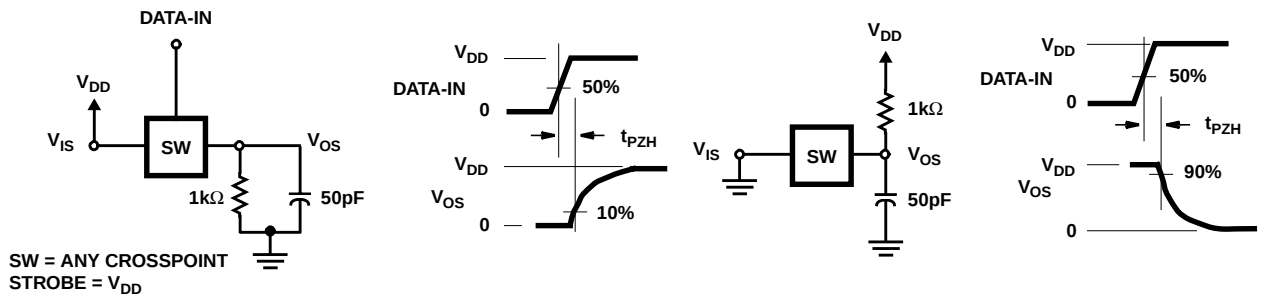


FIGURE 9. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (DATA-IN TO SIGNAL OUTPUT, SWITCH TURN-ON TO HIGH OR LOW LEVEL)

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Test Circuits and Waveforms (Continued)

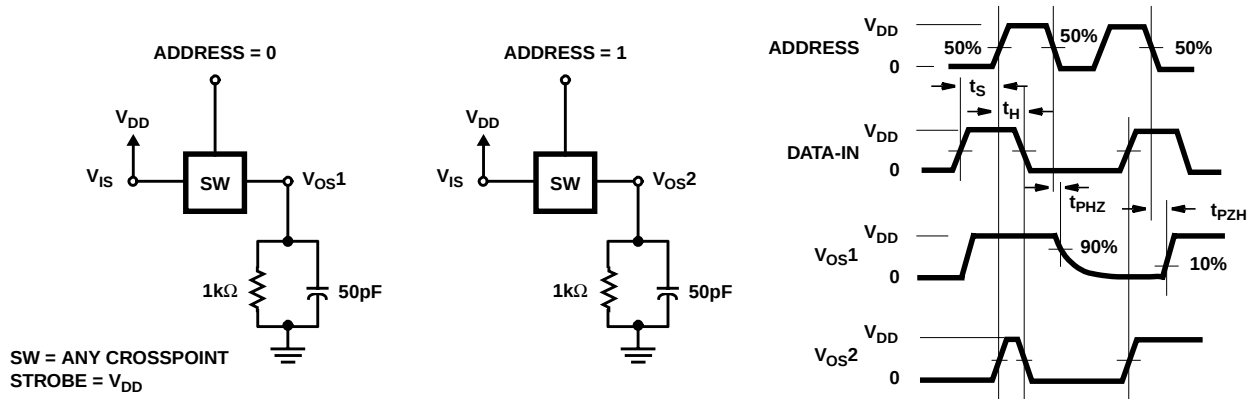


FIGURE 10. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS
(ADDRESS TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-OFF)

Typical Performance Curves

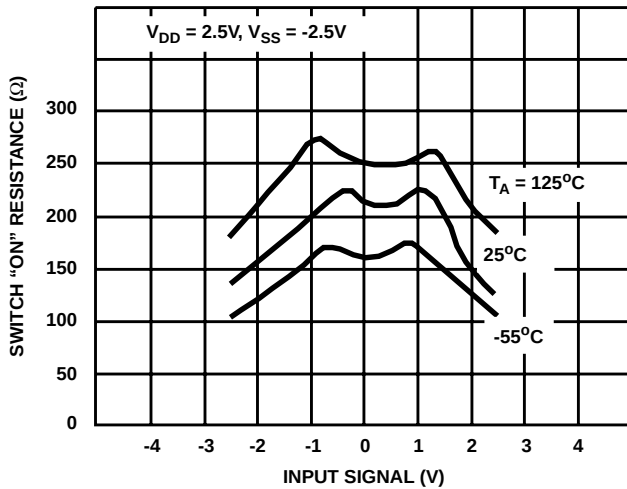


FIGURE 11. TYPICAL ON RESISTANCE AS A FUNCTION OF
INPUT SIGNAL VOLTAGE AT $V_{DD} = -V_{SS} = 2.5V$

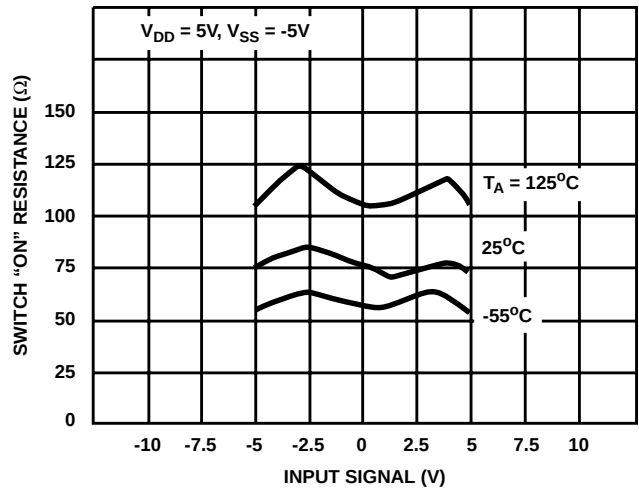


FIGURE 12. TYPICAL ON RESISTANCE AS A FUNCTION OF
INPUT SIGNAL VOLTAGE AT $V_{DD} = -V_{SS} = 5V$

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Typical Performance Curves (Continued)

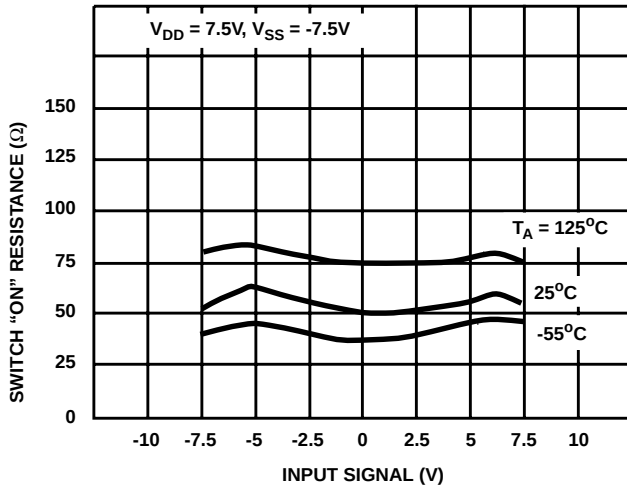


FIGURE 13. TYPICAL ON RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE AT $V_{DD} = -V_{SS} = 7.5V$

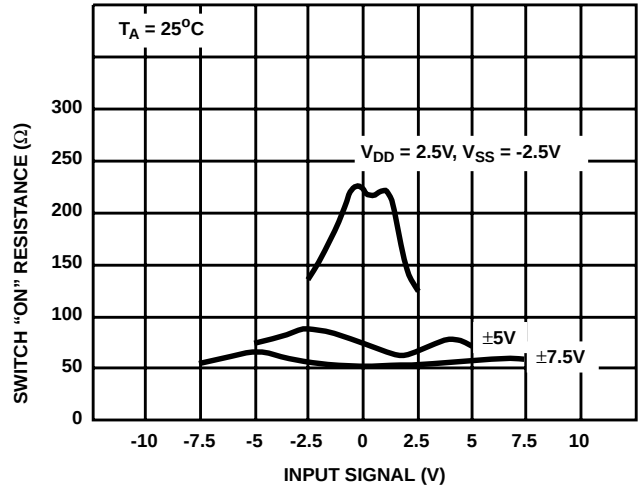


FIGURE 14. TYPICAL ON RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE AT $T_A = 25^\circ C$

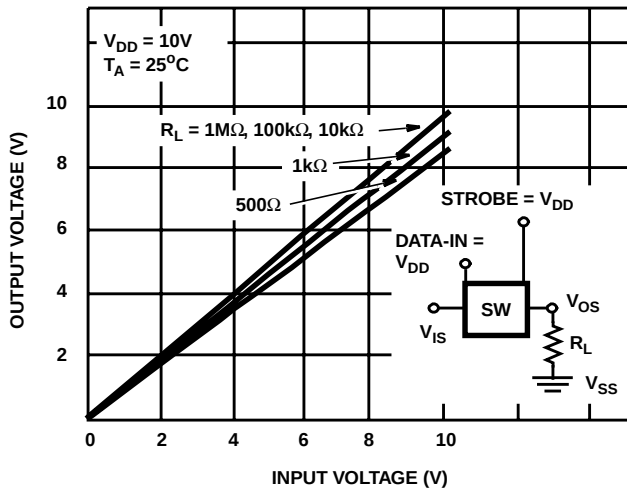


FIGURE 15. TYPICAL SWITCH ON TRANSFER CHARACTERISTICS (1 OF 16 SWITCHES)

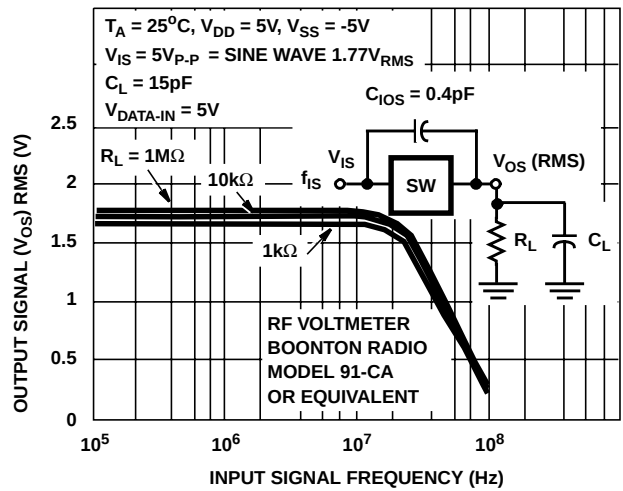


FIGURE 16. TYPICAL SWITCH ON FREQUENCY RESPONSE CHARACTERISTICS