HARRIS Semiconductor

CD22101, CD22102

February 1999

OBSOLETE PRODUCT
NO RECOMMENDED REPLACEMENT
Call Central Applications 1-800-442-7747
or email: centapp@harris.com

CMOS 4 x 4 x 2 Crosspoint Switch with Control Memory

Features

- Low ON Resistance . . . . . 75Ω (Typ) at V_{DD} = 12V
- "Built - In" Latched Inputs
- Large Analog Signal Capability . . . . . $\pm V_{DD}/2$
- Switch Bandwidth 10MHz
- Matched Switch Characteristics
  ΔR_{ON} = 8Ω (Typ) at V_{DD} = 12V
- High Linearity - 0.25% Distortion (Typ) at f = 1kHz, $V_{IN} = 5V_{P-P}$, $V_{DD} - V_{SS}$ = 10V, and R_L = 1kΩ
- Standard CMOS Noise Immunity

Applications

- Telephone Systems
- PBX
- Studio Audio Switching
- Multisystem Bus Interconnect

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD22101E	-40 to 85	24 Ld PDIP	E24.6
CD22101F	-55 to 125	24 Ld CERDIP	F24.6
CD22102E	-40 to 85	24 Ld PDIP	E24.6

Description

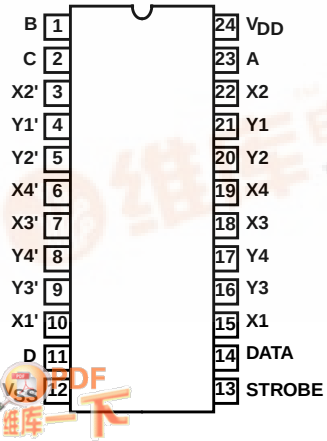
CD22101 and CD22102 crosspoint switches consist of 4 x 4 x 2 arrays of crosspoints (transmission gates) with a 4-line to 16-line decoder and 16 latch circuits. Any one of the sixteen crosspoint pairs can be selected by applying the appropriate four-line address, corresponding crosspoints in each array are turned on and off simultaneously. Any number of crosspoints can be turned on simultaneously.

In the CD22101, the selected crosspoint pair can be turned on or off by applying a logic ONE or ZERO, respectively, to the data input, and applying a ONE to the strobe input. When the device is "powered up", the states of the 16 switches are indeterminate. Therefore, all switches must be turned off by putting the strobe high, data-in low, and then addressing all switches in succession.

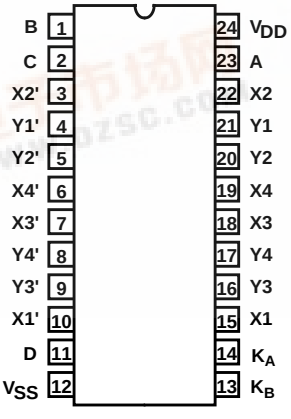
The selected pair of crosspoints in the CD22102 is turned on by applying a logic ONE to the K_A (set) input while a logic ZERO is on the K_B input, and turned off by applying a logic ONE to the K_B (reset) input while a logic ZERO is on the K_A input. In this respect, the control latches of the CD22102 are similar to SET/RESET flip-flops. They differ, however, in that the simultaneous application of ONEs to the K_A and K_B inputs turns off (resets) all crosspoints. All crosspoints in both devices must be turned off as V_{DD} is applied.

Pinouts

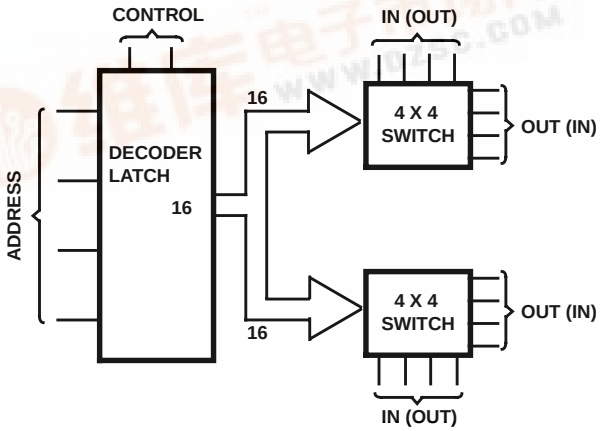
CD22101
(PDIP, SBDIP)
TOP VIEW



CD22102
(PDIP)
TOP VIEW



Functional Diagram



Absolute Maximum Ratings

Supply Voltage (V_{DD}) (Referenced to V_{SS} Terminal) . . . .-0.5 to 20V
Input Voltage (All Inputs) . . . . . -0.5 to V_{DD} +0.5V
Supply Voltage Range
For T_A = Full Package Temperature Range . . . . . 3V to 18V
Input Current (Any One Input) (Note 1) . . . . . ±10mA
Power Dissipation
For T_A = -40°C to 60°C (Package Type E) 500mW
For T_A = 60°C to 85°C
Package Type E) . . . . . Derate Linearly 12mW/°C to 200mW
For T_A = -55°C to 100°C (Package Type D, F) 500mW
For T_A = 100°C to 125°C
(Package Type D, F) . . . . . Derate Linearly 12mW/°C to 200mW
Device Dissipation per Output Transistor
For T_A = Full Package Temperature Range (All Types) 100mW

Thermal Information

Maximum Junction Temperature . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . $-65°C \le T_A \le 150°C$
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

Operating Conditions

Temperature Range
Package Type D, F. . . . . $-55°C \le T_A \le 125°C$
Package Type E. . . . . $-40°C \le T_A \le 85°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Values at -55°C, 25°C, 125°C Apply to D, F, H Packages
Values at -40°C, 25°C, 85°C Apply to E Package

PARAMETER	SYMBOL	TEST CONDITIONS	FIGURE	V_{DD}(V)	-55°C MAX	-40°C MAX	85°C MAX	125°C MAX	25°C MIN	25°C TYP	25°C MAX	UNITS
STATIC CROSSPOINTS												
Quiescent Device Current	I_{DD} (Max)		1	5	5	5	150	150	-	0.04	5	µA
			1	10	10	10	300	300	-	0.04	10	µA
			1	15	20	20	600	600	-	0.04	20	µA
			1	20	100	100	3000	3000	-	0.08	100	µA
On Resistance	R_{ON} (Max)	Any Switch V_{IS} = 0 to V_{DD}	14	5	475	500	725	800	-	225	600	Ω
			15	10	135	145	205	230	-	85	180	Ω
			-	12	100	110	155	175	-	75	135	Ω
			16	15	70	75	110	125	-	65	95	Ω
Δ_{ON} Resistance	ΔR_{ON}	Between Any Two Switches		5	-	-	-	-	-	25	-	Ω
				10	-	-	-	-	-	10	-	Ω
				12	-	-	-	-	-	8	-	Ω
				15	-	-	-	-	-	5	-	Ω
OFF Leakage Current	I_L (Max)	All Switches OFF, V_{IS} = 18V	4	18	±1000				-	±1	±100 (Note 2)	nA
STATIC CONTROLS												
Input Low Voltage	V_{IL} (Max)	OFF Switch I_L < 0.2µA		5	1.5				-	-	1.5	V
				10	3				-	-	3	V
				15	4				-	-	4	V
Input High Voltage	V_{IH} (Min)	ON Switch See R_{ON} Characteristic		5	3.5				3.5	-	-	V
				10	7				7	-	-	V
				15	11				11	-	-	V
Input Current	I_{IN} (Max)	Any Control V_{IN} = 0, 18V	2	18	±0.1	±0.1	±1	±1	-	$\pm 10^{-5}$	±0.1	µA

NOTES:

1. Maximum current through transmission gates (switches) = 25mA.
2. Determined by minimum feasible leakage measurement for automatic testing.

Electrical Specifications $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS					MIN	TYP	MAX	UNITS
		FIGURE	f_{IS} (kHz)	R_L (kΩ)	V_{IS} (V) (Note 3)	V_{DD} (V)				
DYNAMIC CROSSPOINTS										
Propagation Delay Time, (Switch ON) Signal Input to Output	t_{PHL}, t_{PLH}	5	-	-	5	5	-	30	60	ns
			-	10	10	10	-	15	30	ns
					15	15	-	10	20	ns
			C_L = 50pF; t_R , t_F = 20ns							
Frequency Response (Any Switch ON)	f_{3dB}	19	1	1	5	10	-	40	-	MHz
			Sine Wave Input, $20\log\frac{V_{OS}}{V_{IS}}$ = -3dB							
Sine Wave Response (Distortion)	THD	-	1	1	2.5	5	-	1	-	%
			1	1	5	10	-	0.25	-	%
			1	1	7.5	15	-	0.15	-	%
Feedthrough (All Switches OFF)	F_{DT}	13	1.6	0.6	2 (Note 4)	10	-	-96	-	dB
			Sine Wave Input							
Frequency for Signal Crosstalk	F_{CT}	12	-	0.6	1 (Note 4)	10				
Attenuation of 40dB			Sine Wave Input				-	2.5	-	MHz
Attenuation of 95dB								0.1		kHz
Capacitance:										
X_N to Ground	C_{IS}			-	-	-	-	25	-	pF
Y_N to Ground				-	-	-	-	60	-	pF
Feedthrough	C_{IOS}			-	-	-	-	0.6	-	pF
DYNAMIC CONTROLS										
Propagation Delay Time: High Impedance to High Level or Low Level	t_{PZH}, t_{PZL}	6	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	500	1000	ns
Strobe to Output, CD22101						10	-	230	460	ns
						15	-	170	340	ns
Data-In to Output, CD22101	t_{PZH}, t_{PZL}	7	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	515	1000	ns
						10	-	220	440	ns
						15	-	170	340	ns
K_A to Output, CD22102	t_{PZH}, t_{PZL}	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	500	1000	ns
						10	-	215	430	ns
						15	-	160	320	ns
Address to Output CD22101, CD22102	t_{PZH}, t_{PZL}	8	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	480	960	ns
						10	-	225	450	ns
						15	-	155	300	ns

Electrical Specifications $T_A = 25^oC$ **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS					MIN	TYP	MAX	UNITS
		FIGURE	f_{IS} (kHz)	R_L (kΩ)	V_{IS} (V) (Note 3)	V_{DD} (V)				
Propagation Delay Time: High Level or Low Level to High Impedance	t_{PHZ}, t_{PLZ}	6	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	450	900	ns
Strobe to Output, CD22101						10	-	200	400	ns
						15	-	135	270	ns
K_B to Output, CD22102	t_{PHZ}, t_{PLZ}	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	450	900	ns
						10	-	200	400	ns
						15	-	130	260	ns
Data-In to Output, CD22101	t_{PHZ}, t_{PLZ}	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	450	900	ns
						10	-	165	330	ns
						15	-	110	220	ns
$K_A \bullet K_B$ to Output, CD22102	t_{PHZ}, t_{PLZ}	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	280	560	ns
						10	-	130	260	ns
						15	-	90	180	ns
Address to Output CD22101, CD22102	t_{PHZ}, t_{PLZ}	8	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	425	850	ns
						10	-	190	380	ns
						15	-	130	260	ns
Minimum Strobe Pulse Width, CD22101	t_W	6	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	260	500	ns
						10	-	120	240	ns
						15	-	80	160	ns
Address to Strobe Setup or Hold Times, CD22101	t_{SU}, t_H	9	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	-160	0	ns
						10	-	-70	0	ns
						15	-	-50	0	ns
Strobe to Data-In Hold Time, CD22101	t_{HHL}, t_{HLH}	10	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	200	400	ns
						10	-	80	160	ns
						15	-	60	120	ns
Address to K_A and K_B Setup or Hold Times, CD22102	t_{SU}, t_H	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	-160	0	ns
						10	-	-70	0	ns
						15	-	-50	0	ns
Minimum $K_A \bullet K_B$ Pulse Width, CD22102	t_W	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	375	750	ns
						10	-	160	320	ns
						15	-	110	220	ns
Minimum K_A Pulse Width, CD22102	t_W	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	425	850	ns
						10	-	175	350	ns
						15	-	120	240	ns

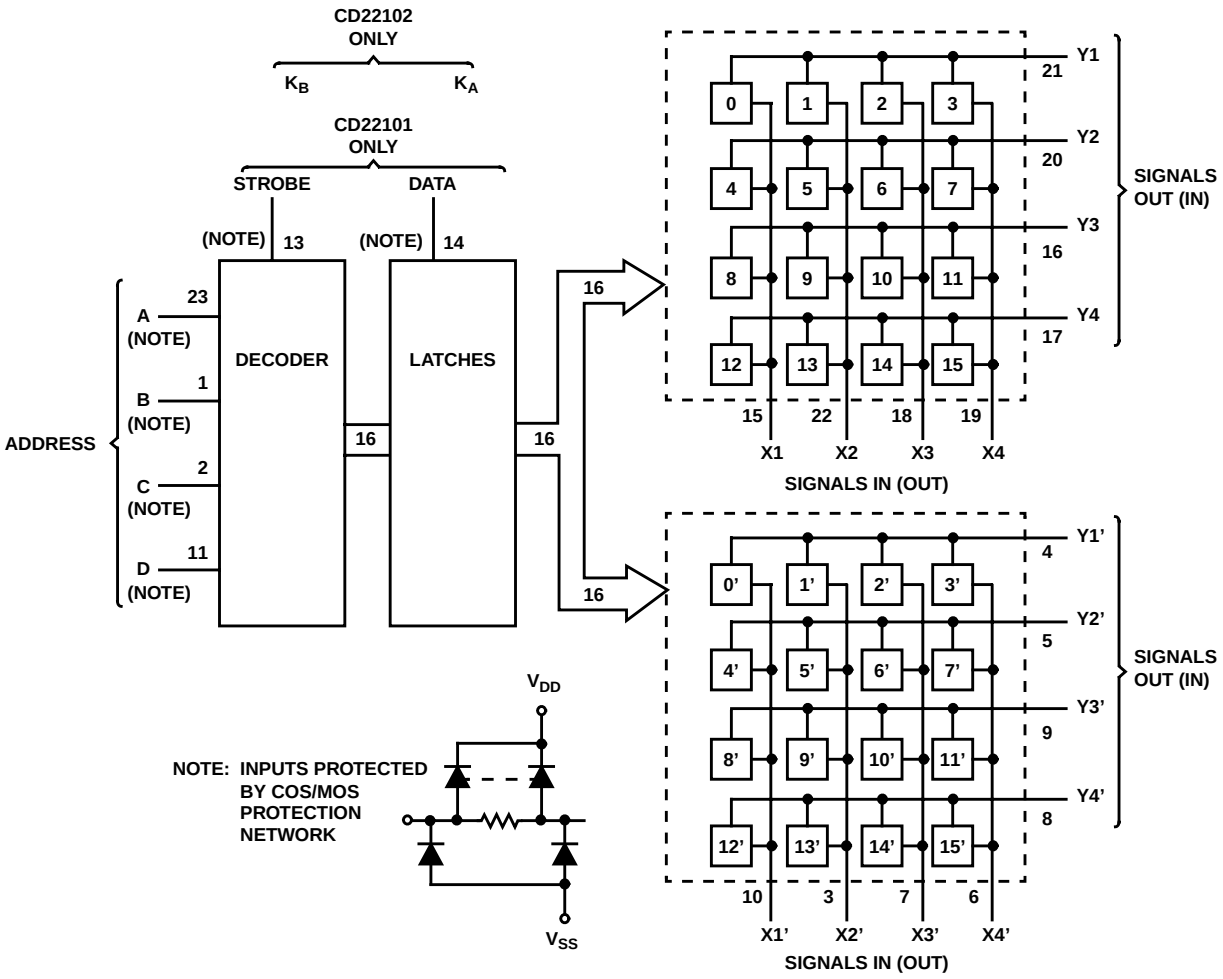
Electrical Specifications $T_A = 25^oC$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS FIGURE	f_{IS} (kHz)	R_L (kΩ)	V_{IS} (V) (Note 3)	V_{DD} (V)	MIN	TYP	MAX	UNITS
Minimum K_B Pulse Width, CD22102	t_W	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	200	400	ns
						10	-	90	180	ns
						15	-	70	140	ns
Control Crosstalk, Data-In, Address or Strobe to Output		11	100	10		5	-	75	-	mV_{PEAK}
			Square Wave Input = 5V, t_R, t_F = 20ns, R_S = 1kΩ							
Input Capacitance	C_{IN}		Any Control Input			-	-	5	7.5	pF

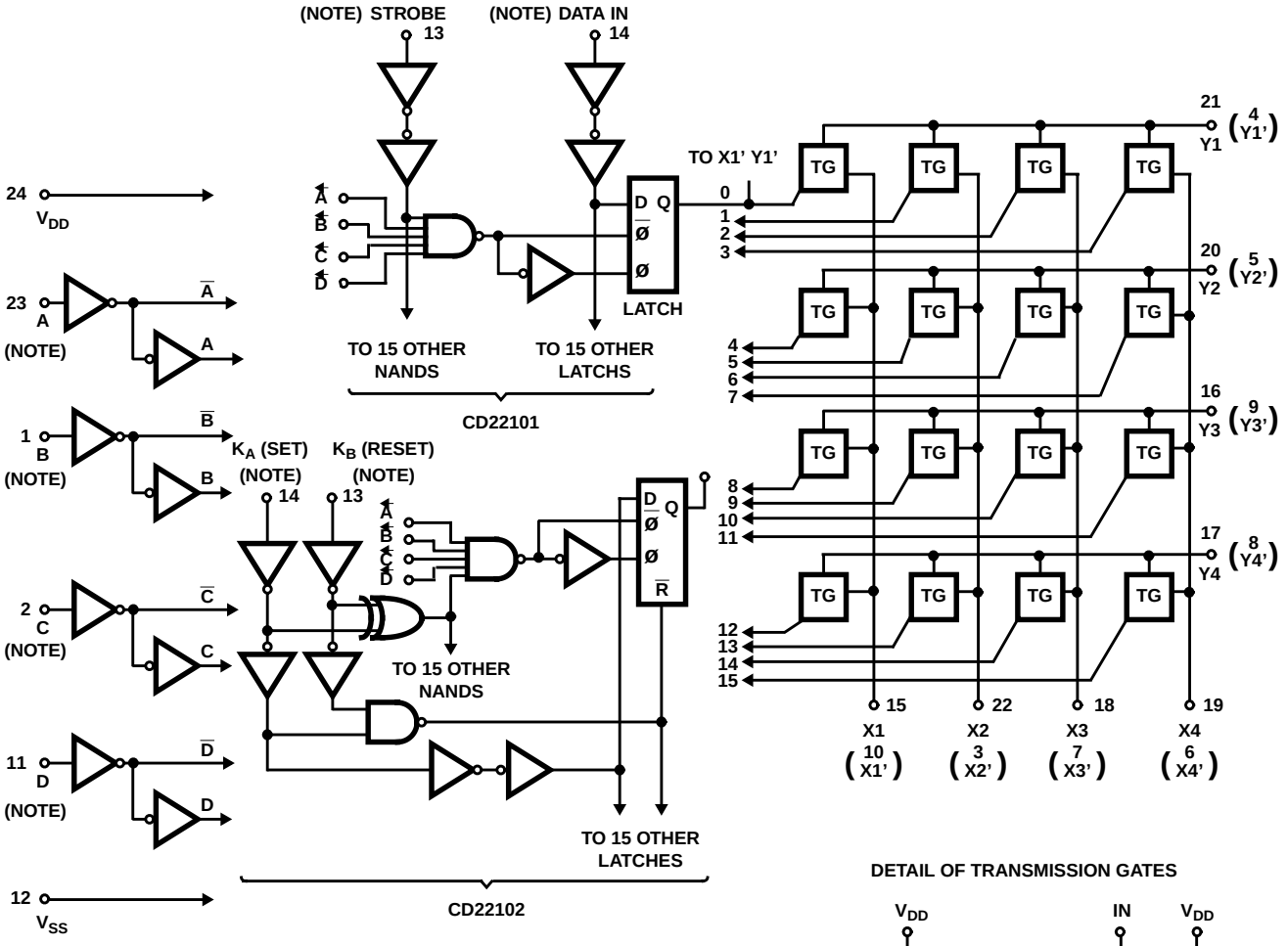
NOTES:

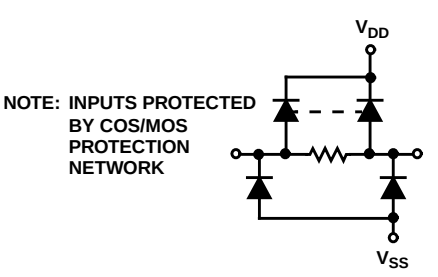
3. Peak-to-peak voltage symmetrical about $\frac{V_{DD}}{2}$, unless otherwise specified.
4. RMS.

Functional Block Diagram

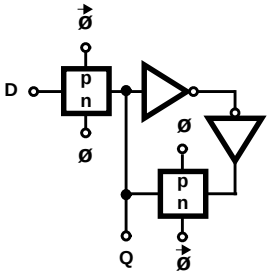


Schematic Diagram

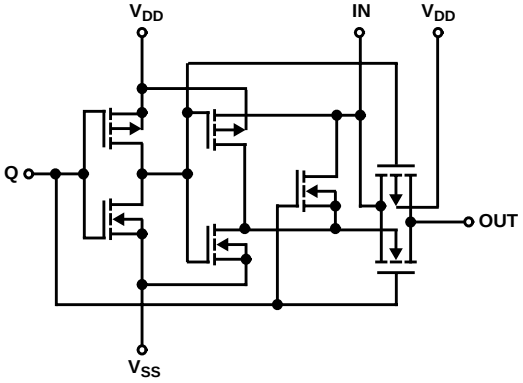




DETAIL OF LATCHES



DETAIL OF TRANSMISSION GATES



DECODER TRUTH TABLE

ADDRESS					ADDRESS				
A	B	C	D	SELECT	A	B	C	D	SELECT
0	0	0	0	X1Y1 and X1'Y1'	0	0	0	1	X1Y3 and X1'Y3'
1	0	0	0	X2Y1 and X2'Y1'	1	0	0	1	X2Y3 and X2'Y3'
0	1	0	0	X3Y1 and X3'Y1'	0	1	0	1	X3Y3 and X3'Y3'
1	1	0	0	X4Y1 and X4'Y1'	1	1	0	1	X4Y3 and X4'Y3'
0	0	1	0	X1Y2 and X1'Y2'	0	0	1	1	X1Y4 and X1'Y4'
1	0	1	0	X2Y2 and X2'Y2'	1	0	1	1	X2Y4 and X2'Y4'
0	1	1	0	X3Y2 and X3'Y2'	0	1	1	1	X3Y4 and X3'Y4'
1	1	1	0	X4Y2 and X4'Y2'	1	1	1	1	X4Y4 and X4'Y4'

CONTROL TRUTH TABLE FOR CD22101

FUNCTION	ADDRESS A	B	C	D	STROBE	DATA	SELECT
Switch ON	1	1	1	1	1	1	15 (X4Y4) and 15' (X4'Y4')
Switch OFF	1	1	1	1	1	0	15 (X4Y4) and 15' (X4'Y4')
No Change	X	X	X	X	0	X	X X X X

1 = High Level 0 = Low Level X = Don't Care

CONTROL TRUTH TABLE FOR CD22102

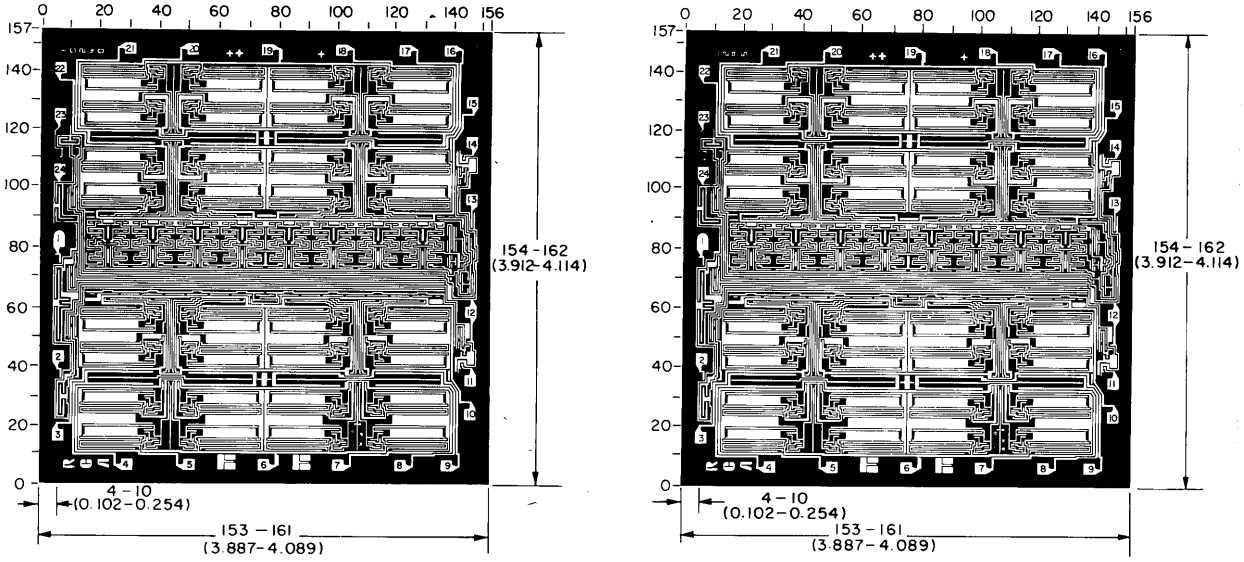
FUNCTION	ADDRESS A	B	C	D	K_A	K_B	SELECT
Switch ON	1	1	1	1	1	0	15 (X4Y4) and 15' (X4'Y4')
Switch OFF	1	1	1	1	0	1	15 (X4Y4) and 15' (X4'Y4')
All Switches OFF (Note 5)	X	X	X	X	1	1	All
No Change	X	X	X	X	0	0	X X X X

1 = High Level 0 = Low Level X = Don't Care

NOTE:

5. In the event that K_A and K_B are changed from levels 1, 1 to 0, 0 K_B should not be allowed to go to 0 before K_A, otherwise a switch which was off will inadvertently be turned on.

Metallization Mask Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Test Circuits and Waveforms

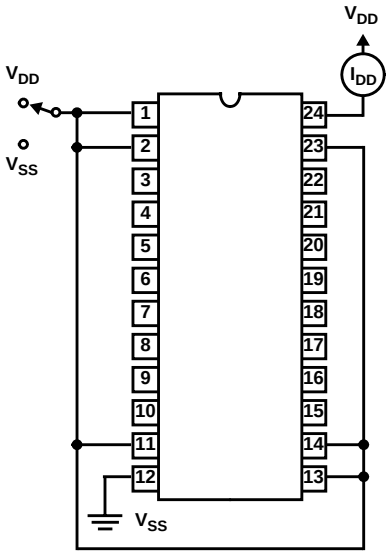
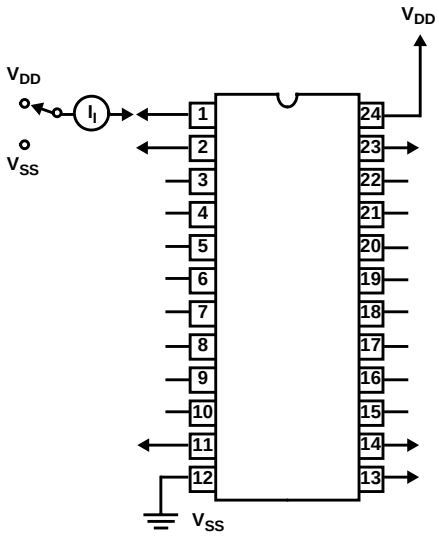
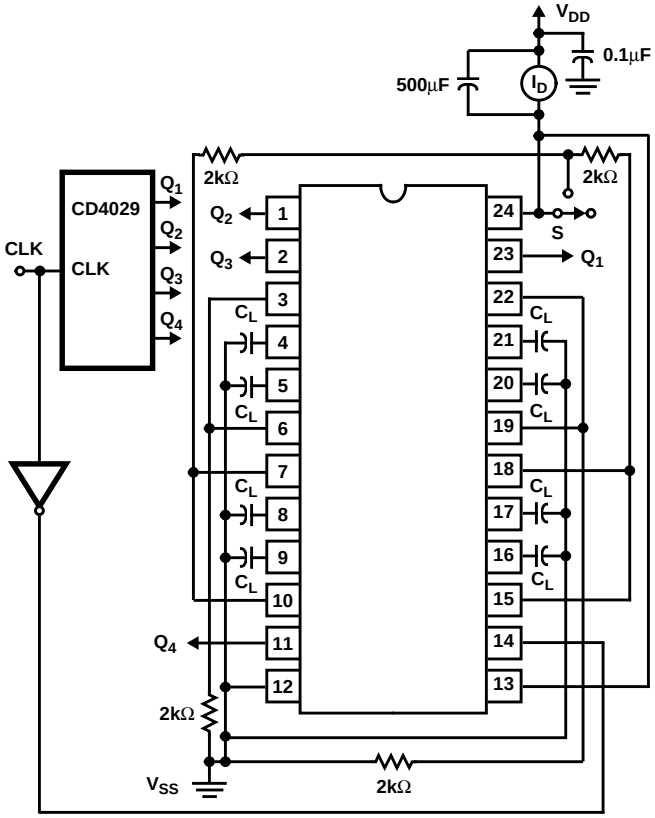


FIGURE 1. QUIESCENT CURRENT TEST CIRCUIT



MEASURE INPUTS SEQUENTIALLY TO BOTH V_{DD} AND V_{SS}
CONNECT ALL UNUSED INPUTS TO EITHER V_{DD} OR V_{SS}

FIGURE 2. INPUT CURRENT TEST CIRCUIT



CLOSE SWITCH S AFTER APPLYING V_{DD}

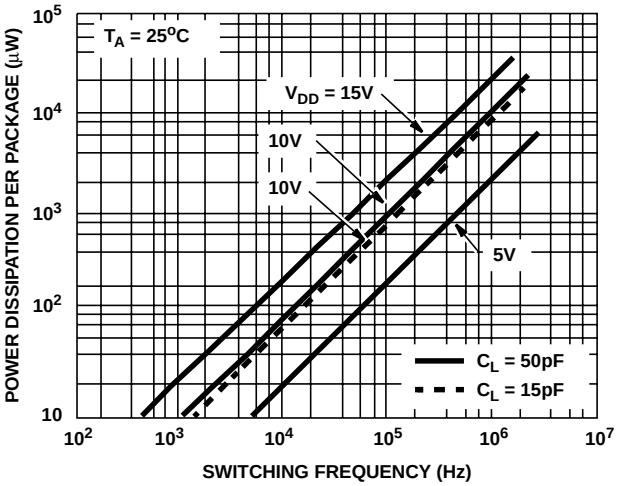


FIGURE 3. DYNAMIC POWER DISSIPATION TEST CIRCUIT FOR CD22101AND TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF SWITCHING FREQUENCY

Test Circuits and Waveforms (Continued)

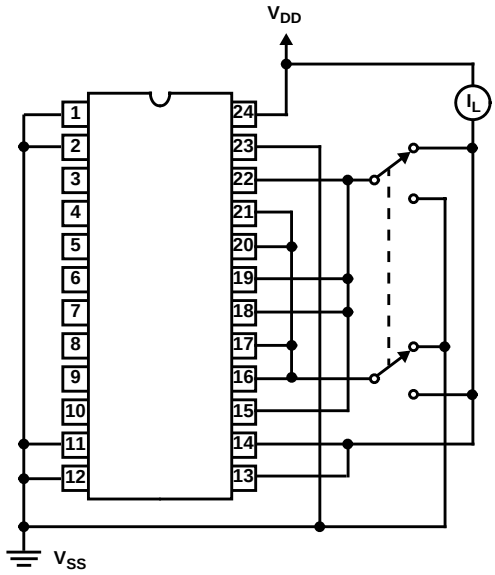


FIGURE 4. OFF SWITCH INPUT OR OUTPUT LEAKAGE CURRENT TEST CIRCUIT (16 OF 32 SWITCHES)

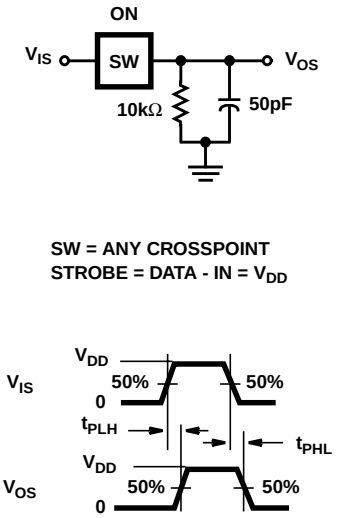
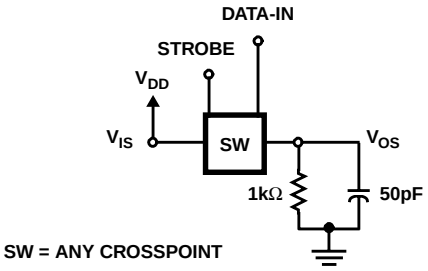


FIGURE 5. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (SIGNAL INPUT TO SIGNAL OUTPUT, SWITCH ON)



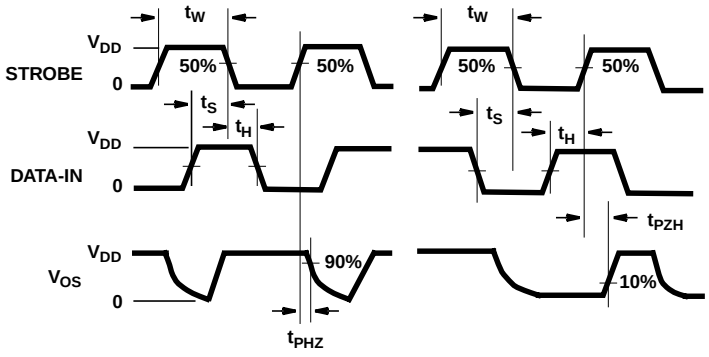


FIGURE 6. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (STROBE TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-OFF)

Test Circuits and Waveforms (Continued)

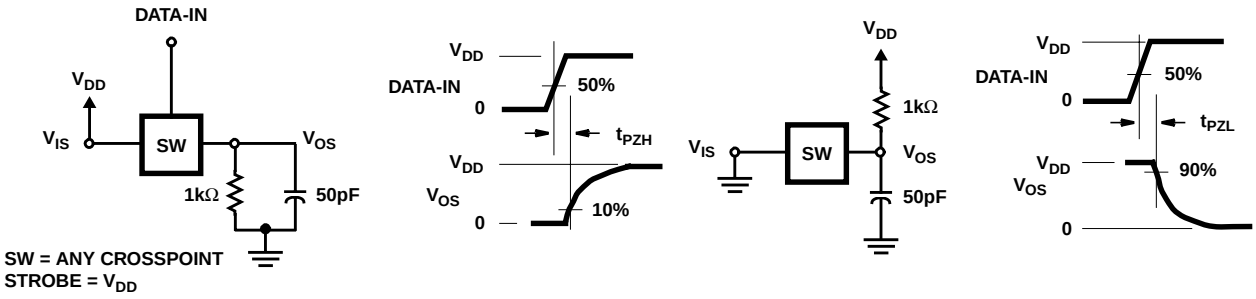


FIGURE 7. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (DATA-IN TO SIGNAL OUTPUT, SWITCH TURN-ON TO HIGH OR LOW LEVEL)

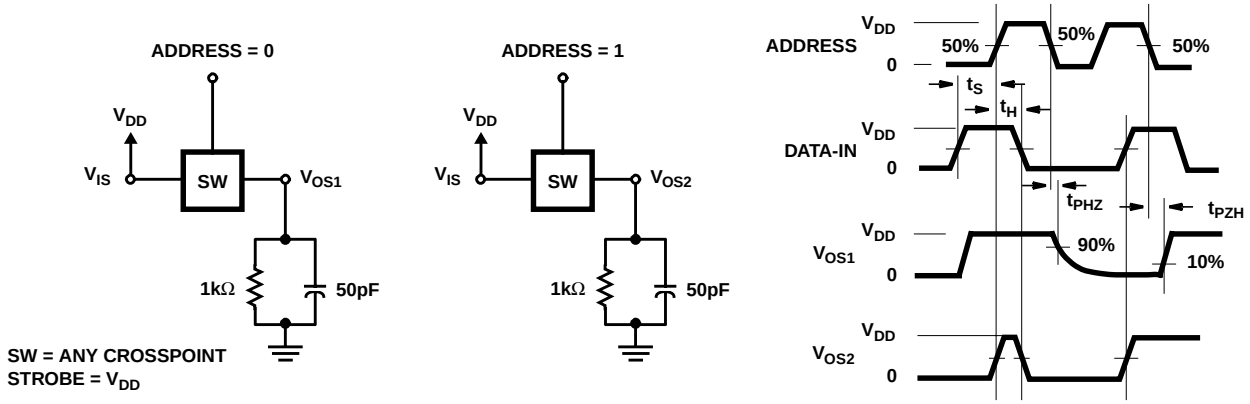
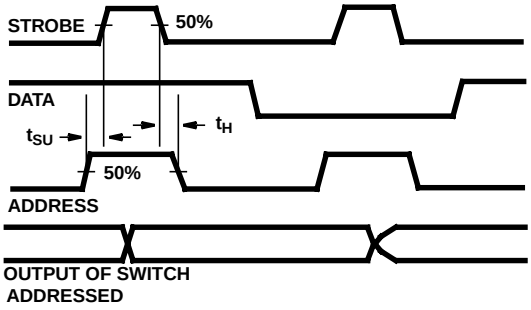


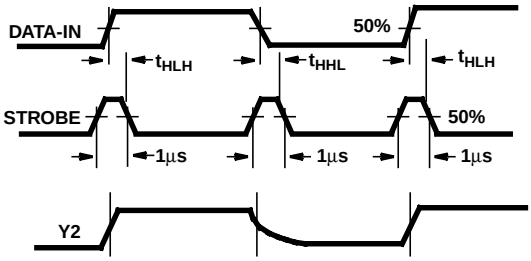
FIGURE 8. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (ADDRESS TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-OFF)

Test Circuits and Waveforms (Continued)



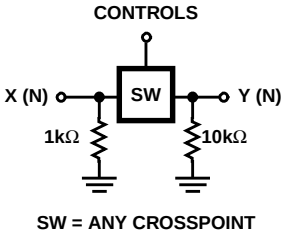
IF SETUP AND HOLD TIMES PROVIDED ARE TOO SHORT, AN UNADDRESSED SWITCH MAY BE TURNED ON OR OFF SIMULTANEOUSLY WITH THE ADDRESSED SWITCH

FIGURE 9. ADDRESS TO STROBE SETUP AND HOLD TIMES



SET ALL SWITCHES TO OFF INITIALLY APPLY VDD TO ALL X INPUTS AND RETURN ALL Y OUTPUTS TO VSS THROUGH 1kΩ. ADDRESS X1Y2 (ABCD) WITH f_{IN} = 10kHz

FIGURE 10. STROBE TO DATA-IN HOLD TIME t_H, FOR CD22101



SW = ANY CROSSPOINT

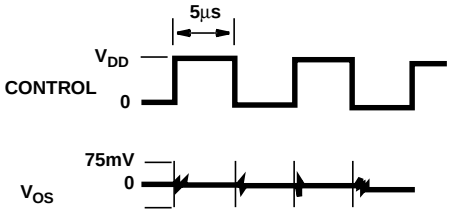
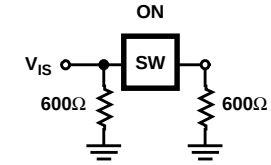
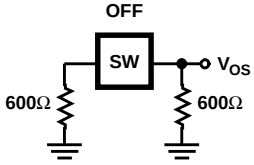


FIGURE 11. TEST CIRCUIT AND WAVEFORMS FOR CROSSTALK (CONTROL INPUT TO SIGNAL OUTPUT)



SW = ANY CROSSPOINT



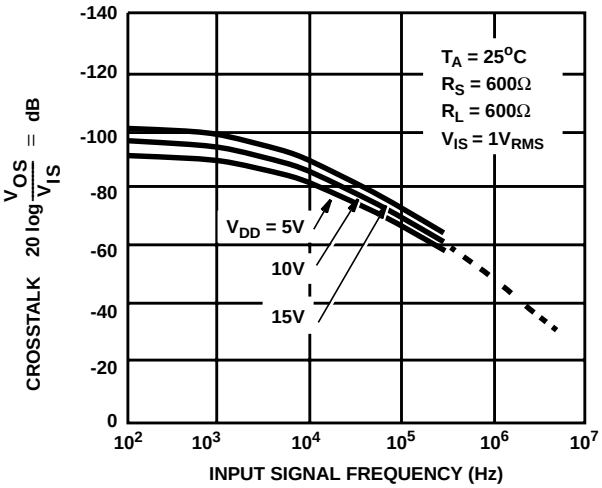
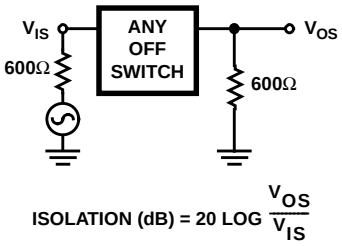


FIGURE 12. TEST CIRCUIT AND TYPICAL CROSSTALK AS A FUNCTION OF FREQUENCY BETWEEN SWITCH CIRCUITS IN THE SAME PACKAGE

Test Circuits and Waveforms (Continued)



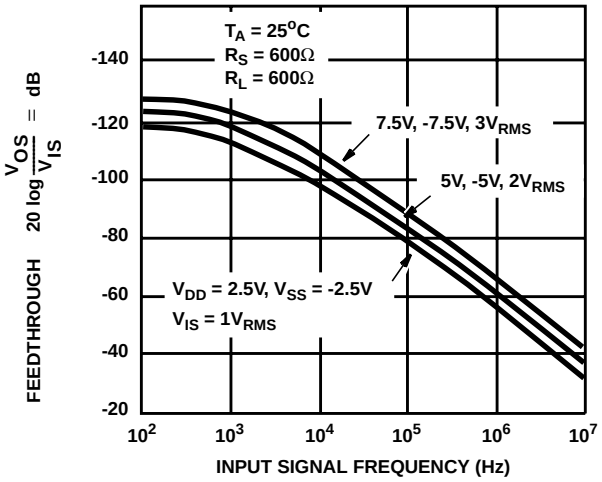


FIGURE 13. TEST CIRCUIT AND TYPICAL FEEDTHROUGH AS A FUNCTION OF FREQUENCY (ANY OFF SWITCH)

Typical Performance Curves

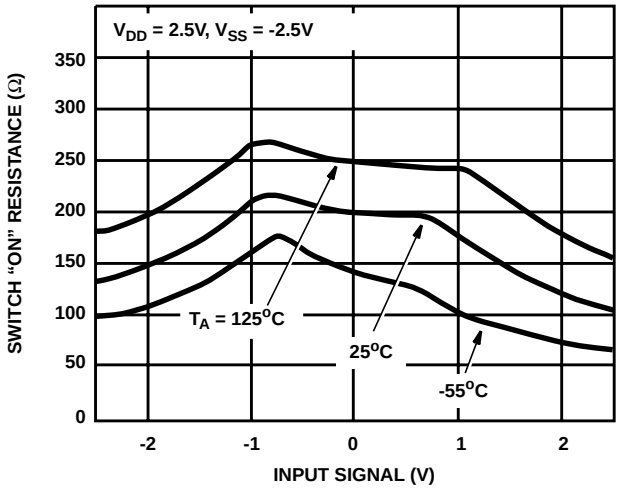


FIGURE 14. TYPICAL ON RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE AT $V_{DD} = -V_{SS} = 2.5V$

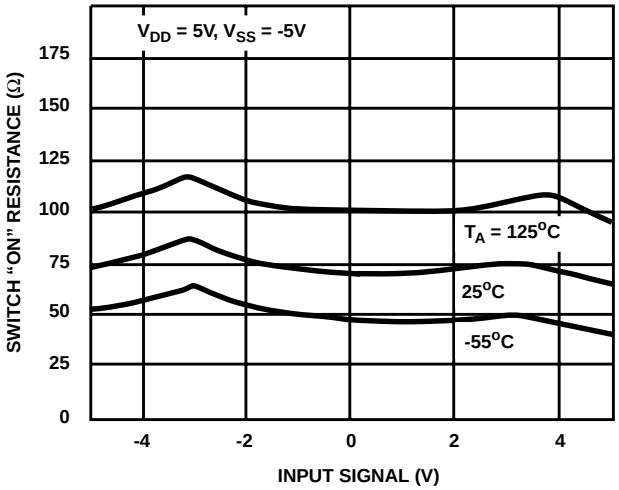


FIGURE 15. TYPICAL ON RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE AT $V_{DD} = -V_{SS} = 5V$

Typical Performance Curves (Continued)

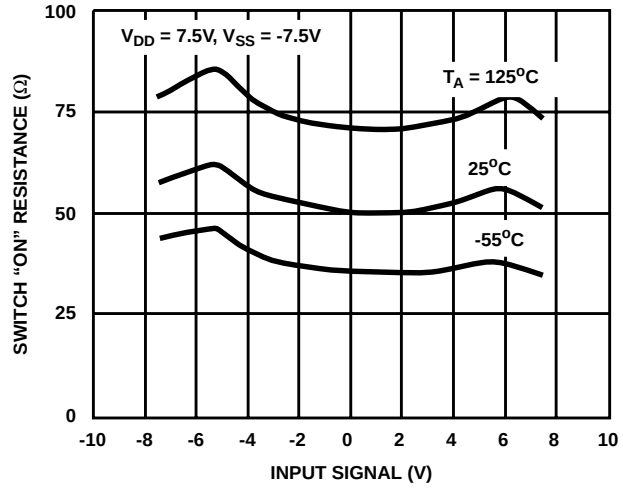


FIGURE 16. TYPICAL ON RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE AT V_{DD} = -V_{SS} = 7.5V

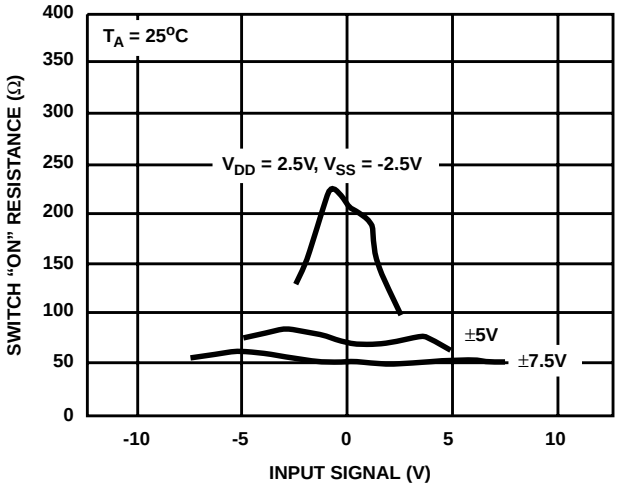


FIGURE 17. TYPICAL ON RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE AT T_A = 25°C

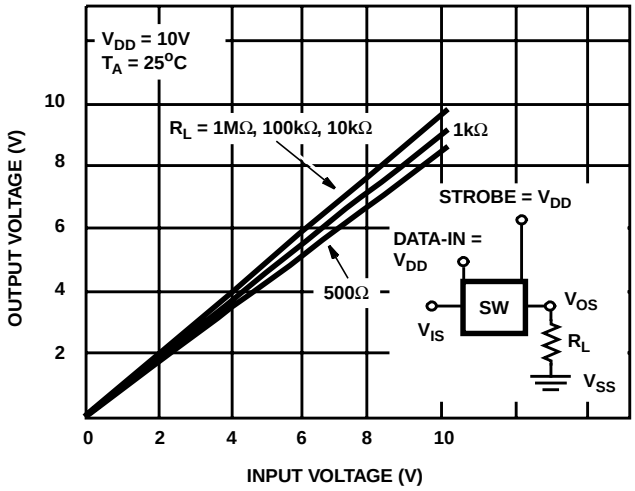


FIGURE 18. TYPICAL SWITCH ON TRANSFER CHARACTERISTICS (1 OF 16 SWITCHES)

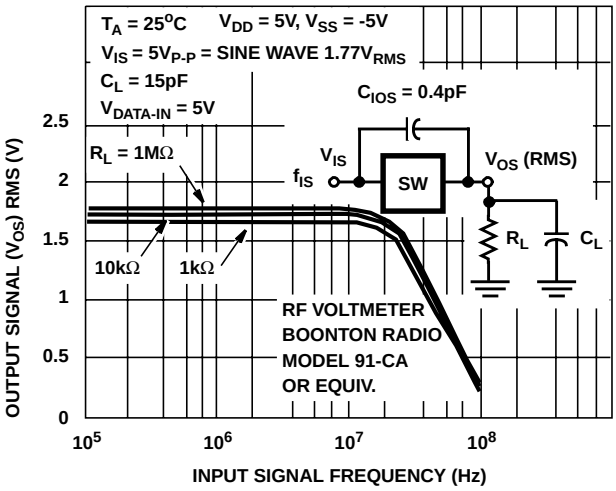


FIGURE 19. TYPICAL SWITCH ON FREQUENCY RESPONSE CHARACTERISTICS