

March 1988

CD4002M/CD4002C Dual 4-Input NOR Gate CD4012M/CD4012C Dual 4-Input NAND Gate

General Description

These NOR and NAND gates are monolithic complementary MOS (CMOS) integrated circuits. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

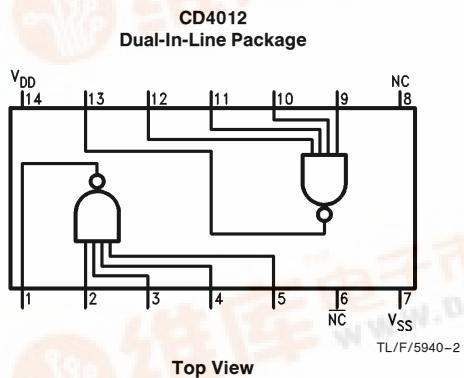
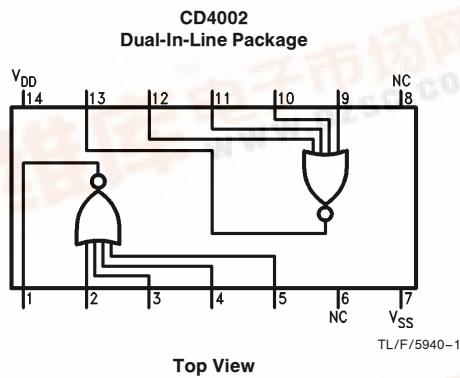
Features

- Wide supply voltage range 3.0V to 15V
- Low power 10 nW (typ.)
- High noise immunity 0.45 V_{DD} (typ.)

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical Electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

Connection Diagrams



Order Number CD4002 or CD4012

**CD4002M/CD4002C Dual 4-Input NOR Gate
CD4012M/CD4012C Dual 4-Input NAND Gate**

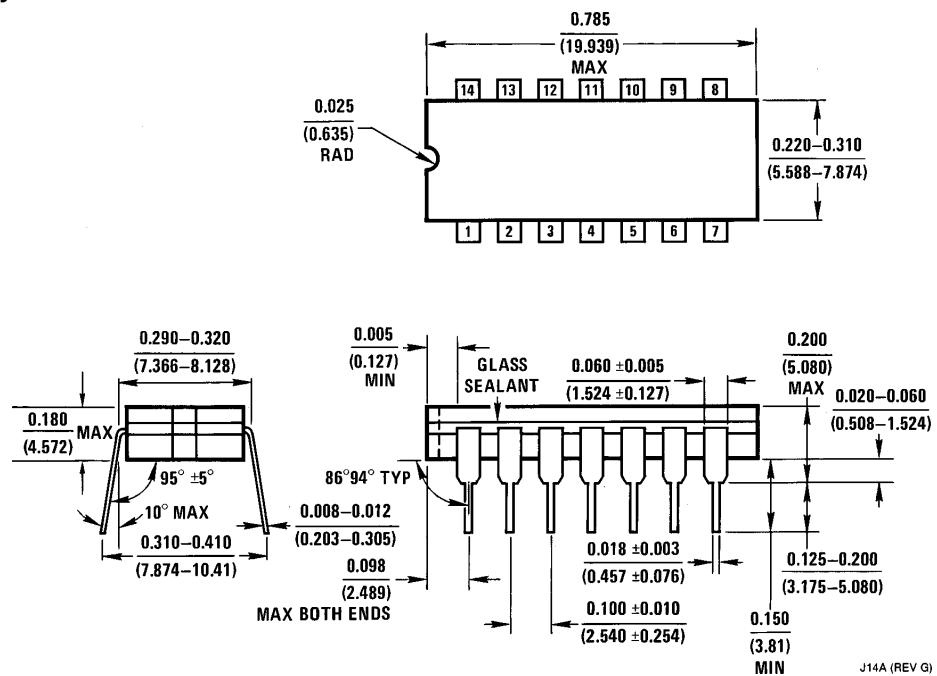
DC Electrical Characteristics CD4002C, CD4012C

Symbol	Parameter	Conditions	Limits						Units	
			−55°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
I _{DD}	Quiescent Device Current	V _{DD} = 5.0V V _{DD} = 10V		0.5 5.0		0.005 0.005	0.5 5.0		15 30	μA μA
P _D	Quiescent Device Dissipation/Package	V _{DD} = 5.0V V _{DD} = 10V		2.5 50		0.025 0.05	2.5 50		75 300	μW μW
V _{OL}	Output Voltage Low Level	V _{DD} = 5.0V, V _I = V _{DD} , I _O = 0A V _{DD} = 10V, V _I = V _{DD} , I _O = 0A		0.05 0.05		0 0	0.05 0.05		0.05 0.05	V V
V _{OH}	Output Voltage High Level	V _{DD} = 5.0V, V _I = V _{SS} , I _O = 0A V _{DD} = 10V, V _I = V _{SS} , I _O = 0A	4.95 9.95		4.95 9.95	5.0 10		4.95 9.95		V V
V _{NL}	Noise Immunity (All Inputs)	V _{DD} = 5.0V, V _O ≥ 3.6V, I _O = 0A V _{DD} = 10V, V _O ≥ 7.2V, I _O = 0A	1.5 3.0		1.5 3.0	2.25 4.5		1.4 2.9		V V
V _{NH}	Noise Immunity (All Inputs)	V _{DD} = 5.0V, V _O ≤ 0.95V, I _O = 0A V _{DD} = 10V, V _O ≤ 2.9V, I _O = 0A	1.4 2.9		1.5 3.0	2.25 4.5		1.5 3.0		V V
I _{DN}	Output Drive Current N-Channel (4002) (Note 2)	V _{DD} = 5.0V, V _O = 0.4V, V _I = V _{DD} V _{DD} = 10V, V _O = 0.5V, V _I = V _{DD}	0.35 0.72		0.3 0.6	1.0 2.5		0.24 0.48		mA mA
I _{DN}	Output Drive Current N-Channel (4012) (Note 2)	V _{DD} = 5.0V, V _O = 0.4V, V _I = V _{DD} V _{DD} = 10V, V _O = 0.5V, V _I = V _{DD}	0.145 0.3		0.12 0.25	0.5 0.6		0.095 0.2		mA mA
I _{DP}	Output Drive Current P-Channel (4002) (Note 2)	V _{DD} = 5.0V, V _O = 2.5V, V _I = V _{SS} V _{DD} = 10V, V _O = 9.5V, V _I = V _{SS}	−0.35 −0.3		−0.3 −0.25	−2.0 −1.0		−0.24 −0.2		mA mA
I _{DP}	Output Drive Current P-Channel (4012) (Note 2)	V _{DD} = 5.0V, V _O = 2.5V, V _I = V _{SS} V _{DD} = 10V, V _O = 9.5V, V _I = V _{SS}	−0.145 −0.35		−0.12 −0.3	−0.5 −1.2		−0.095 −0.24		mA mA
I _I	Input Current					10				pA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: I_{DN} and I_{DP} are tested one output at a time.

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)

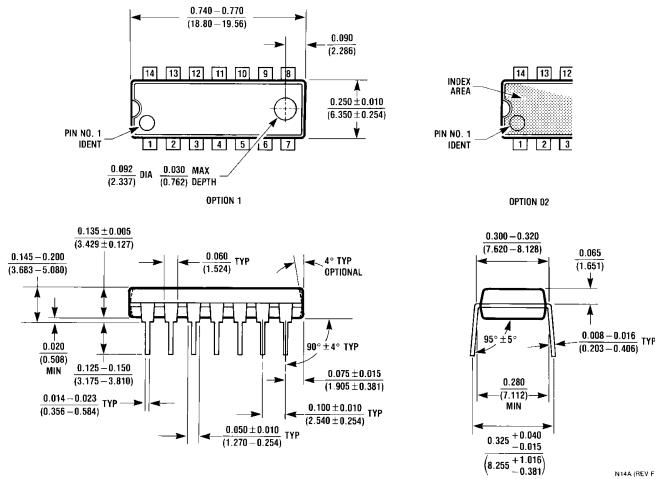
Order Number CD4002MJ, CD4002CJ, CD4012MJ or CD4012CJ

NS Package Number J14A

J14A (REV G)

**CD4002M/CD4002C Dual 4-Input NOR Gate
CD4012M/CD4012C Dual 4-Input NAND Gate**

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number CD4002MN, CD4002CN, CD4012MN or CD4012CN
NS Package Number N14A

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