



HARRIS

CD40116 Types

CMOS High-Speed 8-Bit Bidirectional CMOS/TTL Interface Level Converter

Features:

- Eight inverting channels with conversion from V_{DD} to V_{CC} or V_{CC} to V_{DD}
($4\text{ V} \leq V_{DD} \leq 12\text{ V}$ and $4\text{ V} \leq V_{CC} \leq V_{DD}$)
- Three operating modes:
CMOS-to-TTL level conversion
TTL-to-CMOS level conversion
Interface off; high-impedance on both sides

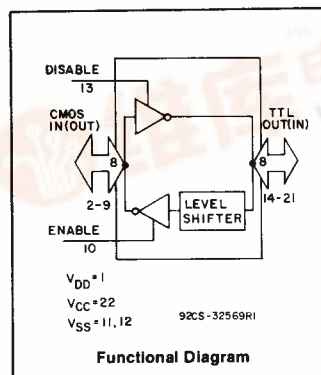
CD40116 is a high-speed 8-bit integrated circuit designed to interface CMOS logic levels with TTL logic levels on the data bus of microprocessor-based systems. CMOS/TTL interface is provided by eight parallel bidirectional buffer/level converters. Buffer INPUT/OUTPUT terminals are either inputs or outputs depending on the desired direction of data flow.

A low level on the DISABLE input with the ENABLE input either high or low, permits conversion of CMOS inputs to TTL outputs. A high level on both the DISABLE and ENABLE inputs permits data flow from TTL inputs to CMOS outputs. A low level on the ENABLE input and a high level on the DISABLE input sets both inputs/outputs to the high-impedance state.

The TTL Input/Output terminals and the ENABLE and DISABLE control inputs are TTL-compatible without the use of external pull-up resistors. The TTL input logic 0 to logic 1 transition occurs at a level of approximately 1.5 volts. The ENABLE and DISABLE inputs may be driven to the V_{DD} rail; therefore, either TTL or CMOS logic drivers, capable of sinking one TTL load, may be used to determine the direction of data flow. The large CMOS and TTL output buffers in this device have high output sink and source current capability and can drive the data bus capacitance with a transition time of approximately 0.25 ns/pF. This fast output transition time, together with the small propagation delay time of the device, allow high-speed operation.

Pin 12 is an additional V_{SS} Pin which is connected directly to the TTL-to-CMOS converters to avoid oscillation in these amplifiers. Pin 12 is connected to Pin 11 through a poly resistor which isolated Pin 12 from V_{SS} switching noise (ground noise).

The CD40116 is supplied in a 22-lead hermetic dual-in-line ceramic package (D suffix), 22-lead plastic package (E suffix), and in chip form (H suffix).

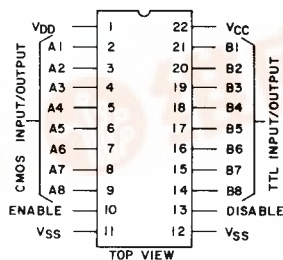


Functional Diagram

- Low propagation delay time:
CMOS-to-TTL conversion - 25 ns typ.
TTL-to-CMOS conversion - 30 ns typ.
($V_{DD} = 12\text{ V}$, $V_{CC} = 5\text{ V}$)
- High TTL sink current - 11 mA typ.
- No external TTL input pull-up resistors required
- High speed drive of large data bus capacitances
- Input/output and power supply terminals located for ease of PC board layout

Applications:

- Interface CMOS microprocessor with TTL memories and peripheral devices
- Interface between and within logic systems which combine CMOS and TTL devices



92CS-30245

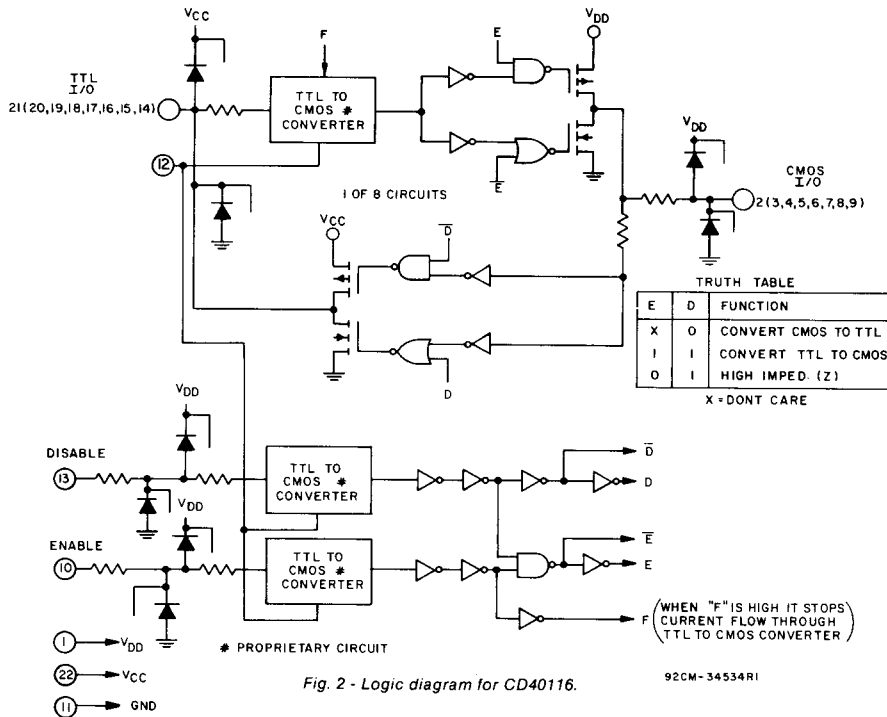
TERMINAL ASSIGNMENT



4
COMMERCIAL CMOS
SPECIAL FUNCTION ICs

See Operating and Handling Considerations — Bypassing and

CD40116 Types



92CM-34534R1

STATIC CHARACTERISTICS $V_{DD} = 12\text{ V}$, $V_{CC} = 5\text{ V}$

CHARACTERISTIC	TEST CONDITIONS	Limits at Indicated Temperatures (°C)							UNITS
		Values at -55, +25, +125 for D, H Packages							
		Values at -40, +25, +85 for E Packages							
		+25							
		-55	-40	+85	+125	MIN.	TYP.	MAX.	
Quiescent Device Current, From V _{DD} Supply, I _{DD} MAX From V _{CC} Supply, I _{CC} MAX	ENABLE = 1	5	5	5	5	—	1	5	mA
	ENABLE = 0	5	5	5	5	—	0.2	5	
		100	100	200	200	—	5	100	μA
Data Flow — CMOS Inputs to TTL Outputs									
Input Current, I _{IN} MAX	V _{IN} = 0, 12 V; Any CMOS input	±60	±60	±60	±60	—	±5	±60	μA
Output Current, I _{OH} MIN I _{OL} MIN	V _{OH} = 3 V, V _{IL} = 2 V	-7.5	-7	-4.9	-4.2	-6	-12	—	mA
	V _{OL} = 0.4 V, V _{IH} = 10 V	7.5	7	4.9	4.2	6	11	—	
TTL 3-State Output Leakage Current I _{OUT} MAX	ENABLE = 1	-500	-500	-500	-500	—	-250	-500	μA
	ENABLE = 0	±100	±100	±100	±100	—	±5	±100	μA
Data Flow — TTL Inputs to CMOS Outputs									
Input Current, I _{IL} MAX I _{IH} MAX I _{IH} MAX	V _{IL} = 0 to 0.7 V; V _{IH} = 2.3 V;	-500	-500	-500	-500	—	-250	-500	μA
	V _{IH} = 5 V;	-450	-350	-350	-350	—	-175	-350	
	Any TTL input	+100	+100	+100	+100	—	+50	+100	
Output Current, I _{OH} MIN I _{OL} MIN	V _{OH} = 11.5 V, V _{IL} = 0.7 V	-4.3	-4.2	-2.9	-2.5	-3.5	-6.5	—	mA
	V _{OL} = 0.5 V, V _{IH} = 2.3 V	4.3	4.2	2.9	2.5	3.5	6.5	—	
CMOS 3-State Output Leakage Current I _{OUT} MAX	V _O = 0, 12 V, V _{IN} = 0.5 V	±60	±60	±60	±60	—	±5	±60	μA
Enable and Disable Inputs									
Input Current, I _{IL} MAX I _{IH} MAX I _{IH} MAX	V _{IL} = 0 to 0.7 V V _{IH} = 2.3 (TTL)	-500	-500	-500	-500	—	-250	-500	μA
		-450	-350	-350	-350	—	-175	-350	
	V _{IH} = 12 V (CMOS)	60	60	60	60	—	5	60	

CD40116 Types

DYNAMIC ELECTRICAL CHARACTERISTICS AT $T_A = 25^\circ\text{C}$; $V_{DD} = 12\text{ V}$, $V_{CC} = 5\text{ V}$

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
	INPUT	OUTPUT	$C_L = 50\text{ pF}$		$C_L = 200\text{ pF}$	
Propagation Delay Times, Data-In to Data-Out, t_{PHL} , t_{PLH}	CMOS	TTL	TYP	MAX	TYP	ns
	TTL	CMOS	25 30	35 45	35 50	
Disable to TTL Out, $t_{PHZ/LZ}$ $t_{PZH/ZL}$			30 35	45 45	30 35	ns
Enable to CMOS Out, $t_{PHZ/LZ}$ $t_{PZH/ZL}$			30 30	50 50	20 45	ns
Transition Time, t_{THL} , t_{TLH}	CMOS	TTL	20	30	55	ns
	TTL	CMOS	20	30	55	

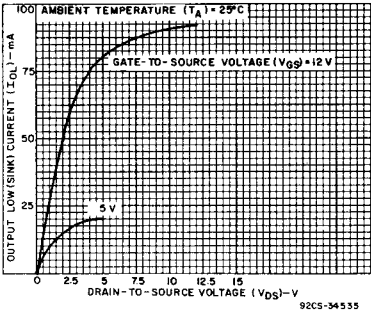


Fig. 3 - Typical N-Channel output low (sink) current characteristics - CMOS to TTL.

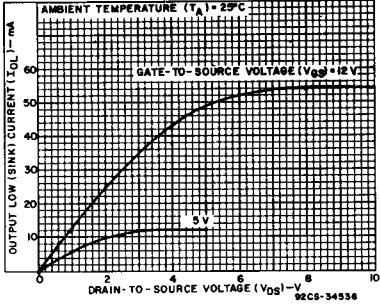


Fig. 4 - Typical output low (sink) current characteristics - TTL to CMOS.

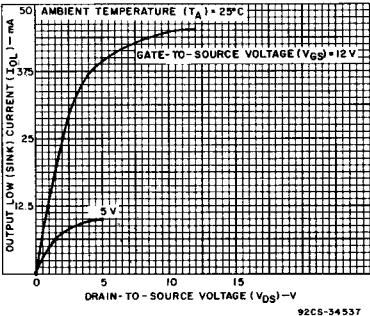


Fig. 5 - Minimum N-Channel output low (sink) current characteristics - CMOS

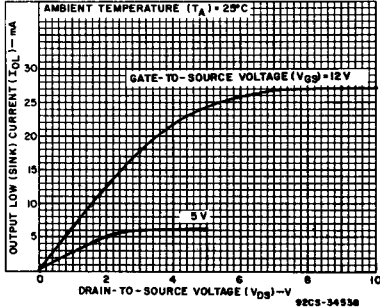


Fig. 6 - Minimum output low (sink) current characteristics - TTL to CMOS.

CD40116 Types

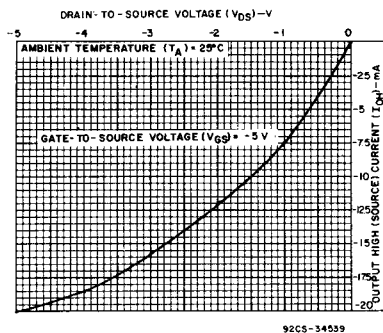


Fig. 7 - Typical P-channel output high (source) current characteristics - CMOS to TTL.

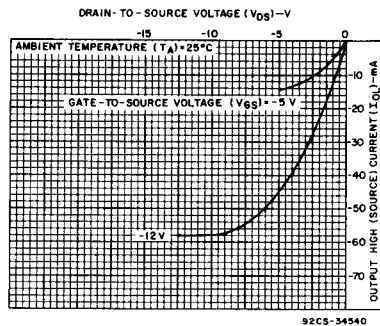


Fig. 8 - Typical output high (source) current characteristics - TTL to CMOS.

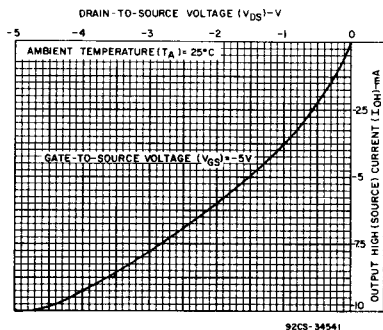


Fig. 9 - Minimum P-Channel output high (source) current characteristic - CMOS to TTL.

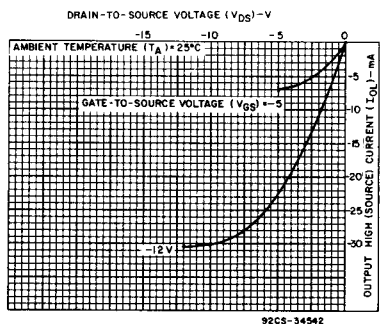


Fig. 10 - Minimum output high (source) current characteristics - TTL to CMOS.

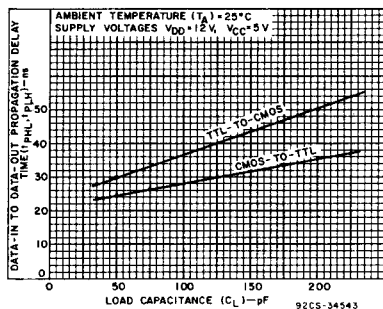


Fig. 11 - Typical DATA-IN to DATA-OUT propagation delay as a function of load capacitance.

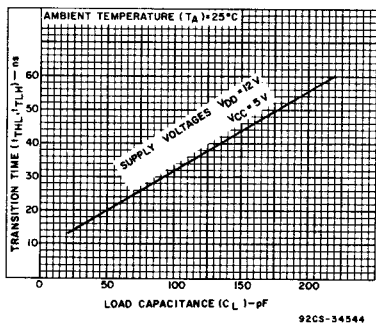


Fig. 12 - Typical transition time as a function of load capacitance CMOS-to-TTL or TTL-to-CMOS.

CD40116 Types

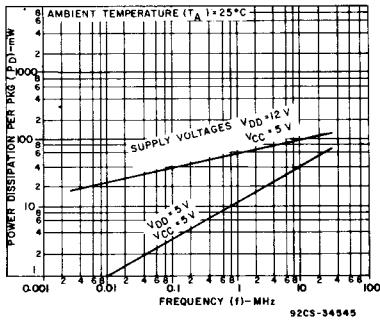


Fig. 13 - Power dissipation as a function of frequency - CMOS to TTL.

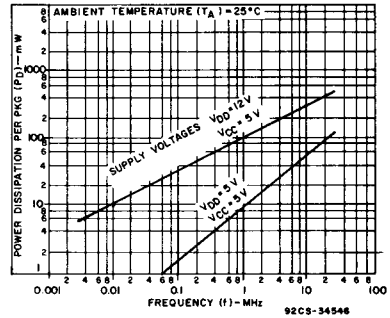
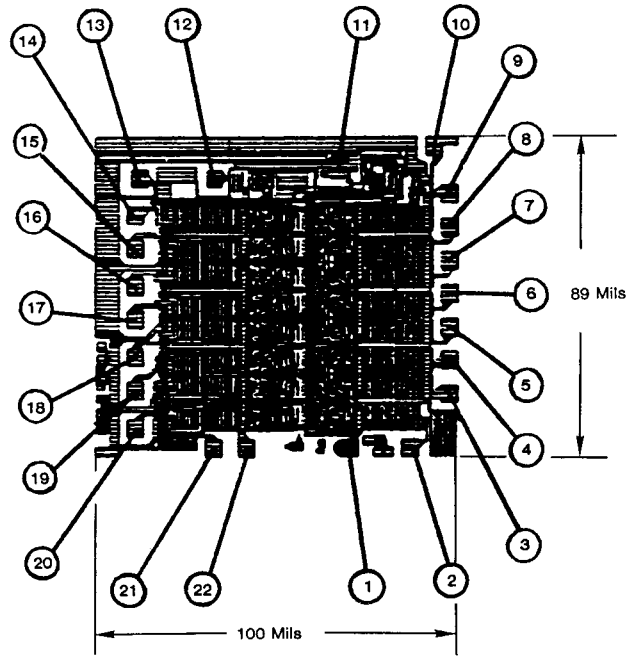


Fig. 14 - Power dissipation as a function of frequency - TTL to CMOS.



Dimensions and Pad Layout for CD40116H
Chip No. is TA11951B.