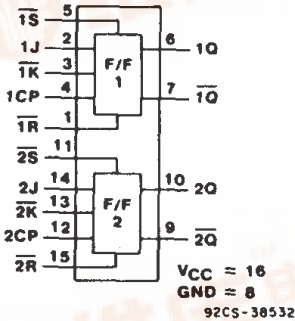




Data sheet acquired from Harris Semiconductor
SCHS282

CD54/74AC109, CD54/74AC112 CD54/74ACT109, CD54/74ACT112



CD54/74AC/ACT109
FUNCTIONAL DIAGRAM

Dual "J-K" Flip-Flop with Set and Reset

CD54/74AC/ACT109 - Positive-Edge-Triggered (J, \bar{K})

CD54/74AC/ACT112 - Negative-Edge-Triggered (J, K)

Type Features:

- Buffered inputs
- Typical propagation delay:
4.8 ns @ $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$

Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST[®]/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$ output drive current
 - Fanout to 15 FAST[®] ICs
 - Drives 50-ohm transmission lines

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

The RCA CD54/74AC109 and CD54/74AC112 and the CD54/74ACT109 and CD54/74ACT112 dual "J-K" flip-flops with set and reset use the RCA ADVANCED CMOS technology. These flip-flops have independent J, K (or \bar{K}), Set, Reset, and Clock inputs and Q and \bar{Q} outputs. The CD54/74AC/ACT112 changes state on the negative-going transition of the clock pulse. The CD54/74AC/ACT109 changes state on the positive-going transition of the clock. Set and Reset are accomplished asynchronously by low-level inputs.

The CD74AC/ACT109 and CD74AC/ACT112 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to $+85^\circ\text{C}$); and Extended Industrial/Military (-55 to $+125^\circ\text{C}$).

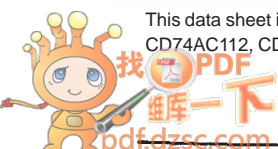
The CD54AC/ACT109 and CD54AC/ACT112, available in chip form (H suffix), are operable over the -55 to $+125^\circ\text{C}$ temperature range.

CD54/74AC/ACT109 TRUTH TABLE

INPUTS					OUTPUTS	
\bar{S}	\bar{R}	CP	J	\bar{K}	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H		L	L	L	H
H	H		H	L	TOGGLE	
H	H		L	H	NO CHANGE	
H	H		H	H	H	L
H	H	L	X	X	NO CHANGE	

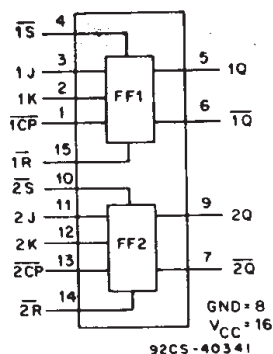
*Unpredictable and unstable condition if both \bar{S} and \bar{R} go high simultaneously.

9



Technical Data

CD54/74AC109, CD54/74AC112 CD54/74ACT109, CD54/74ACT112



CD54/74AC/ACT112
FUNCTIONAL DIAGRAM

CD54/74AC/ACT112 TRUTH TABLE

INPUTS					OUTPUTS	
\bar{S}	\bar{R}	\bar{CP}	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	High-to-Low transition	L	L	NO CHANGE	NO CHANGE
H	H	High-to-Low transition	H	L	H	L
H	H	High-to-Low transition	L	H	L	H
H	H	High-to-Low transition	H	H	TOGGLE	TOGGLE
H	H	H	X	X	NO CHANGE	NO CHANGE

*Output states unpredictable if \bar{S} and \bar{R} go High simultaneously after both being Low at the same time.

H = High steady state

L = Low steady state

X = Irrelevant

High-to-Low transition

Low-to-High transition

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE (V_{CC})	-0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	± 50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	± 50 mA
DC V_{CC} OR GROUND CURRENT (I_{CC} OR I_{GND})	± 100 mA*
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE (T_A)	-55 to $+125^\circ\text{C}$
STORAGE TEMPERATURE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. (1.59 mm) with solder contacting lead tips only	$+300^\circ\text{C}$

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC} †: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I , V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	$^\circ\text{C}$
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

†Unless otherwise specified, all voltages are referenced to ground

CD54/74AC109, CD54/74AC112 CD54/74ACT109, CD54/74ACT112

STATIC ELECTRICAL CHARACTERISTICS: AC Series

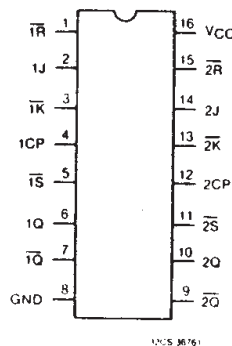
CHARACTERISTICS		TEST CONDITIONS		V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C						UNITS
					+25		-40 to +85		-55 to +125		
		V _i (V)	I _o (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V _{IH}			1.5 3 5.5	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	V
Low-Level Input Voltage	V _{IL}			1.5 3 5.5	— — —	0.3 0.9 1.65	— — 1.65	0.3 — —	— 0.9 1.65	0.3 0.9 1.65	V
High-Level Output Voltage	V _{OH}	V _{IH} or V _{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
		#, * }	-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V _{OL}	V _{IH} or V _{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
		#, * }	75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I _i	V _{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, FF	I _{CC}	V _{CC} or GND	0	5.5	—	4	—	40	—	80	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

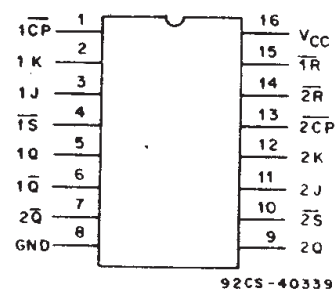
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

9

TERMINAL ASSIGNMENT DIAGRAMS



CD54/74AC/ACT109



CD54/74AC/ACT112

Technical Data

CD54/74AC109, CD54/74AC112 CD54/74ACT109, CD54/74ACT112

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V _{cc} (V)	AMBIENT TEMPERATURE (T _A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V _I (V)	I _O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V _{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V _{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V _{OH}	V _{IH} or V _{IL} #, * }	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
		-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V _{OL}	V _{IH} or V _{IL} #, * }	0.05	4.5	—	0.10	—	0.10	—	0.10	V
		24	4.5	—	0.36	—	0.44	—	0.50	
		75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I _I	V _{cc} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, FF I _{cc}	V _{cc} or GND	0	5.5	—	4	—	40	—	80	μA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI _{cc}	V _{cc} -2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*	
	109	112
J, CP, \overline{CP}	1	1
K	—	0.53
\overline{K}	0.53	—
\overline{S} , \overline{R}	0.58	0.58

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC109, CD54/74AC112

CD54/74ACT109, CD54/74ACT112

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Maximum CP, (\overline{CP}) Frequency 109	f _{max}	1.5 3.3* 5†	9 81 114	— — —	8 71 100	— — —	MHz
112	f _{max}	1.5 3.3 5	9 81 114	— — —	8 71 100	— — —	MHz
CP, (\overline{CP}) Pulse Width	t _w	1.5 3.3 5	55 6 4.4	— — —	63 7 5	— — —	ns
\overline{R} , \overline{S} Pulse Width	t _w	1.5 3.3 5	49 5.5 3.9	— — —	56 6.3 4.5	— — —	ns
Setup Time J, \overline{K} to CP 109	t _{su}	1.5 3.3 5	61 6.8 4.8	— — —	69 7.7 5.5	— — —	ns
J, K to \overline{CP} 112	t _{su}	1.5 3.3 5	44 4.9 3.5	— — —	50 5.6 4	— — —	ns
Hold Time J, \overline{K} to CP 109	t _H	1.5 3.3 5	0 0 0	— — —	0 0 0	— — —	ns
J, K to \overline{CP} 112	t _H	1.5 3.3 5	0 0 0	— — —	0 0 0	— — —	ns
Removal Time \overline{R} , \overline{S} to CP, (\overline{CP})	t _{rem}	1.5 3.1 5	27 3.1 2.2	— — —	31 3.5 2.5	— — —	ns

*3.3 V: min. is @ 3 V

†5 V: min is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP, (CP) to Q, Q̄	t _{PLH} t _{PHL}	1.5 3.3* 5†	— 3.7 2.7	117 13.1 9.4	— 3.6 2.6	129 14.4 10.3	ns
S̄, R to Q, Q̄	t _{PLH} t _{PHL}	1.5 3.3 5	— 4.4 3.2	139 15.5 11.1	— 4.3 3.1	153 17.1 12.2	ns
Power Dissipation Capacitance	C _{PD} §	—	56 Typ.		56 Typ.		pF
Input Capacitance	C _I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V†5 V: min. is @ 5.5 V
max. is @ 4.5 V§C_{PD} is used to determine the dynamic power consumption, per flip-flop.P_D = C_{PD}V_{CC}² f_i + Σ (C_LV_{CC}² f_o) where f_i = input frequencyf_o = output frequencyC_L = output load capacitanceV_{CC} = supply voltage.

Technical Data

CD54/74AC109, CD54/74AC112 CD54/74ACT109, CD54/74ACT112

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Maximum CP, (\overline{CP}) Frequency 109	f _{max}	5*	114	—	100	—	MHz
112			114	—	100	—	
CP, (\overline{CP}) Pulse Width	t _w	5	4.4	—	5	—	ns
R, \overline{S} Pulse Width	t _w	5	4.8	—	5.5	—	ns
Setup Time J, K to CP (109)	t _{su}	5	4.8	—	5.5	—	ns
J, K to \overline{CP} (112)			3.5	—	4	—	
Hold Time J, K to CP (109)	t _h	5	0	—	0	—	ns
J, K to \overline{CP} (112)			1	—	1	—	
Removal Time R, \overline{S} to CP, (\overline{CP})	t _{rem}	5	2.2	—	2.5	—	ns

*5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; $t_r, t_f = 3$ ns, $C_L = 50$ pF

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays CP, (CP) to Q, Q	t _{PLH} t _{PHL}	5*	2.7	9.4	2.6	10.3	ns
S, R, to Q, Q	t _{PLH} t _{PHL}	5	3.2	11.1	3.1	12.2	ns
Power Dissipation Capacitance	C _{PD} §	—	56 Typ.		56 Typ.		pF
Input Capacitance	C _I	—	—	10	—	10	pF

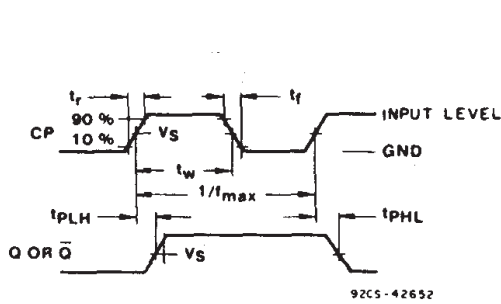
*5 V: min. is @ 5.5 V
max. is @ 4.5 V

§ C_{PD} is used to determine the dynamic power consumption, per flip-flop.

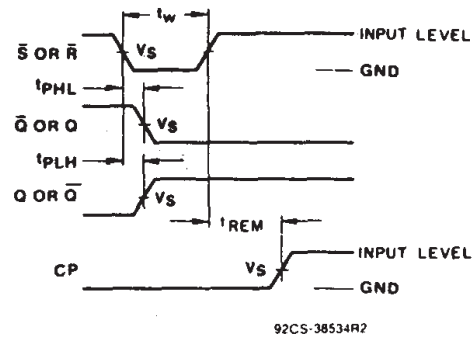
$P_D = C_{PD}V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
 f_o = output frequency
 C_L = output load capacitance
 V_{CC} = supply voltage.

CD54/74AC109, CD54/74AC112 CD54/74ACT109, CD54/74ACT112

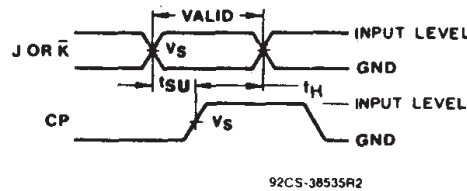
CD54/74AC/ACT109 Waveforms



Clock to output delays and clock pulse width.

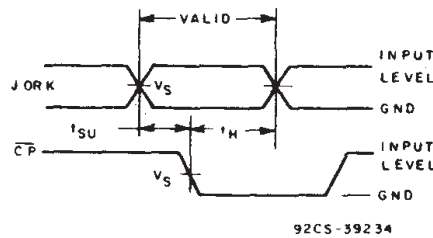
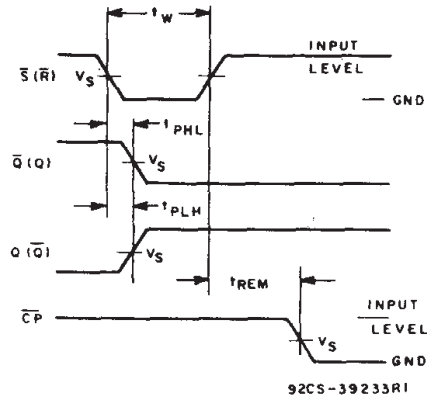
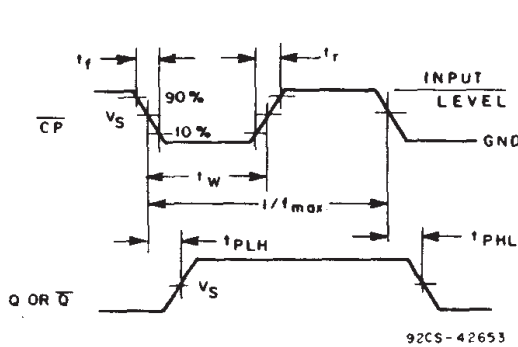


Reset or Set prerequisite and propagation delays.

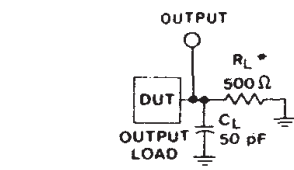


Data setup and hold times.

CD54/74/AC/ACT112 Waveforms



Propagation delay times, and setup and hold times.



*FOR AC SERIES ONLY: WHEN
V_{CC} = 1.5 V, R_L = 1 kΩ

92CS 42189

Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V _{CC}	3 V
Input Switching Voltage, V _S	0.5 V _{CC}	1.5 V
Output Switching Voltage, V _S	0.5 V _{CC}	0.5 V _{CC}

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.