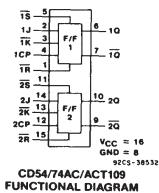


Technical Data



CD54/74AC109, CD54/74AC112 CD54/74ACT109, CD54/74ACT112

Data sheet acquired from Harris Semiconductor SCHS282



Dual "J-K" Flip-Flop with Set and Reset

CD54/74AC/ACT109 - Positive-Edge-Triggered (J, \overline{K}) CD54/74AC/ACT112 - Negative-Edge-Triggered (J, K)

Type Features:

Buffered inputs

■ Typical propagation delay:
 4.8 ns @ V_{cc} = 5 V, T_A = 25° C, C_L = 50 pF

The RCA CD54/74AC109 and CD54/74AC112 and the CD54/74ACT109 and CD54/74ACT112 dual "J-K" flip-flops with set and reset use the RCA ADVANCED CMOS technology. These flip-flops have independent J, K (or K), Set, Reset, and Clock inputs and Q and \overline{Q} outputs. The CD54/74AC/ACT112 changes state on the negative-going transition of the clock pulse. The CD54/74AC/ACT109 changes state on the positive-going transition of the clock. Set and Reset are accomplished asynchronously by low-level inputs.

The CD74AC/ACT109 and CD74AC/ACT112 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT109 and CD54AC/ACT112, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- Exceeds 2-kV ESD Protection MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST*/AS/S with significantly
- reduced power consumption
- Balanced propagation delays
 AC types feature 1.5 V/te 5.5 V/te
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
 - ± 24-mA output drive current
 - Fanout to 15 FAST* ICs
 - Drives 50-ohm transmission lines

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

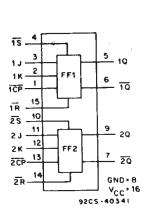
CD54/74AC/ACT109 TRUTH TABLE INPUTS **OUTPUTS** ŝ R CP ĸ J Q ā L н Х Х Х н L н L х Х x L н L Ł Х х H H' н н L L н L н Н TOGGLE н L н н L Н NO CHANGE н н н н н L н н L X х **NO CHANGE**

Unpredictable and unstable condition if both \overline{S} and \widetilde{R} go high simultaneously.

This data sheet is applicable to the CD54/74AC109, CD54AC112, CD45ACT109, and CD54ACT112. See SCHS233 for information on the CD74AC112, CD74ACT109, and CD74ACT112.

File Number 1967

Technical Data ______ CD54/74AC109, CD54/74AC112 CD54/74ACT109, CD54/74ACT112



		INPUTS			OUT	PUTS
s	R	ĈP	J	к	0	ā
L	н	x	x	x	н	L
`н ∶	L.	² X	x	x	L	н
L	L	Χ.	х	x	. н.	н.
н	н	- _	L	L	NO CH	IANGE
н	่ห	_٦_	н	L	н	L
н	н	_٦_	L	н	L	н
н	н	_/_	н	н	TOC	IGLE
н	н	н	X	×	NO CH	IANGE

CD54/74AC/ACT112 TRUTH TABLE

*Output states unpredictable if \overline{S} and \overline{R} go High simultaneously after both being Low at the same time.

- H = High steady state
- L = Low steady state X = Irrelevant

☐__ = High-to-Low transition

MAXIMUM RATINGS, Absolute-Maximum Values:

CD54/74AC/ACT112 FUNCTIONAL DIAGRAM

······································	
DC SUPPLY-VOLTAGE (Vcc)	
DC INPUT DIODE CURRENT. I_{ik} (for $V_i < -0.5 V$ or $V_i > V_{cc} + 0.5 V$)	±20 mA
DC OUTPUT DIODE CURRENT. l_{ok} (for $V_0 < -0.5$ V or $V_0 > V_{cc} + 0.5$ V)	±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I ₀ (for V ₀ > -0.5 V of	$V_0 < V_{cc} + 0.5 V$) ±50 mA
DC V _{cc} or GROUND CURRENT (I _{cc} or I _{GND})	±100 mA*
POWER DISSIPATION PER PACKAGE (PD):	
For $T_A = -55$ to $\pm 100^{\circ}$ C (PACKAGE TYPE E)	
For $T_A = \pm 100$ to $\pm 125^{\circ}$ C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For $T_{A} = -55$ to $\pm 70^{\circ}$ C (PACKAGE TYPE M)	
For $T_{A} = +70$ to $\pm 125^{\circ}$ C (PACKAGE TYPE M)	Derate Linearly at 6 mw/°C to 70 mw
OPERATING-TEMPERATURE BANGE (TA)	
STORAGE TEMPERATURE (T _{stg})	65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in (1.59 ± 0.79 mm) from case for 10 s maximum	+265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder conta	acting lead tips only+300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

	LIN	NITS	UNITS	
CHARACTERISTICS	MIN.	MAX.	UNITS	
Supply-Voltage Range, V _{CC} *: (For T _A = Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	v v	
DC Input or Output Voltage, V ₁ , V ₀	0	Vcc	V	
Operating Temperature, T _A	-55	+125	°C	
Input Rise and Fall Slew Rate, dt/dv at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V	

*Unless otherwise specified, all voltages are referenced to ground

Technical Data CD54/74AC109, CD54/74AC112 CD54/74ACT109, CD54/74ACT112

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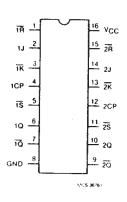
STATIC ELECTRICAL CHARACTERISTICS: AC Series

					AMBIENT TEMPERATURE (T _A) - °C						
CHARACTERISTICS		TEST CO	EST CONDITIONS		+25		-40 to +85		-55 to +125		UNITS
		V, (V)	l _o (mA)	V _{cc} (V)	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	1
High-Level Input Voltage	V _{ін}			1.5 3 5.5	1.2 2.1 3.85		1.2 2.1 3.85	-	1.2 2.1 3.85		v
Low-Level Input Voltage	Vit			1.5 3 5.5	-	0.3 0.9 1.65		0.3 0.9 1.65		0.3 0.9 1.65	v
High-Level Output			-0.05	1.5	1.4		1.4	_	1.4		
Voltage	Vон	VIH	-0.05	3	2.9		2.9		2.9		1
		or .	-0.05	4.5	4.4	-	4.4	_	4.4	-	1
		ViL	-4	3	2.58		2.48		2.4		l v
			-24	4.5	3.94	_	3.8	_	3.7		1
		#, * {	-75	5.5	_		3.85			_	
		<i>"</i> , "	-50	5.5	_	-	—		3.85	—	
Low-Level Output			0.05	1.5	—	0.1		0.1	_	0.1	
Voltage	Vol	· ViH	0.05	3	—	0.1	—	0.1	_	0.1	
		or	0.05	4.5	_	0.1	_	0.1	_	0.1	
		VIL	12	3	-	0.36	-	0.44	_	0.5	v
			24	4.5	—	0.36	—	0.44		0.5	
		#, * {	75	5.5	_	_		1.65	_	—	
		<u>"')</u>	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	lı -	V _{cc} or GND		5.5	—	±0.1	-	±1	_	±1	μA
Quiescent Supply Current, FF	lcc	V _{cc} or GND	0	5.5	_	4		40	_	80	μΑ

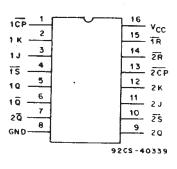
2

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation. * Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

TERMINAL ASSIGNMENT DIAGRAMS



CD54/74AC/ACT109



CD54/74AC/ACT112

Technical Data CD54/74AC109, CD54/74AC112 CD54/74ACT109, CD54/74ACT112 STATIC ELECTRICAL CHARACTERISTICS: ACT Series

						Т ТЕМРЕ	RATURE	(T _A) - °(0		
CHARACTERISTICS		TEST CONDITIONS		V _{cc}	Y ₂₅ +25		-40 to +85		-55 to +125		UNITS
		V, (V)	l _o (mA)	(Ÿ)	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	ViH			4.5 to 5.5	2	_	2		2	_	v
Low-Level Input Voltage	ViL			4.5 to 5.5		0.8	_	0.8	_	0.8	v
High-Level Output		Vн	-0.05	4.5	4.4	-	4.4	-	4.4		
Voltage	Vон	or V _{IL}	-24	4.5	3.94	-	3.8	—	3.7		
		#, * {	-75	5.5			3.85	Γ –	—	_] V
		#, ~ <u>}</u>	-50	5.5			<u> </u>	-	3.85		
Low-Level Output		ViH	0.05	4.5	—	0.10		0.10	—	0.10	
Voltage	VOL	or Vit	24	4.5	-	0.36	—	0.44		0.50	v .
		6	75	5.5	_	Γ	—	1.65	—	—	
		#, * {	50	5.5		-		—	_	1.65]
Input Leakage Current	1	V _{cc} or GND		5.5	_	±0.1	_	±1	_	±1	μA
Quiescent Supply Current, FF	lcc	V _{cc} or GND	0	5.5	_	4	-	40	—	80	μΑ
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	Δlcc	V _{cc} -2.1		4.5 to 5.5	_	2.4		2.8		3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation. * Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*					
INFUT	109	112				
J, CP, CP	1	1				
K	_	0.53				
ĸ	0.53	—				
<u></u>	0.58	0.58				

*Unit load is Alcc limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Technical Data

CD54/74AC109, CD54/74AC112 CD54/74ACT109, CD54/74ACT112

PREREQUISITE FOR SWITCHING: AC Series

	^{х.} ж		AMBI	ENT TEMPE	ERATURE (1	「∧) - °C	
CHARACTERISTICS	SYMBOL	V _{cc} (V)	-40 to +85		-55 to +125		
		(•)	MIN.	MAX.	MIN.	MAX.	7
Maximum CP, (CP) Frequency 109	f _{max}	1.5 3.3* 5†	9 81 114		8 71 100		MHz
112	fmax	1.5 3.3 5	9 81 114	-	8 71 100		MHz
CP, (CP) Pulse Width	tw	1.5 3.3 5	55 6 4.4	 	63 7 5		ns
Ř, Š Pulse Width	tw	1.5 3.3 5	49 5.5 3.9	 	56 6.3 4.5		ns
Setup Time J, K to CP 109	tsu	1.5 3.3 5	61 6.8 4.8		69 7.7 5.5		ns
J, K to ĈP 112	tsu	1.5 3.3 5	44 4.9 3.5		50 5.6 4	-	ns
Hold Time J, K to CP 109	t _H	1.5 3.3 5	0 0 0		0 0 0	-	ns
J, K to CP 112	tн	1.5 3.3 5	0 0 0		0 0 0		ns
Removal Time R, S to CP, (CP)	trem	1.5 3.1 5	27 3.1 2.2		31 3.5 2.5		ns

*3.3 V: min. is @ 3 V

†5 V: min is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t,, t, = 3 ns, CL = 50 pF

			AMB	ENT TEMPE	RATURE (T	γ) - °C	1
CHARACTERISTICS	SYMBOL	V _{cc} (V)	-40 t	o +85	-55 to		
		(V)	MIN.	MAX.	MIN.	MAX.	1
Propagation Delays: CP, (CP) to Q, Q	tрін tрні	1.5 3.3* 5†	 3.7 2.7	117 13.1 9.4	 3.6 2.6	129 14.4 10.3	ns
S, R to Q, Q	t _{РLH} t _{PHL}	1.5 3.3 5	 4,4 3.2	139 15.5 11.1		153 17,1 12.2	ns
Power Dissipation Capacitance	CPD§	_	56	Тур.	56	Гур.	pF
Input Capacitance	C ₁	_	_	10		10	pF

*3.3 V: min. is @ 3.6 V max. is @ 3 V

† 5 V: min. is @ 5.5 V max. is @ 4.5 V §CPD is used to determine the dynamic power consumption, per flip-flop. $P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where $f_i = input$ frequency

 $f_0 = output frequency$

 C_L = output load capacitance

 $V_{cc} =$ supply voltage.

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Technical Data CD54/74AC109, CD54/74AC112 CD54/74ACT109, CD54/74ACT112

PREREQUISITE FOR SWITCHING: ACT Series

			AMBI	AMBIENT TEMPERATURE (TA) - °C					
CHARACTERISTICS	SYMBOL	V _{cc} (V)	-40 to +85		-55 to +125		UNITS		
		(*)	MIN.	MAX.	MIN.	MAX.			
Maximum CP, (CP) Frequency 109	fmax	5*	114	_	100	_	MHz		
112			114	_	100	-			
CP, (CP) Pulse Width	tw	5	4.4	_	5	—	ns:		
R, S Pulse Width	tw	5	4.8	_	5.5		ns		
Setup Time J, K to CP (109)	tsu	5	.4.8	·	5.5	-	ns		
J, K to CP (112)	· · · · ·		3.5	_	4	·]		
Hold Time J, K to CP (109)	tH	5	0	_	0	_	ns		
J, K to CP (112)			1	_	1]		
Removal Time R, S to CP, (CP)	tREM	5	2.2		2.5		ns		

*5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t,, t, = 3 ns, CL = 50 pF

			AMBI	ENT TEMPE	RATURE (1	「₄) - °C	
CHARACTERISTICS	SYMBOL	V _{cc} (V)	c -40 to +85		-55 to	UNITS	
		(*)	MIN.	MAX.	MIN.	MAX.	1
Propagation Delays_ CP, (CP) to Q, Q	t _{РLH} t _{РHL}	5*	2.7	9.4	2.6	10.3	ns
S, R, to Q, Q	tрын трнс	5	3.2	11.1	3.1	12.2	ns
Power Dissipation Capacitance	CPD§	·	56	Тур.	56	Тур.	pF
Input Capacitance	C,		-	10	-	10	pF

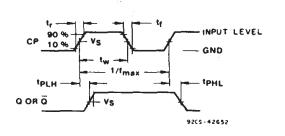
*5 V: min. is @ 5.5 V max. is @ 4.5 V §CPD is used to determine the dynamic power consumption, per flip-flop. $P_{D} = C_{PD}V_{CC}^{2} f_{i} + \Sigma (C_{L}V_{CC}^{2} f_{o}) + V_{CC} \Delta I_{CC} \text{ where } f_{i} = \text{input frequency}$

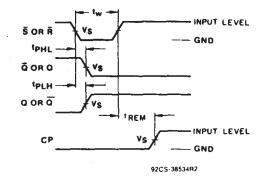
 $f_o = output frequency$ $C_L = output load capacitance$

 V_{cc} = supply voltage.

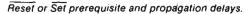
CD54/74AC109, CD54/74AC112 CD54/74ACT109, CD54/74ACT12

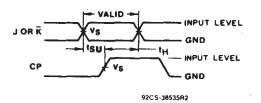
CD54/74AC/ACT109 Waveforms





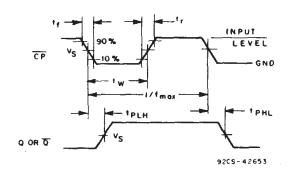
Clock to output delays and clock pulse width.

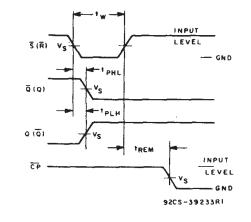


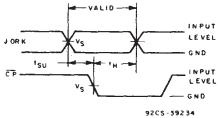


Data setup and hold times.









Propagation delay times, and setup and hold times.

9265 42189

Test circuit.

OUTPUT 50 pF

	CD54/74AC	CD54/74ACT
Input Level	Vcc	3 V
Input Switching Voltage, Vs	0.5 V _{cc}	1.5 V
Output Switching Voltage, Vs	0.5 V _{cc}	0.5 V _{cc}

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