

# CD54AC273, CD74AC273 CD54ACT273, CD74ACT273

August 1998 - Revised April 2000

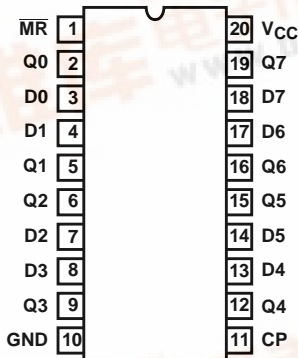
## Octal D Flip-Flop with Reset

### Features

- Buffered Inputs
- Typical Propagation Delay
  - 6.5ns at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 50pF$
- Exceeds 2kV ESD Protection MIL-STD-883, Method 3015
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S with Significantly Reduced Power Consumption
- Balanced Propagation Delays
- AC Types Feature 1.5V to 5.5V Operation and Balanced Noise Immunity at 30% of the Supply
- $\pm 24mA$  Output Drive Current
  - Fanout to 15 FAST™ ICs
  - Drives 50 $\Omega$  Transmission Lines

### Pinout

CD54AC273, CD54ACT273  
(CDIP)  
CD74AC273, CD74ACT273  
(PDIP, SOIC)  
TOP VIEW



### Description

The 'AC273 and 'ACT273 devices are octal D-type flip-flops with reset that utilize advanced CMOS logic technology. Information at the D input is transferred to the Q output on the positive-going edge of the clock pulse. All eight flip-flops are controlled by a common clock (CP) and a common reset (MR). Resetting is accomplished by a low voltage level independent of the clock.

### Ordering Information

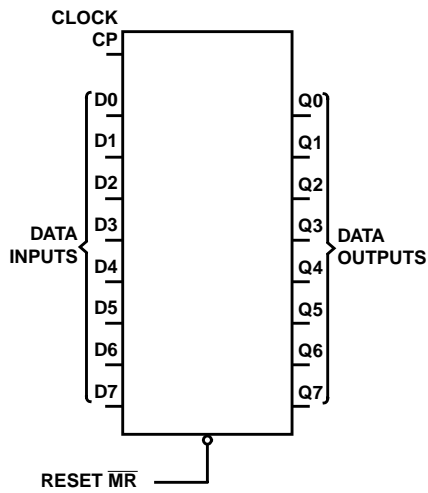
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CD74AC273E	-40°C to 85°C	20 Ld PDIP
CD54AC273F3A	-55°C to 125°C	20 Ld CDIP
CD74ACT273E	-40°C to 85°C	20 Ld PDIP
CD54ACT273F3A	-55°C to 125°C	20 Ld CDIP
CD74AC273M	-40°C to 85°C	20 Ld SOIC
CD74ACT273M	-40°C to 85°C	20 Ld SOIC

#### NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office for ordering information.

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**Functional Diagram**



**TRUTH TABLE**

INPUTS			OUTPUTS
RESET (MR)	CLOCK CP	DATA Dn	Qn
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q0

H = High level (steady state), L = Low level (steady state), X = Irrelevant, ↑ = Transition from Low to High level, Q0 = The level of Q before the indicated steady-state input conditions were established.

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### Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 6V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 50mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 50mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ (Note 3) .....	$\pm 100mA$

### Thermal Information

Thermal Resistance, $\theta_{JA}$ (Typical, Note 5)	
E Package .....	69°C/W
M Package .....	58°C/W
Maximum Junction Temperature (Plastic Package) .....	150°C
Maximum Storage Temperature Range .....	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) .....	300°C

### Operating Conditions

Temperature Range, $T_A$	
CD54AC273, CD54ACT273 .....	-55°C to 125°C
CD74AC273, CD74ACT273 .....	-40°C to 85°C
Supply Voltage Range, $V_{CC}$ (Note 4)	
AC Types .....	1.5V to 5.5V
ACT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I, V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Slew Rate, $dt/dv$	
AC Types, 1.5V to 3V .....	50ns (Max)
AC Types, 3.6V to 5.5V .....	20ns (Max)
ACT Types, 4.5V to 5.5V .....	10ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

#### NOTES:

3. For up to 4 outputs per device, add  $\pm 25mA$  for each additional output.
4. Unless otherwise specified, all voltages are referenced to ground.
5. The package thermal impedance is calculated in accordance with JESD 51.

### DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS	
		$V_I$ (V)	$I_O$ (mA)		MIN	MAX	MIN	MAX	MIN	MAX		
<b>AC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	1.5	1.2	-	1.2	-	1.2	-	V	
				3	2.1	-	2.1	-	2.1	-	V	
				5.5	3.85	-	3.85	-	3.85	-	V	
Low Level Input Voltage	$V_{IL}$	-	-	1.5	-	0.3	-	0.3	-	0.3	V	
				3	-	0.9	-	0.9	-	0.9	V	
				5.5	-	1.65	-	1.65	-	1.65	V	
High Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.05	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
			-0.05	-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-4	-4	3	2.58	-	2.48	-	2.4	-	V
			-24	-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V
-50 (Note 6, 7)	-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V			

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**DC Electrical Specifications (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
Low Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	-	5.5	-	±0.1	-	±1	-	±1	µA
Quiescent Supply Current MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	8	-	80	-	160	µA
<b>ACT TYPES</b>											
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V
Low Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	-	5.5	-	±0.1	-	±1	-	±1	µA
Quiescent Supply Current MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	8	-	80	-	160	µA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	2.4	-	2.8	-	3	mA

**NOTES:**

- Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
- Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

**ACT Input Load Table**

INPUT	UNIT LOAD
Dn	0.5
MR	0.57
CP	1

NOTE: Unit load is ΔI<sub>CC</sub> limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

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**Prerequisite For Switching Function**

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	
<b>AC TYPES</b>							
Data to CP Set-Up Time	t <sub>SU</sub>	1.5	2	-	2	-	ns
		3.3 (Note 9)	2	-	2	-	ns
		5 (Note 10)	2	-	2	-	ns
Hold Time	t <sub>H</sub>	1.5	2	-	2	-	ns
		3.3	2	-	2	-	ns
		5	2	-	2	-	ns
Removal Time, $\overline{MR}$ to CP	t <sub>REM</sub>	1.5	2	-	2	-	ns
		3.3	2	-	2	-	ns
		5	2	-	2	-	ns
$\overline{MR}$ Pulse Width	t <sub>W</sub>	1.5	55	-	63	-	ns
		3.3	6.1	-	7	-	ns
		5	4.4	-	5	-	ns
CP Pulse Width	t <sub>W</sub>	1.5	55	-	63	-	ns
		3.3	6.1	-	7	-	ns
		5	4.4	-	5	-	ns
CP Frequency	f <sub>MAX</sub>	1.5	9	-	8	-	MHz
		3.3	81	-	71	-	MHz
		5	114	-	100	-	MHz
<b>ACT TYPES</b>							
Data to CP Set-Up Time	t <sub>SU</sub>	5 (Note 10)	2	-	2	-	ns
Hold Time	t <sub>H</sub>	5	2	-	2	-	ns
Removal Time $\overline{MR}$ to CP	t <sub>REM</sub>	5	2	-	2	-	ns
$\overline{MR}$ Pulse Width	t <sub>W</sub>	5	4.4	-	5	-	ns
CP Pulse Width	t <sub>W</sub>	5	5.3	-	6	-	ns
CP Frequency	f <sub>MAX</sub>	5	97	-	85	-	MHz

**Switching Specifications** Input t<sub>r</sub>, t<sub>f</sub> = 3ns, C<sub>L</sub> = 50pF (Worst Case)

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>AC TYPES</b>									
Propagation Delay, CP to Qn	t <sub>PLH</sub> , t <sub>PHL</sub>	1.5	-	-	154	-	-	169	ns
		3.3 (Note 9)	4.9	-	17.2	4.7	-	18.9	ns
		5 (Note 10)	3.5	-	12.3	3.4	-	13.5	ns

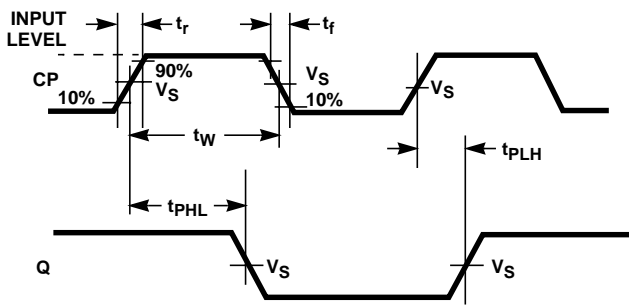
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**Switching Specifications** Input  $t_r, t_f = 3\text{ns}$ ,  $C_L = 50\text{pF}$  (Worst Case) (Continued)

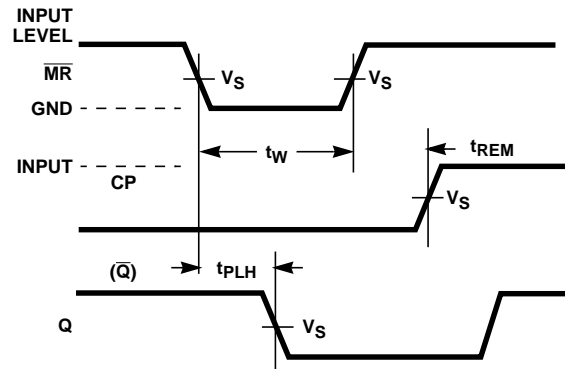
PARAMETER	SYMBOL	$V_{CC}$ (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay, MR to Qn	$t_{PLH}, t_{PHL}$	1.5	-	-	154	-	-	169	ns
		3.3	4.9	-	17.2	4.7	-	18.9	ns
		5	3.5	-	12.3	3.4	-	13.5	ns
Input Capacitance	$C_I$	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	$C_{PD}$ (Note 11)	-	-	45	-	-	45	-	pF
<b>ACT TYPES</b>									
Propagation Delay, CP to Qn	$t_{PLH}, t_{PHL}$	5 (Note 10)	3.5	-	12.3	3.4	-	13.5	ns
Propagation Delay, MR to Qn	$t_{PLH}, t_{PHL}$	5	3.5	-	12.3	3.4	-	13.5	ns
Input Capacitance	$C_I$	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	$C_{PD}$ (Note 11)	-	-	45	-	-	45	-	pF

NOTES:

8. Limits tested 100%.
9. 3.3V Min is at 3.6V, Max is at 3V.
10. 5V Min is at 5.5V, Max is at 4.5V.
11.  $C_{PD}$  is used to determine the dynamic power consumption per flip-flop.  
 AC:  $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o)$   
 ACT:  $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency,  $f_o$  = output frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

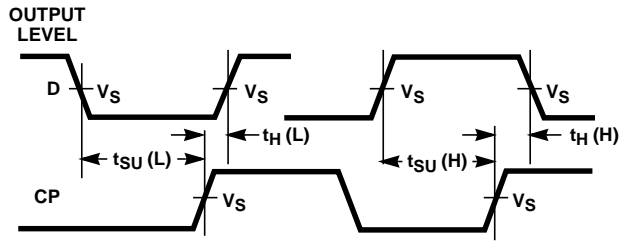


**FIGURE 1. PROPAGATION DELAY TIMES AND CLOCK PULSE WIDTH**

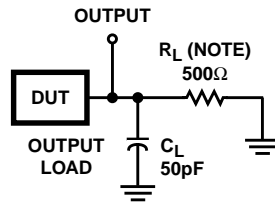


**FIGURE 2. PREREQUISITE AND PROPAGATION DELAY TIMES FOR MASTER RESET**

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**FIGURE 3. PREREQUISITE FOR CLOCK**



NOTE: For AC Series Only: When  $V_{CC} = 1.5V$ ,  $R_L = 1k\Omega$ .

	AC	ACT
Input Level	$V_{CC}$	3V
Input Switching Voltage, $V_S$	$0.5 V_{CC}$	1.5V
Output Switching Voltage, $V_S$	$0.5 V_{CC}$	$0.5 V_{CC}$

**FIGURE 4. PROPAGATION DELAY TIMES**

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