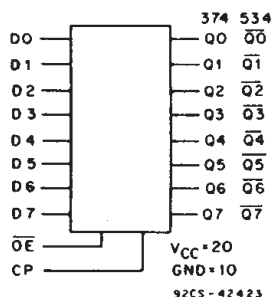




Data sheet acquired from Harris Semiconductor
SCHS290

CD54/74AC374, CD54/74AC534 CD54/74ACT374, CD54/74ACT534



FUNCTIONAL DIAGRAM

Octal D-Type Flip-Flops, 3-State Positive-Edge Triggered

CD54/74AC/ACT374 - Non-Inverting

CD54/74AC/ACT534 - Inverting

Type Features:

- Buffered inputs
- Typical propagation delay:
5 ns @ $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$

The RCA-CD54/74AC374 and CD54/74AC534 and the CD54/74ACT374 and CD54/74ACT534 octal D-type, 3-state, positive-edge triggered flip-flops use the RCA ADVANCED CMOS technology. The eight flip-flops enter data into their registers on the LOW-to-HIGH transition of the clock (CP). The Output Enable (\overline{OE}) controls the 3-state outputs and is independent of the register operation. When the Output Enable (\overline{OE}) is HIGH, the outputs are in the high-impedance state. The CD54/74AC/ACT374 and CD54/74AC/ACT534 share the same pin configurations, but the CD54/74AC/ACT374 outputs are non-inverted while the CD54/74AC/ACT534 devices have inverted outputs. (For flow-through pin configurations, see CD54/74AC/ACT564 and CD54/74AC/ACT574.)

The CD74AC/ACT374 and CD74AC/ACT534 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to $+85^\circ\text{C}$); and Extended Industrial/Military (-55 to $+125^\circ\text{C}$).

The CD54AC/ACT374 and CD54AC/ACT534, available in chip form (H suffix), are operable over the -55 to $+125^\circ\text{C}$ temperature range.

Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latch-up-resistant CMOS process and circuit design
- Speed of bipolar FAST*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$ output drive current
 - Fanout to 15 FAST* ICs
 - Drives 50-ohm transmission lines

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

| INPUTS | | | OUTPUTS | |
|-----------------|----|----|---------|-----------------|
| | | | 374 | 534 |
| \overline{OE} | CP | Dn | Qn | \overline{Qn} |
| L | | H | H | L |
| L | | L | L | H |
| L | L | X | QO | QO |
| H | X | X | Z | Z |

H = High level (steady state)

L = Low level (steady state)

X = Don't care

= Transition from low to high level

QO = The level of Q before the indicated steady-state input conditions were established

Z = High impedance

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CD54/74AC374, CD54/74AC534 CD54/74ACT374, CD54/74ACT534

MAXIMUM RATINGS, Absolute-Maximum Values:

| | |
|--|---|
| DC SUPPLY-VOLTAGE (V_{CC}) | -0.5 to 6 V |
| DC INPUT DIODE CURRENT, I_{IK} (for $V_i < -0.5$ V or $V_i > V_{CC} + 0.5$ V) | ± 20 mA |
| DC OUTPUT DIODE CURRENT, I_{OK} (for $V_o < -0.5$ V or $V_o > V_{CC} + 0.5$ V) | ± 50 mA |
| DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_o (for $V_o > -0.5$ V or $V_o < V_{CC} + 0.5$ V) | ± 50 mA |
| DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) | ± 100 mA* |
| POWER DISSIPATION PER PACKAGE (P_D): | |
| For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE E) | 500 mW |
| For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E) | Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW |
| For $T_A = -55$ to $+70^\circ\text{C}$ (PACKAGE TYPE M) | 400 mW |
| For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M) | Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW |
| OPERATING-TEMPERATURE RANGE (T_A) | -55 to $+125^\circ\text{C}$ |
| STORAGE TEMPERATURE (T_{stg}) | -65 to $+150^\circ\text{C}$ |
| LEAD TEMPERATURE (DURING SOLDERING): | |
| At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s maximum | $+265^\circ\text{C}$ |
| Unit inserted into PC board min. thickness $1/16$ in. (1.59 mm) with solder contacting lead tips only | $+300^\circ\text{C}$ |

*For up to 4 outputs per device; add ± 25 mA for each additional output.

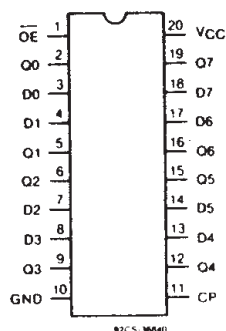
RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

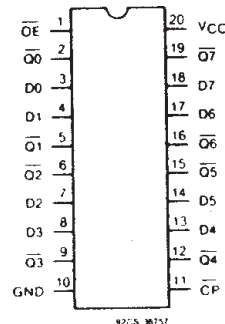
| CHARACTERISTIC | LIMITS | | UNITS |
|---|--------|----------|------------------|
| | MIN. | MAX. | |
| Supply-Voltage Range, V_{CC} *: (For T_A = Full Package-Temperature Range) AC Types ACT Types | 1.5 | 5.5 | V |
| | 4.5 | 5.5 | V |
| | 0 | V_{CC} | V |
| DC Input or Output Voltage, V_i , V_o | 0 | V_{CC} | V |
| Operating Temperature, T_A | -55 | $+125$ | $^\circ\text{C}$ |
| Input Rise and Fall Slew Rate, dt/dv at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types) | 0 | 50 | ns/V |
| | 0 | 20 | ns/V |
| | 0 | 10 | ns/V |
| | 0 | 10 | ns/V |

*Unless otherwise specified, all voltages are referenced to ground.

TERMINAL ASSIGNMENT DIAGRAMS



CD54/74AC/ACT374



CD54/74AC/ACT534

Technical Data

CD54/74AC374, CD54/74AC534 CD54/74ACT374, CD54/74ACT534

STATIC ELECTRICAL CHARACTERISTICS: AC Series

| CHARACTERISTICS | | TEST CONDITIONS | | V _{CC} (V) | AMBIENT TEMPERATURE (T _A) - °C | | | | | | UNITS |
|-------------------------------|-----------------|--|------------------------|------------------------|--|------|------------|------|-------------|------|-------|
| | | | | | +25 | | -40 to +85 | | -55 to +125 | | |
| | | V _I (V) | I _O (mA) | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| High-Level Input Voltage | V _{IH} | | | 1.5 | 1.2 | — | 1.2 | — | 1.2 | — | V |
| | | | | 3 | 2.1 | — | 2.1 | — | 2.1 | — | |
| | | | | 5.5 | 3.85 | — | 3.85 | — | 3.85 | — | |
| Low-Level Input Voltage | V _{IL} | | | 1.5 | — | 0.3 | — | 0.3 | — | 0.3 | V |
| | | | | 3 | — | 0.9 | — | 0.9 | — | 0.9 | |
| | | | | 5.5 | — | 1.65 | — | 1.65 | — | 1.65 | |
| High-Level Output Voltage | V _{OH} | V _{IH} or V _{IL} #, * { | -0.05 | 1.5 | 1.4 | — | 1.4 | — | 1.4 | — | V |
| | | | -0.05 | 3 | 2.9 | — | 2.9 | — | 2.9 | — | |
| | | | -0.05 | 4.5 | 4.4 | — | 4.4 | — | 4.4 | — | |
| | | | -4 | 3 | 2.58 | — | 2.48 | — | 2.4 | — | |
| | | | -24 | 4.5 | 3.94 | — | 3.8 | — | 3.7 | — | |
| | | | -75 | 5.5 | — | — | 3.85 | — | — | — | |
| | | | -50 | 5.5 | — | — | — | — | 3.85 | — | |
| Low-Level Output Voltage | V _{OL} | V _{IH} or V _{IL} #, * { | 0.05 | 1.5 | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 0.05 | 3 | — | 0.1 | — | 0.1 | — | 0.1 | |
| | | | 0.05 | 4.5 | — | 0.1 | — | 0.1 | — | 0.1 | |
| | | | 12 | 3 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | | | 24 | 4.5 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | | | 75 | 5.5 | — | — | — | 1.65 | — | — | |
| | | | 50 | 5.5 | — | — | — | — | — | 1.65 | |
| Input Leakage Current | I _I | V _{CC} or GND | | 5.5 | — | ±0.1 | — | ±1 | — | ±1 | μA |
| 3-State Leakage Current | I _{OZ} | V _{IH} or V _{IL} V _O = V _{CC} or GND | | 5.5 | — | ±0.5 | — | ±5 | — | ±10 | μA |
| Quiescent Supply Current, MSI | I _{CC} | V _{CC} or GND | 0 | 5.5 | — | 8 | — | 80 | — | 160 | μA |

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC374, CD54/74AC534 CD54/74ACT374, CD54/74ACT534

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

| CHARACTERISTICS | TEST CONDITIONS | | V _{CC} (V) | AMBIENT TEMPERATURE (T _A) - °C | | | | | | UNITS |
|---|---|------------------------|------------------------|--|------|------------|------|-------------|------|-------|
| | | | | +25 | | -40 to +85 | | -55 to +125 | | |
| | V _I (V) | I _O (mA) | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| High-Level Input Voltage V _{IH} | | | 4.5 to 5.5 | 2 | — | 2 | — | 2 | — | V |
| Low-Level Input Voltage V _{IL} | | | 4.5 to 5.5 | — | 0.8 | — | 0.8 | — | 0.8 | V |
| High-Level Output Voltage V _{OH} | V _{IH} or V _{IL} #1, * { | -0.05 | 4.5 | 4.4 | — | 4.4 | — | 4.4 | — | V |
| | | -24 | 4.5 | 3.94 | — | 3.8 | — | 3.7 | — | |
| | | -75 | 5.5 | — | — | 3.85 | — | — | — | |
| | | -50 | 5.5 | — | — | — | — | 3.85 | — | |
| Low-Level Output Voltage V _{OL} | V _{IH} or V _{IL} #1, * { | 0.05 | 4.5 | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | 24 | 4.5 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | | 75 | 5.5 | — | — | — | 1.65 | — | — | |
| | | 50 | 5.5 | — | — | — | — | — | 1.65 | |
| Input Leakage Current I _I | V _{CC} or GND | | 5.5 | — | ±0.1 | — | ±1 | — | ±1 | μA |
| 3-State Leakage Current I _{OZ} | V _{IH} or V _{IL} V _O = V _{CC} or GND | | 5.5 | — | ±0.5 | — | ±5 | — | ±10 | μA |
| Quiescent Supply Current, MSI I _{CC} | V _{CC} or GND | 0 | 5.5 | — | 8 | — | 80 | — | 160 | μA |
| Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI _{CC} | V _{CC} -2.1 | | 4.5 to 5.5 | — | 2.4 | — | 2.8 | — | 3 | mA |

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

| INPUT | UNIT LOADS* |
|-------|-------------|
| D, OE | 0.7 |
| CP | 1.17 |

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Technical Data

CD54/74AC374, CD54/74AC534 CD54/74ACT374, CD54/74ACT534

PREREQUISITE FOR SWITCHING: AC Series

| CHARACTERISTICS | SYMBOL | V _{CC} (V) | AMBIENT TEMPERATURE (T _A) - °C | | | | UNITS |
|-----------------------------|------------------|------------------------|--|------|-------------|------|-------|
| | | | -40 to +85 | | -55 to +125 | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| Clock Pulse Width | t _w | 1.5 | 44 | — | 50 | — | ns |
| | | 3.3* | 4.9 | — | 5.6 | — | |
| | | 5† | 3.5 | — | 4 | — | |
| Setup Time Data to Clock | t _{su} | 1.5 | 2 | — | 2 | — | ns |
| | | 3.3 | 2 | — | 2 | — | |
| | | 5 | 2 | — | 2 | — | |
| Hold Time Data to Clock | t _h | 1.5 | 2 | — | 2 | — | ns |
| | | 3.3 | 2 | — | 2 | — | |
| | | 5 | 2 | — | 2 | — | |
| Maximum Clock Frequency | f _{MAX} | 1.5 | 11 | — | 10 | — | MHz |
| | | 3.3 | 101 | — | 89 | — | |
| | | 5 | 143 | — | 125 | — | |

*3.3 V: min. is @ 3 V

†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

| CHARACTERISTICS | SYMBOL | V _{CC} (V) | AMBIENT TEMPERATURE (T _A) - °C | | | | UNITS |
|---|--------------------------------------|------------------------|--|---------------------|-----------------|---------------------|-------|
| | | | -40 to +85 | | -55 to +125 | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| Propagation Delays: Clock to Q AC374 | t _{PLH} t _{PHL} | 1.5 3.3* 5† | — 3.9 2.8 | 123 13.7 9.8 | — 3.8 2.7 | 135 15.1 10.8 | ns |
| Clock to \overline{Q} AC534 | t _{PLH} t _{PHL} | 1.5 3.3 5 | — 4.1 2.9 | 128 14.4 10.3 | — 4 2.8 | 141 15.8 11.3 | ns |
| Output Enable to Q, \overline{Q} | t _{PZL} t _{PZH} | 1.5 3.3 5 | — 5.6 3.7 | 165 19.8 13.2 | — 5.5 3.6 | 181 21.8 14.5 | ns |
| Output Disable to Q, \overline{Q} | t _{PLZ} t _{PHZ} | 1.5 3.3 5 | — 4.7 3.7 | 165 16.5 13.2 | — 4.5 3.6 | 181 18.1 14.5 | ns |
| Power Dissipation Capacitance | C _{PD} § | — | 67 Typ. | | 67 Typ. | | pF |
| Min. (Valley) V _{OH} During Switching of Other Outputs (Output Under Test Not Switching) | V _{OHV} See Fig. 1 | 5 | 4 Typ. @ 25°C | | | | V |
| Max. (Peak) V _{OL} During Switching of Other Outputs (Output Under Test Not Switching) | V _{OLP} See Fig. 1 | 5 | 1 Typ. @ 25°C | | | | V |
| Input Capacitance | C _I | — | — | 10 | — | 10 | pF |
| 3-State Output Capacitance | C _O | — | — | 15 | — | 15 | pF |

*3.3 V: min. is @ 3.6 V

max. is @ 3 V

†5 V: min. is @ 5.5 V

max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per flip flop.

P_D = C_{PD} V_{CC}² f_i + Σ V_{CC}² f_o C_L where f_i = input frequency

f_o = output frequency

C_L = output load capacitance

V_{CC} = supply voltage.

CD54/74AC374, CD54/74AC534 **CD54/74ACT374, CD54/74ACT534**

PREREQUISITE FOR SWITCHING: ACT Series

| CHARACTERISTICS | SYMBOL | V _{CC} (V) | AMBIENT TEMPERATURE (T _A) - °C | | | | UNITS |
|-----------------------------|------------------|------------------------|--|------|-------------|------|-------|
| | | | -40 to +85 | | -55 to +125 | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| Clock Pulse Width | t _w | 5† | 3.9 | — | 4.5 | — | ns |
| Setup Time Data to Clock | t _{su} | 5 | 2 | — | 2 | — | ns |
| Hold Time Data to Clock | t _h | 5 | 2.6 | — | 3 | — | ns |
| Maximum Clock Frequency | f _{max} | 5 | 125 | — | 110 | — | MHz |

†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; $t_r, t_f = 3$ ns, $C_L = 50$ pF

| CHARACTERISTICS | SYMBOL | V _{CC} (V) | AMBIENT TEMPERATURE (T _A) - °C | | | | UNITS |
|---|--|------------------------|--|------|-------------|------|-------|
| | | | -40 to +85 | | -55 to +125 | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| Propagation Delays: Clock to Q ACT374 | t _{PLH} t _{PHL} | 5† | 2.9 | 10.2 | 2.8 | 11.2 | ns |
| Clock to \overline{Q} ACT534 | t _{PLH} t _{PHL} | 5 | 3 | 10.6 | 2.9 | 11.7 | ns |
| Output Enable and Disable to Q ACT374 | t _{PLZ} t _{PHZ} t _{PZL} t _{PZH} | 5 | 3.7 | 13.2 | 3.6 | 14.5 | ns |
| Output Enable and Disable to \overline{Q} ACT534 | t _{PLZ} t _{PHZ} t _{PZL} t _{PZH} | 5 | 3.7 | 13.2 | 3.6 | 14.5 | ns |
| Power Dissipation Capacitance | C _{PD} § | — | 67 Typ. | | 67 Typ. | | pF |
| Min. (Valley) V _{OH} During Switching of Other Outputs (Output Under Test Not Switching) | V _{OHV} See Fig. 1 | 5 | 4 Typ. @ 25°C | | | | V |
| Max. (Peak) V _{OL} During Switching of Other Outputs (Output Under Test Not Switching) | V _{OLP} See Fig. 1 | 5 | 1 Typ. @ 25°C | | | | V |
| Input Capacitance | C _i | — | — | 10 | — | 10 | pF |
| 3-State Output Capacitance | C _o | — | — | 15 | — | 15 | pF |

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§ C_{PD} is used to determine the dynamic power consumption, per flip flop.

 $P_D = C_{PD} V_{CC}^2 f_i + V_{CC}^2 f_o C_L + V_{CC} \Delta I_{CC}$ where f_i = input frequency
 f_o = output frequency
 C_L = output load capacitance
 V_{CC} = supply voltage.

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CD54AC374F3A | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | Level-NC-NC-NC |
| CD54ACT374F3A | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | Level-NC-NC-NC |
| CD54ACT534F3A | OBSOLETE | CDIP | J | 20 | | TBD | Call TI | Call TI |
| CD74AC374E | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| CD74AC374EE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| CD74AC374M | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC374M96 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC374M96E4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC374ME4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC534M96 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC534M96E4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT374E | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| CD74ACT374M | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT374M96 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT374M96E4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT374ME4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| PINS ** DIM | 14 | 16 | 18 | 20 |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

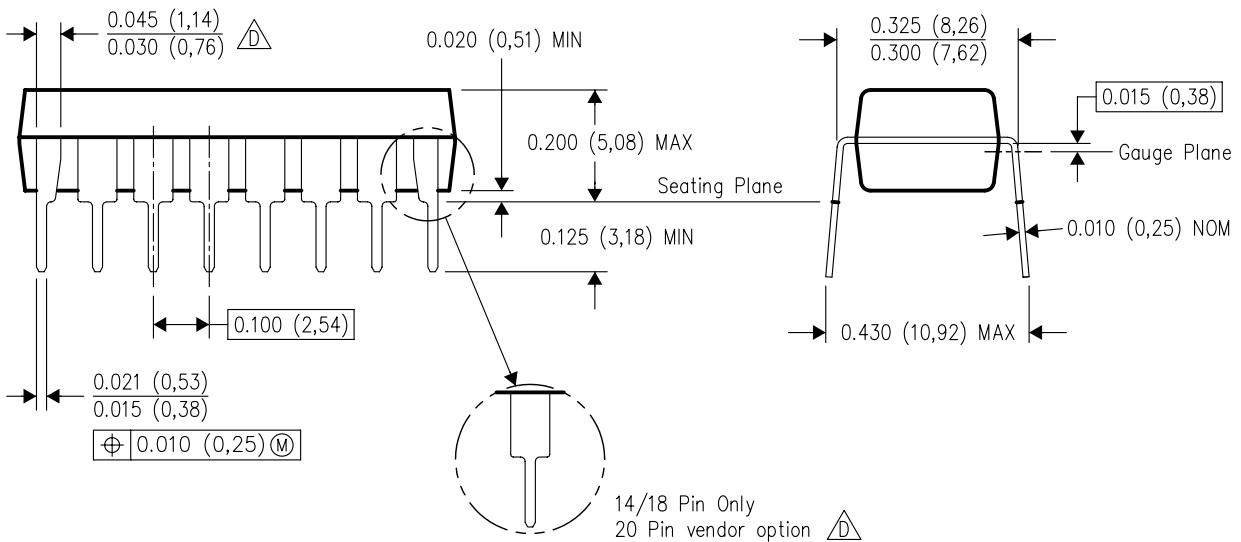
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



| PINS ** | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| DIM | | | | |
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



4040000-4/F 06/2004

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AC.

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