



Data sheet acquired from Harris Semiconductor  
SCHS245

September 1998

# CD74AC245, CD74ACT245

## Octal-Bus Transceiver, Three-State, Non-Inverting

### Features

- Buffered Inputs
- Typical Propagation Delay
  - 4ns at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 50pF$
- Exceeds 2kV ESD Protection MIL-STD-883, Method 3015
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S with Significantly Reduced Power Consumption
- Balanced Propagation Delays
- AC Types Feature 1.5V to 5.5V Operation and Balanced Noise Immunity at 30% of the Supply
- $\pm 24mA$  Output Drive Current
  - Fanout to 15 FAST™ ICs
  - Drives 50 $\Omega$  Transmission Lines

### Description

The CD74AC245 and CD74ACT245 are octal-bus transceivers that utilize the Harris Advanced CMOS Logic technology. They are non-inverting three-state bidirectional transceiver-buffers intended for two-way transmission from "A" bus to "B" bus or "B" bus to "A". The logic level present on the direction input (DIR) determines the data direction. When the output enable input (OE) is HIGH, the outputs are in the high-impedance state.

### Ordering Information

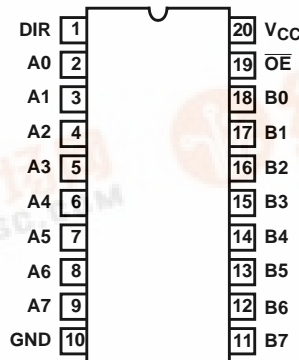
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74AC245E	-55 to 125	20 Ld PDIP	E20.3
CD74ACT245E	-55 to 125	20 Ld PDIP	E20.3
CD74AC245M	-55 to 125	20 Ld SOIC	M20.3
CD74ACT245M	-55 to 125	20 Ld SOIC	M20.3
CD74AC245SM	-55 to 125	20 Ld SSOP	M20.15
CD74ACT245SM	-55 to 125	20 Ld SSOP	M20.15

#### NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

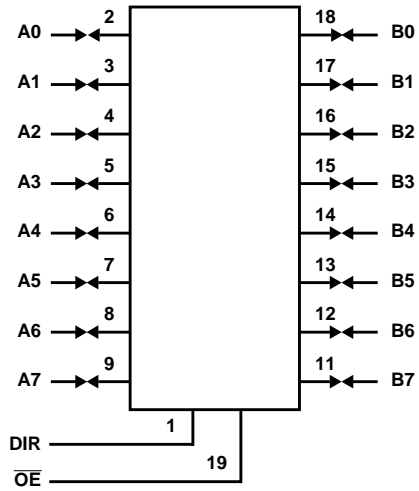
### Pinout

CD74AC245, CD74ACT245  
(PDIP, SSOP, SOIC)  
TOP VIEW



## CD74AC245, CD74ACT245

### Functional Diagram



**TRUTH TABLE**

CONTROL INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

H = High Level, L = Low Level, X = Irrelevant  
 To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

## CD74AC245, CD74ACT245

### Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 6V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 50mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 50mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ (Note 3) .....	$\pm 100mA$

### Thermal Information

Thermal Resistance (Typical, Note 5)	$\theta_{JA}$ ( $^{\circ}C/W$ )
PDIP Package .....	125
SOIC Package .....	120
SSOP Package .....	130
Maximum Junction Temperature (Plastic Package) .....	$150^{\circ}C$
Maximum Storage Temperature Range .....	$-65^{\circ}C$ to $150^{\circ}C$
Maximum Lead Temperature (Soldering 10s) .....	$300^{\circ}C$

### Operating Conditions

Temperature Range, $T_A$ .....	$-55^{\circ}C$ to $125^{\circ}C$
Supply Voltage Range, $V_{CC}$ (Note 4)	
AC Types .....	1.5V to 5.5V
ACT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I$ , $V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Slew Rate, $dt/dv$	
AC Types, 1.5V to 3V .....	50ns (Max)
AC Types, 3.6V to 5.5V .....	20ns (Max)
ACT Types, 4.5V to 5.5V .....	10ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

#### NOTES:

3. For up to 4 outputs per device, add  $\pm 25mA$  for each additional output.
4. Unless otherwise specified, all voltages are referenced to ground.
5.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

### DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$		-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS	
		$V_I$ (V)	$I_O$ (mA)		MIN	MAX	MIN	MAX	MIN	MAX		
<b>AC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	1.5	1.2	-	1.2	-	1.2	-	V	
				3	2.1	-	2.1	-	2.1	-	V	
				5.5	3.85	-	3.85	-	3.85	-	V	
Low Level Input Voltage	$V_{IL}$	-	-	1.5	-	0.3	-	0.3	-	0.3	V	
				3	-	0.9	-	0.9	-	0.9	V	
				5.5	-	1.65	-	1.65	-	1.65	V	
High Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.05	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
			-0.05	-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-4	-4	3	2.58	-	2.48	-	2.4	-	V
			-24	-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V
-50 (Note 6, 7)	-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V			

## CD74AC245, CD74ACT245

### DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
Low Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	-	5.5	-	±0.1	-	±1	-	±1	μA
Three-State Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND	-	5.5	-	±0.5	-	±5	-	±10	μA
Quiescent Supply Current MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	8	-	80	-	160	μA
<b>ACT TYPES</b>											
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V
Low Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	-	5.5	-	±0.1	-	±1	-	±1	μA
Three-State or Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND	-	5.5	-	±0.5	-	±5	-	±10	μA
Quiescent Supply Current MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	8	-	80	-	160	μA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	2.4	-	2.8	-	3	mA

**NOTES:**

6. Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
7. Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

## CD74AC245, CD74ACT245

### ACT Input Load Table

INPUT	UNIT LOAD
An, Bn	0.83
$\overline{OE}$	0.64
DIR	0.15

NOTE: Unit load is  $\Delta I_{CC}$  limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

### Switching Specifications Input $t_r, t_f = 3ns, C_L = 50pF$ (Worst Case)

PARAMETER	SYMBOL	$V_{CC}$ (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>AC TYPES</b>									
Propagation Delay, Data to Output	$t_{PLH}, t_{PHL}$	1.5	-	-	96	-	-	106	ns
		3.3 (Note 9)	3.2	-	10.8	3	-	11.9	ns
		5 (Note 10)	2.2	-	7.7	2.1	-	8.5	ns
Propagation Delay, Output Disable to Output	$t_{PLZ}, t_{PHZ}$	1.5	-	-	159	-	-	175	ns
		3.3	4.7	-	15.9	4.4	-	17.5	ns
		5	3.7	-	12.7	3.5	-	14	ns
Propagation Delay, Output Enable to Output	$t_{PZL}, t_{PZH}$	1.5	-	-	159	-	-	175	ns
		3.3	5.6	-	19	5.3	-	21	ns
		5	3.7	-	12.7	3.5	-	14	ns
Minimum (Valley) $V_{OH}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OHV}$ See Figure 1	5	-	4 at 25°C	-	-	4 at 25°C	-	V
Maximum (Peak) $V_{OL}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OLP}$ See Figure 1	5	-	1 at 25°C	-	-	1 at 25°C	-	V
Three-State Output Capacitance	$C_O$	-	-	15	-	-	15	-	pF
Input Capacitance	$C_I$	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	$C_{PD}$ (Note 11)	-	-	57	-	-	57	-	pF
<b>ACT TYPES</b>									
Propagation Delay, Data to Output	$t_{PLH}, t_{PHL}$	5 (Note 10)	2.7	-	9.1	2.5	-	10	ns
Propagation Delay, Output Disable to Output	$t_{PLZ}, t_{PHZ}$	5	3.7	-	12.7	3.5	-	14	ns
Propagation Delay, Output Enable to Output	$t_{PZL}, t_{PZH}$	5	3.8	-	13.1	3.6	-	14.4	ns
Minimum (Valley) $V_{OH}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OHV}$ See Figure 1	5	-	4 at 25°C	-	-	4 at 25°C	-	V
Maximum (Peak) $V_{OL}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OLP}$ See Figure 1	5	-	1 at 25°C	-	-	1 at 25°C	-	V

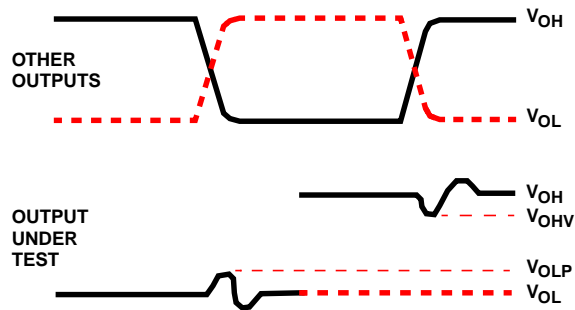
## CD74AC245, CD74ACT245

### Switching Specifications Input $t_r$ , $t_f = 3\text{ns}$ , $C_L = 50\text{pF}$ (Worst Case) (Continued)

PARAMETER	SYMBOL	$V_{CC}$ (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Three-State Output Capacitance	$C_O$	-	-	15	-	-	15	-	pF
Input Capacitance	$C_I$	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	$C_{PD}$ (Note 11)	-	-	57	-	-	57	-	pF

**NOTES:**

8. Limits tested 100%.
9. 3.3V Min is at 3.6V, Max is at 3V.
10. 5V Min is at 5.5V, Max is at 4.5V
11.  $C_{PD}$  is used to determine the dynamic power consumption per channel.  
 AC:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$   
 ACT:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

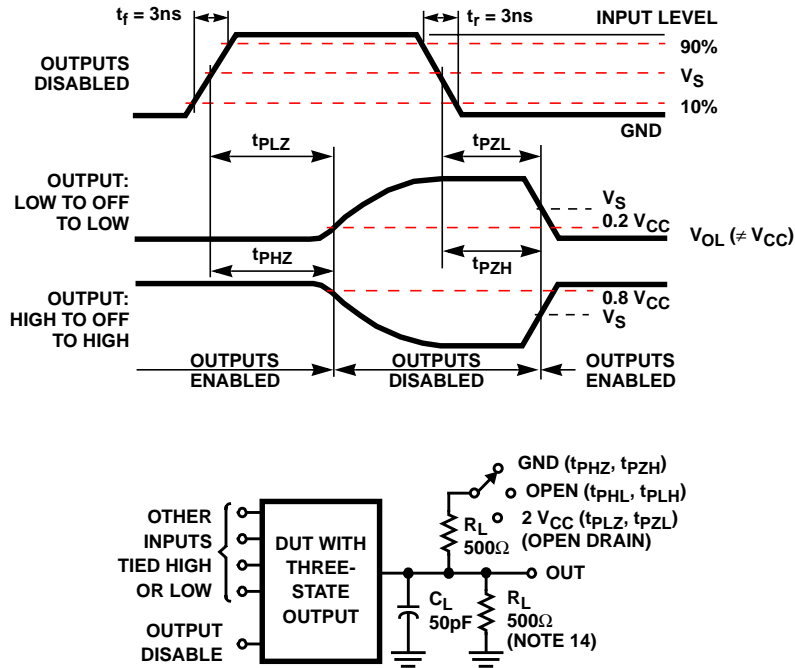


**NOTES:**

12. Input pulses have the following characteristics:  $PRR \leq 1\text{MHz}$ ,  $t_r = 3\text{ns}$ , SKEW 1ns.
13. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with  $0.1\mu\text{F}$  capacitor. Scope and probes require 700MHz bandwidth.

**FIGURE 1. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS**

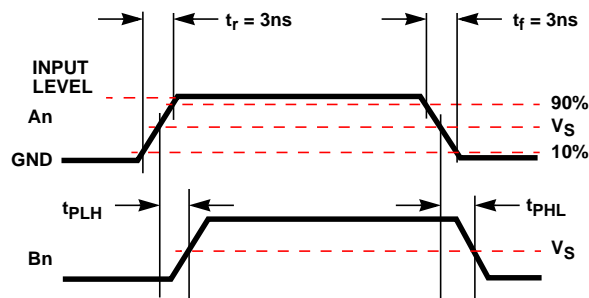
## CD74AC245, CD74ACT245



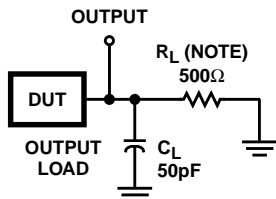
NOTE:

14. For AC Series only: When  $V_{CC} = 1.5\text{V}$ ,  $R_L = 1\text{k}\Omega$ .

**FIGURE 2. THREE-STATE PROPAGATION DELAY TIMES AND TEST CIRCUIT**



**FIGURE 3. PROPAGATION DELAY TIMES**



NOTE: For AC Series Only: When  $V_{CC} = 1.5\text{V}$ ,  $R_L = 1\text{k}\Omega$ .

	CD74AC	CD74ACT
Input Level	$V_{CC}$	3V
Input Switching Voltage, $V_S$	$0.5 V_{CC}$	1.5V
Output Switching Voltage, $V_S$	$0.5 V_{CC}$	$0.5 V_{CC}$

**FIGURE 4. PROPAGATION DELAY TIMES**

## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.