CD54ACT138, CD74ACT138 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

SCHS329A - JANUARY 2003 - REVISED FEBRUARY 2003

- Inputs Are TTL-Voltage Compatible
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Designed Specifically for High-Speed Memory Decoders and Data-Transmission Systems
- Incorporate Three Enable Inputs to Simplify Cascading and/or Data Reception
- Balanced Propagation Delays
- ±24-mA Output Drive Current
 Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015

CD54ACT138...F PACKAGE CD74ACT138...E OR M PACKAGE (TOP VIEW) 16 V_{CC} В П2 15 Y0 СΠ 14 TY1 **G**2A **∏**4 13 Y2 12 Y3 G2B [5 G1 **∏**6 11 TY4 Y7 🛮 7 10 Y5 9 Y6 GND 8

description/ordering information

The 'ACT138 decoders/demultiplexers are designed for high-performance memory-decoding and data-routing applications that require very short propagation-delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications (see Application Information).

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
PDIP – E		Tube	CD74ACT138E	CD74ACT138E
–55°C to 125°C	SOIC – M	Tube	CD74ACT138M	ACT138M
	301C – W	Tape and reel	CD74ACT138M96	ACTISON
	CDIP – F	Tube	CD54ACT138F3A	CD54ACT138F3A

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

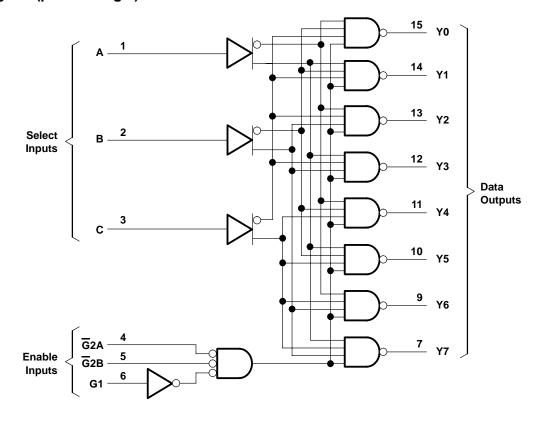


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ГU	IV	u		u	N	- 1/4	н	0	ᆫ	_

ENA	BLE INF	PUTS	SEL	ECT INP	UTS				OUT	PUTS			
G1	G2A	G2B	С	В	Α	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
Х	Н	Х	Х	Χ	Х	Н	Н	Н	Н	Н	Н	Н	Н
Х	X	Н	Х	X	X	Н	Н	Н	Н	Н	Н	Н	Н
L	X	X	Х	Χ	X	Н	Н	Н	Н	Н	Н	Н	Н
Н	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
Н	L	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н
Н	L	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н
Н	L	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
Н	L	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н
Н	L	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н
Н	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н
Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L

logic diagram (positive logic)



CD54ACT138, CD74ACT138 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 6 V
Input clamp current, I_{IK} ($V_I < 0 \text{ V or } V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I _{OK} (V _O < 0 V or V _O > V _{CC}) (see Note 1)	±50 mA
Continuous output current, I _O (V _O > 0 V or V _O < V _{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 2): E package	67°C/W
M package	73°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

		T _A =	25°C	–55°C to 125°C		–40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
VCC	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2		2		2		V
V _{IL}	Low-level input voltage		0.8		8.0		0.8	V
٧ _I	Input voltage	0	VCC	0	VCC	0	VCC	V
Vo	Output voltage	0	VCC	0	VCC	0	VCC	V
loh	High-level output current		-24		-24		-24	mA
l _{OL}	Low-level output current		24		24		24	mA
Δt/Δν	Input transition rise or fall rate		10		10		10	ns/V

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST COND	vcc	T _A = 25°C		–55°C to 125°C		–40°C to 85°C		UNIT		
			MIN	MAX	MIN	MAX	MIN	MAX			
		I _{OH} = -50 μA	4.5 V	4.4		4.4		4.4			
V	\\\. = \\\. \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94		3.7		3.8		٧	
VOH	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -50 \text{ mA}^{\dagger}$	5.5 V			3.85				V	
		$I_{OH} = -75 \text{ mA}^{\dagger}$	5.5 V					3.85			
	VI = VIH or VIL	I _{OL} = 50 μA	4.5 V		0.1		0.1		0.1	 	
Val		I _{OL} = 24 mA	4.5 V		0.36		0.5		0.44		
VOL		I _{OL} = 50 mA [†]	5.5 V				1.65				
		$I_{OL} = 75 \text{ mA}^{\dagger}$	5.5 V						1.65		
lį	$V_I = V_{CC}$ or GND		5.5 V		±0.1		±1		±1	μΑ	
ICC	$V_I = V_{CC}$ or GND,	IO = 0	5.5 V		8		160		80	μΑ	
ΔI _{CC} ‡	$V_{I} = V_{CC} - 2.1 \text{ V}$		4.5 V to 5.5 V		2.4		3		2.8	mA	
C _i					10		10		10	pF	

[†] Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C. ‡ Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

ACT INPUT LOAD TABLE

INPUT	UNIT LOAD
A, B, or C	0.83
G2A or G2B	1
G1	0.42

Unit Load is ΔI_{CC} limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55° 125		–40°C to 85°C		UNIT
	(1141 01)	(0011 01)	MIN	MAX	MIN	MAX	
^t PLH	A, B, C	Any Y	3	12	3.1	10.9	20
^t PHL	А, В, С	Ally 1	3	12	3.1	10.9	ns
^t PLH	04	Any Y	2.8	11	2.8	10	ns
tPHL	G1	Ally 1	2.8	11	2.8	10	115
t _{PLH}	<u></u>	Any	2.6	10.5	2.7	9.5	nc
t _{PHL}	G2A, G2B	Any Y	2.6	10.5	2.7	9.5	ns

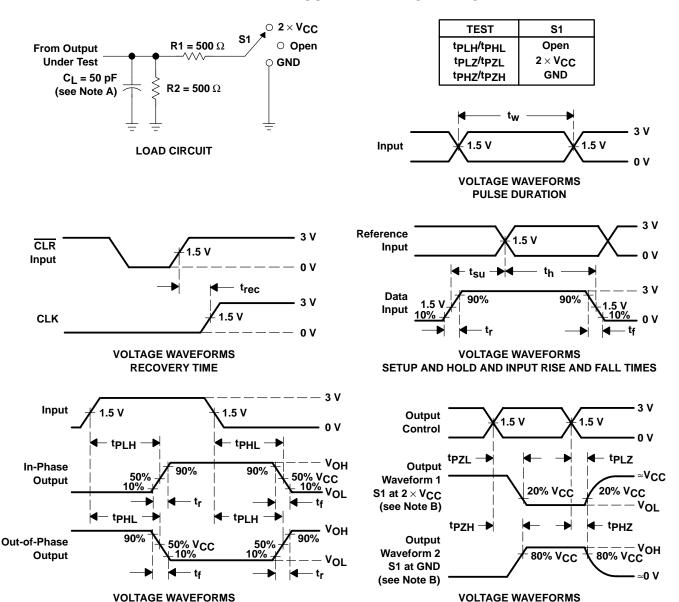
operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TYP	UNIT
C _{pd}	Power dissipation capacitance	110	pF



OUTPUT ENABLE AND DISABLE TIMES

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.

PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \ \Omega$, $t_f = 3 \ ns$, $t_f = 3 \ ns$. Phase relationships between waveforms are arbitrary.
- D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
- E. The outputs are measured one at a time with one input transition per measurement.
- F. tpLH and tpHL are the same as tpd.
- G. tpz and tpzH are the same as ten.
- H. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- I. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



APPLICATION INFORMATION

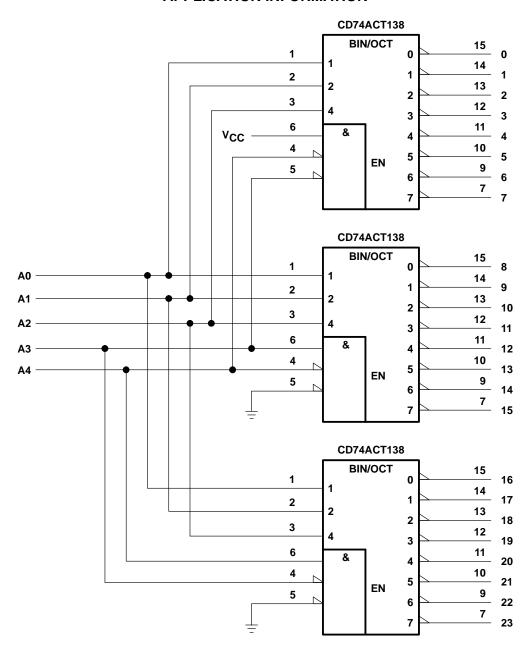


Figure 2. 24-Bit Decoding Scheme

APPLICATION INFORMATION

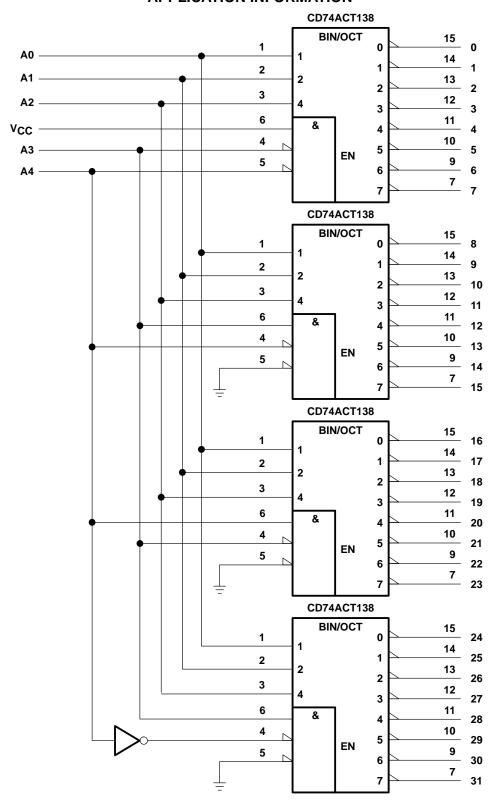


Figure 3. 32-Bit Decoding Scheme



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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD54ACT138F3A	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD74ACT138E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74ACT138EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74ACT138M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT138M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT138M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT138M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT138ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT138MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

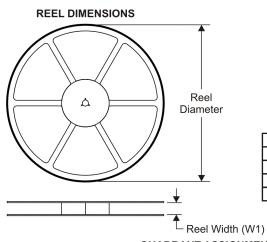
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

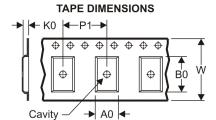
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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

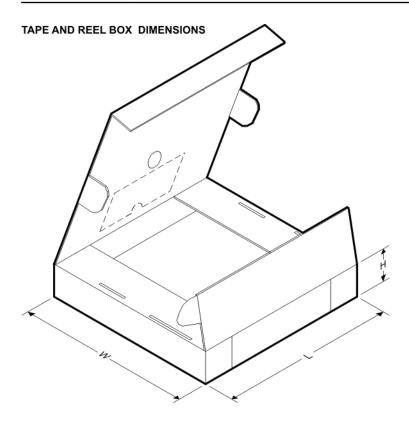
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74ACT138M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74ACT138M96	SOIC	D	16	2500	333.2	345.9	28.6

14 LEADS SHOWN

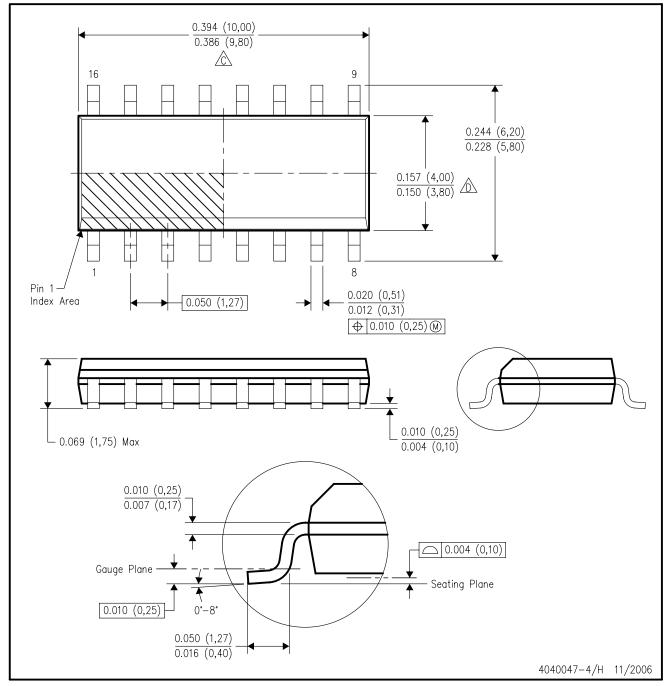


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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