CD54HC297, CD74HC297, CD74HCT297

Data sheet acquired from Harris Semiconductor
SCHS177B

November 1997 - Revised May 2003

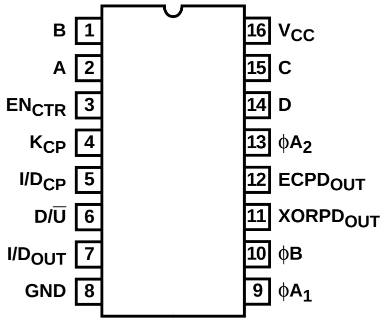
High-Speed CMOS Logic Digital Phase-Locked Loop

Features

- **Digital Design Avoids Analog Compensation Errors**
- **Easily Cascadable for Higher Order Loops**
- **Useful Frequency Range**
  - **K-Clock . . . . .DC to 55MHz (Typ)**
  - **I/D-Clock . . . . DC to 35MHz (Typ)**
- **Dynamically Variable Bandwidth**
- **Very Narrow Bandwidth Attainable**
- **Power-On Reset**
- **Output Capability**
  - **Standard . . . . $XORPD_{OUT}$, $ECPD_{OUT}$**
  - **Bus Driver . . . . I/D_{OUT}**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . 15 LSTTL Loads**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **’HC297 Types**
  - **Operation Voltage . . . . 2 to 6V**
  - **High Noise Immunity $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at 5V**
- **CD74HCT297 Types**
  - **Operation Voltage . . . . .4.5 to 5.5V**
  - **Direct LSTTL Input Logic Compatibility $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)**
  - **CMOS Input Compatibility $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Pinout

CD54HC297
(CERDIP)
CD74HC297, CD74HCT29
(PDIP)
TOP VIEW



Description

The ’HC297 and CD74HCT297 are high-speed silicon gate CMOS devices that are pin-compatible with low power Schottky TTL (LSTTL).

These devices are designed to provide a simple, cost-effective solution to high-accuracy, digital, phase-locked-loop applications. They contain all the necessary circuits, with the exception of the divide-by-N counter, to build first-order phase-locked-loops.

Both EXCLUSIVE-OR (XORPD) and edge-controlled phase detectors (ECPD) are provided for maximum flexibility. The input signals for the EXCLUSIVE-OR phase detector must have a 50% duty factor to obtain the maximum lock-range.

Proper partitioning of the loop function, with many of the building blocks external to the package, makes it easy for the designer to incorporate ripple cancellation (see Figure 2) or to cascade to higher order phase-locked-loops.

The length of the up/down K-counter is digitally programmable according to the K-counter function table. With A, B, C and D all LOW, the K-counter is disabled. With A HIGH and B, C and D LOW, the K-counter is only three stages long, which widens the bandwidth or capture range and shortens the lock time of the loop. When A, B, C and D are all programmed HIGH, the K-counter becomes seventeen stages long, which narrows the bandwidth or capture range and lengthens the lock time. Real-time control of loop bandwidth by manipulating the A to D inputs can maximize the overall performance of the digital phase-locked-loop.

The ’HC297 and CD74HCT297 can perform the classic first order phase-locked-loop function without using analog components. The accuracy of the digital phase-locked-loop (DPLL) is not affected by V_{CC} and temperature variations but depends solely on accuracies of the K-clock and loop propagation delays.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE
CD54HC297F3A	-55 to 125	16 Ld CERDIP
CD74HC297E	-55 to 125	16 Ld PDIP
CD74HCT297E	-55 to 125	16 Ld PDIP

The phase detector generates an error signal waveform that, at zero phase error, is a 50% duty factor square wave. At the limits of linear operation, the phase detector output will be either HIGH or LOW all of the time depending on the direction of the phase error (ϕIN - ϕOUT). Within these limits the phase detector output varies linearly with the input phase error according to the gain K_d, which is expressed in terms of phase detector output per cycle or phase error. The phase detector output can be defined to vary between ±1 according to the relation:

$$\text{phase detector output} = \frac{\%\text{HIGH} - \%\text{LOW}}{100}$$

The output of the phase detector will be $K_d \phi_e$, where the phase error $\phi_e = \phi\text{IN} - \phi\text{OUT}$.

EXCLUSIVE-OR phase detectors (XORPD) and edge-controlled phase detectors (ECPD) are commonly used digital types. The ECPD is more complex than the XORPD logic function but can be described generally as a circuit that changes states on one of the transitions of its inputs. The gain (K_d) for an XORPD is 4 because its output remains HIGH ($\text{XORPD}_{\text{OUT}}$ = 1) for a phase error of one quarter cycle.

Similarly, K_d for the ECPD is 2 since its output remains HIGH for a phase error of one half cycle. The type of phase detector will determine the zero-phase-error point, i.e., the phase separation of the phase detector inputs for a ϕe defined to be zero. For the basic DPLL system of Figure 3, ϕe = 0 when the phase detector output is a square wave.

The XORPD inputs are one quarter cycle out-of-phase for zero phase error. For the ECPD, ϕe = 0 when the inputs are one half cycle out of phase.

The phase detector output controls the up/down input to the K-counter. The counter is clocked by input frequency Mf_c which is a multiple M of the loop center frequency f_c. When the K-counter recycles up, it generates a carry pulse. Recycling while counting down generates a borrow pulse. If the carry and the borrow outputs are conceptually combined into one output that is positive for a carry and negative for a borrow, and if the K-counter is considered as a frequency divider with the ratio Mf_c/K, the output of the K-counter will equal the input frequency multiplied by the division ratio. Thus the output from the K-counter is $(K_d \phi_e Mf_c)/K$.

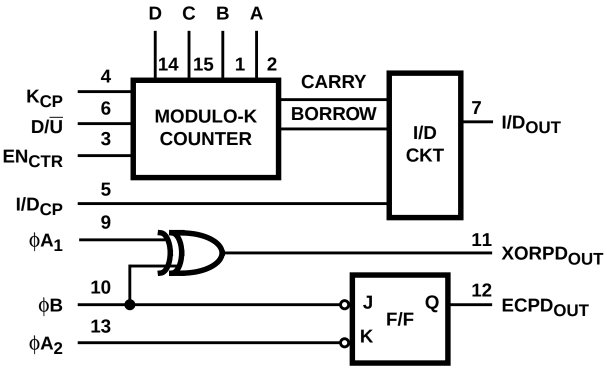
The carry and borrow pulses go to the increment/decrement (I/D) circuit which, in the absence of any carry or borrow pulses has an output that is one half of the input clock (I/D_{CP}). The input clock is just a multiple, 2N, of the loop center frequency. In response to a carry of borrow pulse, the I/D circuit will either add or delete a pulse at I/D_{OUT}. Thus the output of the I/D circuit will be $Nf_c + (K_d \phi_e Mf_c)/2K$.

The output of the N-counter (or the output of the phase-locked-loop) is thus: $f_o = f_c + (K_d \phi_e Mf_c)/2KN$.

If this result is compared to the equation for a first-order analog phase-locked-loop, the digital equivalent of the gain of the VCO is just $Mf_c/2KN$ or f_c/K for M = 2N.

Thus, the simple first-order phase-locked-loop with an adjustable K-counter is the equivalent of an analog phase-locked-loop with a programmable VCO gain.

Functional Diagram



FUNCTION TABLE
EXCLUSIVE-OR PHASE DETECTOR

ϕA_1	ϕB	XORPD OUT
L	L	L
L	H	H
H	L	H
H	H	L

FUNCTION TABLE
EDGE-CONTROLLED PHASE DETECTOR

ϕA_2	ϕB	ECPD OUT
H or L	↓	H
↓	H or L	L
H or L	↑	No Change
↑	H or L	No Change

H = Steady-State High Level, L = Steady-State Low Level, ↑ = LOW to HIGH ϕ Transition, ↓ = HIGH to LOW ϕ Transition

K-COUNTER FUNCTION TABLE
(DIGITAL CONTROL)

D	C	B	A	MODULO (K)
L	L	L	L	Inhibited
L	L	L	H	2^3
L	L	H	L	2^4
L	L	H	H	2^5
L	H	L	L	2^6
L	H	L	H	2^7
L	H	H	L	2^8
L	H	H	H	2^9
H	L	L	L	2^{10}
H	L	L	H	2^{11}
H	L	H	L	2^{12}
H	L	H	H	2^{13}
H	H	L	L	2^{14}
H	H	L	H	2^{15}
H	H	H	L	2^{16}
H	H	H	H	2^{17}

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
  For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . ±20mA
DC Output Diode Current, I_{OK}
  For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . ±20mA
DC Drain Current, per Output, I_O
  For -0.5V < V_O < V_{CC} + 0.5V . . . . ±25mA
DC Output Source or Sink Current per Output Pin, I_O
  For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . ±50mA

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
  E (PDIP) Package 67
Maximum Junction Temperature . . . . 150^oC
Maximum Storage Temperature Range . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . 300^oC

Operating Conditions

Temperature Range, T_A . . . . -55^oC to 125^oC
Supply Voltage Range, V_{CC}
  HC Types . . . . 2V to 6V
  HCT Types . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . 0V to V_{CC}
Input Rise and Fall Time
  2V . . . . 1000ns (Max)
  4.5V . . . . 500ns (Max)
  6V . . . . 400ns (Max)

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

		TEST CONDITIONS			25^oC			-40^oC TO 85^oC		-55^oC TO 125^oC		
PARAMETER	**SYMBOL**	**V_I (V)**	**I_O (mA)**	**V_{CC} (V)**	**MIN**	**TYP**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-6 (Note 2)	4.5	3.98	-	-	3.84	-	3.7	-	V
			-7.8 (Note 2)	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4 (Note 2)	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2 (Note 2)	6	-	-	0.26	-	0.33	-	0.4	V

DC Electrical Specifications **(Continued)**

		TEST CONDITIONS			25^{o}C			-40^{o}C TO 85^{o}C		-55^{o}C TO 125^{o}C		
PARAMETER	**SYMBOL**	**V_I (V)**	**I_O (mA)**	**V_{CC} (V)**	**MIN**	**TYP**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} to GND	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 2)	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
EN_{CTR}, $D/\overline{U}$	0.3
A, B, C, D, K_{CP}, ϕA_2	0.6
I/D_{CP}, ϕA_1, ϕB	1.5

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360µA max at 25^{o}C.

Prerequisite For Switching Function

PARAMETER	SYMBOL	V_{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
HC TYPES									
Maximum Clock Frequency K_{CP}	f_{MAX}	2	6	-	5	-	4	-	MHz
		4.5	30	-	24	-	20	-	MHz
		6	35	-	28	-	24	-	MHz
Maximum Clock Frequency I/D_{CP}	f_{MAX}	2	4	-	3	-	2	-	MHz
		4.5	20	-	16	-	13	-	MHz
		6	24	-	19	-	15	-	MHz
Clock Pulse Width K_{CP}	t_w	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
Clock Pulse Width I/D_{CP}	t_W	2	125	-	155	-	190	-	ns
		4.5	25	-	31	-	38	-	ns
		6	21	-	26	-	32	-	ns
Set-up Time $D/\overline{U}$, EN_{CTR} to K_{CP}	t_{SU}	2	100	-	125	-	150	-	ns
		4.5	20	-	25	-	30	-	ns
		6	17	-	21	-	26	-	ns
Hold Time $D/\overline{U}$, EN_{CTR} to K_{CP}	t_H	2	0	-	0	-	0	-	ns
		4.5	0	-	0	-	0	-	ns
		6	0	-	0	-	0	-	ns
HCT TYPES									
Maximum Clock Frequency K_{CP}	f_{MAX}	4.5	30	-	24	-	20	-	MHz
Maximum Clock Frequency I/D_{CP}	f_{MAX}	4.5	20	-	16	-	13	-	MHz
Clock Pulse Width K_{CP}	t_w	4.5	16	-	20	-	24	-	ns
Clock Pulse Width I/D_{CP}	t_w	4.5	25	-	31	-	38	-	ns
Set-up Time $D/\overline{U}$, EN_{CTR} to K_{CP}	t_{SU}	4.5	20	-	25	-	30	-	ns
Hold Time $D/\overline{U}$, EN_{CTR} to K_{CP}	t_H	4.5	0	-	0	-	0	-	ns

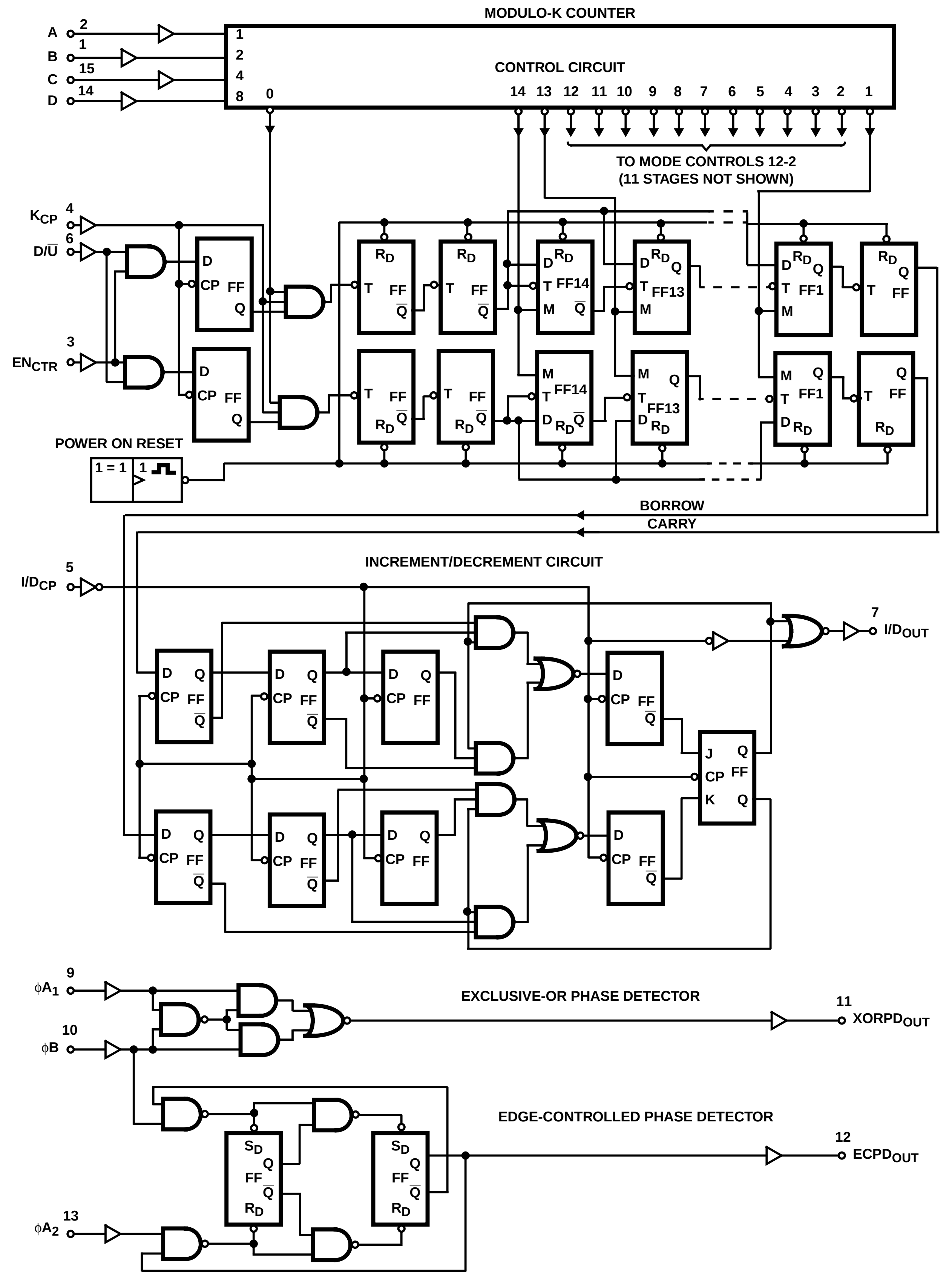
Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
HC TYPES								
Propagation Delay, I/D_{CP} to I/D_{OUT}	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	175	220	265	ns
			4.5	-	35	44	53	ns
			6	-	30	34	43	ns

Switching Specifications Input t_r, t_f = 6ns (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
Propagation Delay, ϕA_1, ϕB to $XORPD_{OUT}$	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	150	190	225	ns
			4.5	-	30	38	45	ns
			6	-	26	33	38	ns
Propagation Delay, ϕB, ϕA_2 to $ECPD_{OUT}$	t_{PHL}, t_{PHL}	C_L = 50pF	2	-	200	250	300	ns
			4.5	-	40	50	60	ns
			6	-	34	43	51	ns
Output Transition Time $XORPD_{OUT}$ $ECPD_{OUT}$	t_{TLH}	C_L = 50pF	2	-	75	95	110	ns
			4.5	-	15	19	22	ns
			6	-	13	16	19	ns
Output Transition Time I/D_{OUT}	t_{TLH}	C_L = 50pF	2	-	60	75	90	ns
			4.5	-	12	15	18	ns
			6	-	10	13	15	ns
Input Capacitance	C_I	-	-	-	10	10	10	pF
HCT TYPES								
Propagation Delay, I/D_{CP} to I/D_{OUT}	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	35	44	53	ns
Propagation Delay, ϕA_1, ϕB to $XORPD_{OUT}$	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	30	38	45	ns
Propagation Delay, ϕB, ϕA_2 to $ECPD_{OUT}$	t_{PHL}, t_{PHL}	C_L = 50pF	4.5	-	40	50	60	ns
Output Transition Time $XORPD_{OUT}$	t_{TLH}	C_L = 50pF	4.5	-	15	19	22	ns
Output Transition Time $ECPD_{OUT}$	t_{TLH}	C_L = 50pF	4.5	-	12	15	18	ns
Input Capacitance	C_I	-	-	-	10	10	10	pF

Logic Diagram



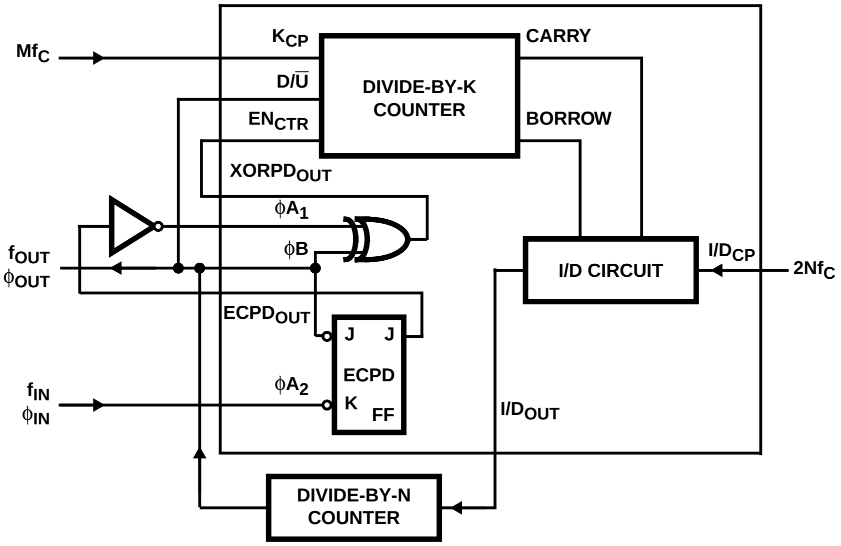


FIGURE 1. DPLL USING BOTH PHASE DETECTORS IN A RIPPLE-CANCELLATION SCHEME

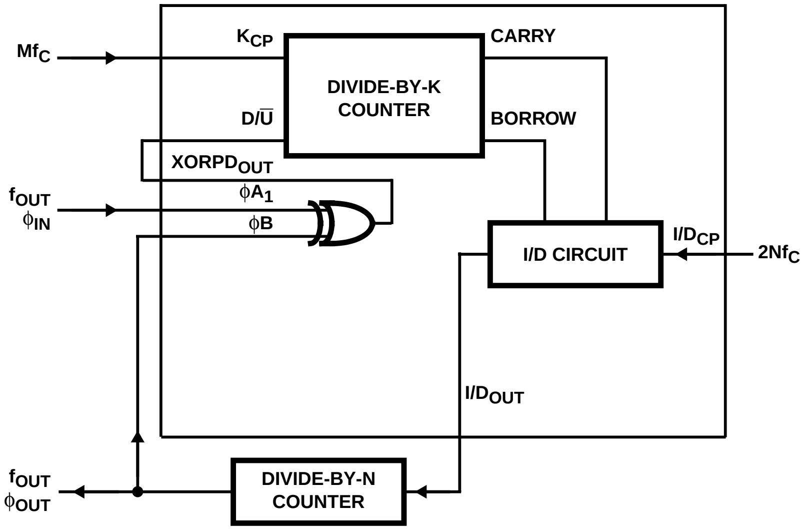


FIGURE 2. DPLL USING EXCLUSIVE-OR PHASE DETECTION

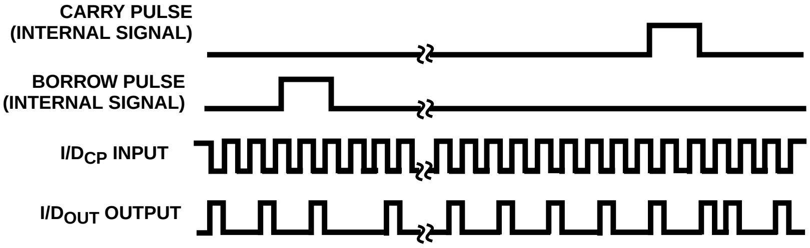


FIGURE 3. TIMING DIAGRAM: I/D_{OUT} IN-LOCK CONDITION

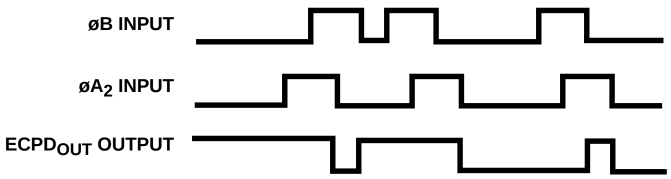


FIGURE 4. TIMING DIAGRAM: EDGE CONTROLLED PHASE COMPARATOR WAVEFORMS

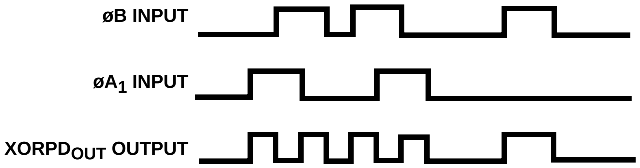


FIGURE 5. TIMING DIAGRAM: EXCLUSIVE OR PHASE DETECTOR WAVEFORMS

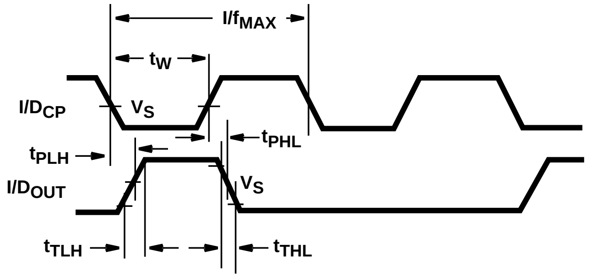


FIGURE 6. WAVEFORMS SHOWING THE CLOCK (I/D$_{CP}$) TO OUTPUT (I/D$_{OUT}$) PROPAGATION DELAYS, CLOCK PULSE WIDTH, OUTPUT TRANSITION TIMES AND MAXIMUM CLOCK PULSE FREQUENCY

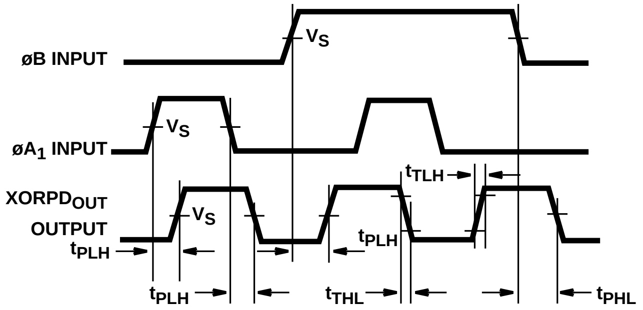


FIGURE 7. WAVEFORMS SHOWING THE PHASE INPUT (øB, øA$_1$) TO OUTPUT (XORPD$_{OUT}$) PROPAGATION DELAYS AND OUTPUT TRANSITION TIMES

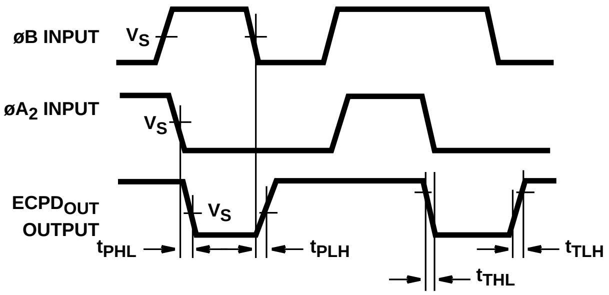
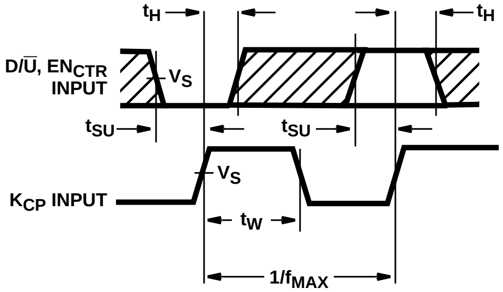


FIGURE 8. WAVEFORMS SHOWING THE PHASE INPUT (øB, $øA_2$) TO OUTPUT ($ECPD_{OUT}$) PROPAGATION DELAYS AND OUTPUT TRANSITION TIMES



NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

FIGURE 9. WAVEFORMS SHOWING THE CLOCK (K_{CP}) PULSE WIDTH AND MAXIMUM CLOCK PULSE FREQUENCY, AND THE INPUT (D/$\overline{U}$, EN_{CTR}) TO CLOCK (K_{CP}) SETUP AND HOLD TIMES

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-8999001EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD54HC297F3A	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD74HC297E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC297EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT297E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT297EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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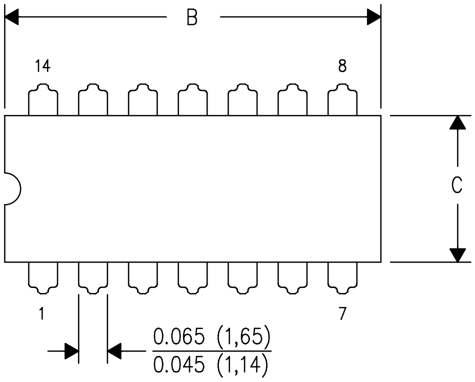
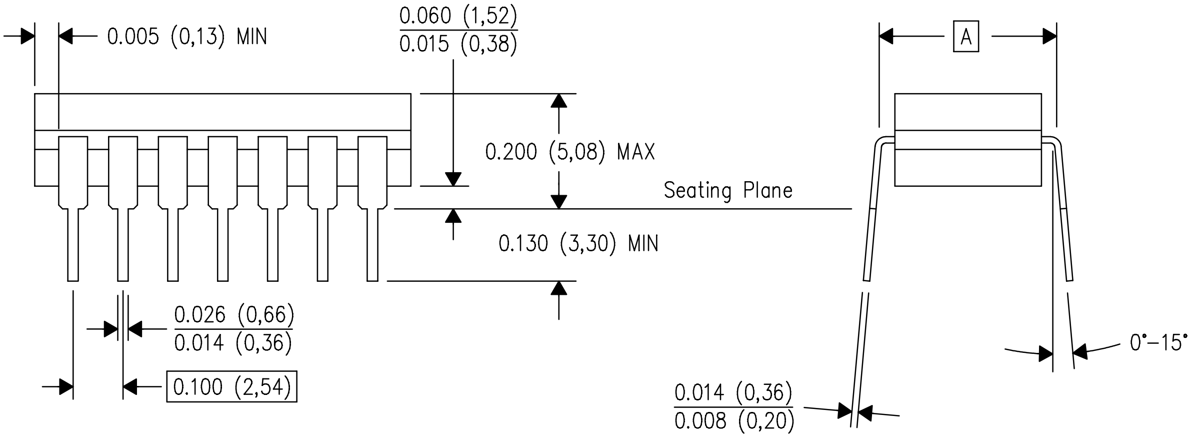
J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



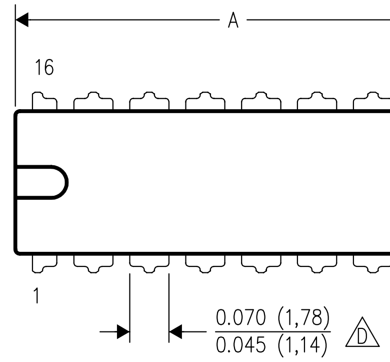


4040083/F 03/03

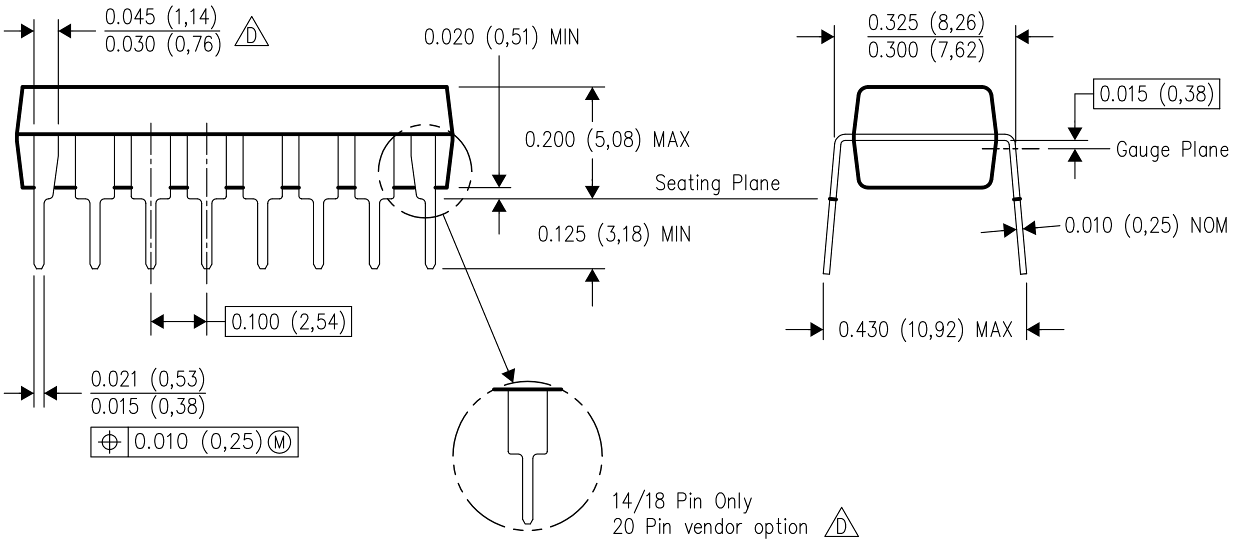
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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