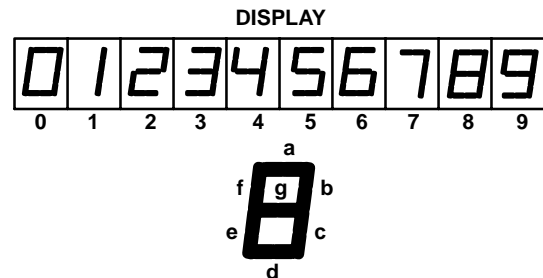
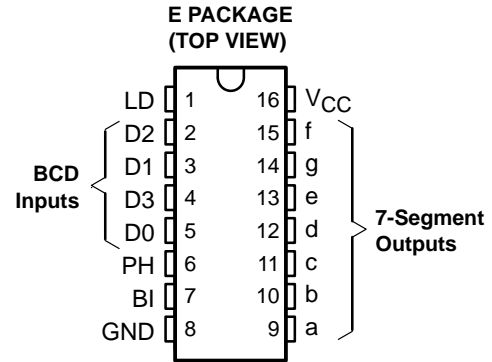


# CD74HCT4543 BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER

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- 4.5-V to 5.5-V  $V_{CC}$  Operation
- Input Latches for BCD Code Storage
- Blanking Capability
- Phase Input for Complementing Outputs
- Fanout (Over Temperature Range)
  - Standard Outputs – 10 LSTTL Loads
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction, Compared to LSTTL Logic ICs
- Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8\text{ V}$  Maximum,  $V_{IH} = 2\text{ V}$  Minimum
- CMOS Input Compatibility,  $I_I \leq 1\ \mu\text{A}$  at  $V_{OL}$ ,  $V_{OH}$



## description/ordering information

The CD74HCT4543 high-speed silicon-gate is a BCD-to-7 segment latch/decoder/driver designed primarily for directly driving liquid-crystal displays. While the latch enable (LD) is low, the latches are enabled to store the BCD inputs. When the latch enable is high, the latches are disabled, making the outputs transparent to the BCD inputs. The device has an active-high blanking input (BI) and a phase input (PH) to which a square wave is applied for liquid-crystal applications. This square wave also is applied to the backplane of the liquid-crystal display.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	PDIP – E	Tube	CD74HCT4543E	CD74HCT4543E

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# CD74HCT4543 BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER

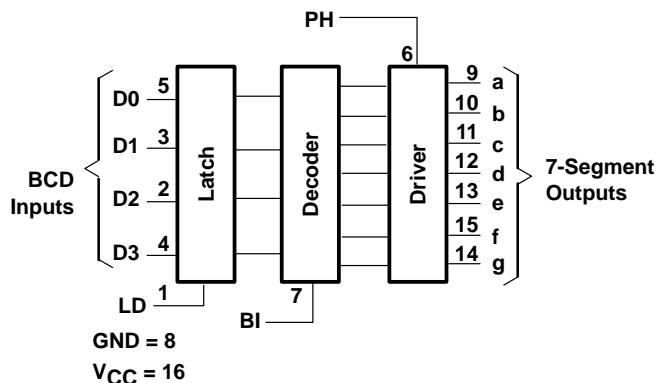
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FUNCTION TABLE

LD	BI	PH	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	a	b	c	d	e	f	g	Display
X	H	L	X	X	X	X	L	L	L	L	L	L	L	Blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	L	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	L	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	L	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	L	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	Blank
L	L	L	X	X	X	X	†							†
As above	H		As above				Inverse of above							As above

† Depends on BCD code previously applied when LD = high.

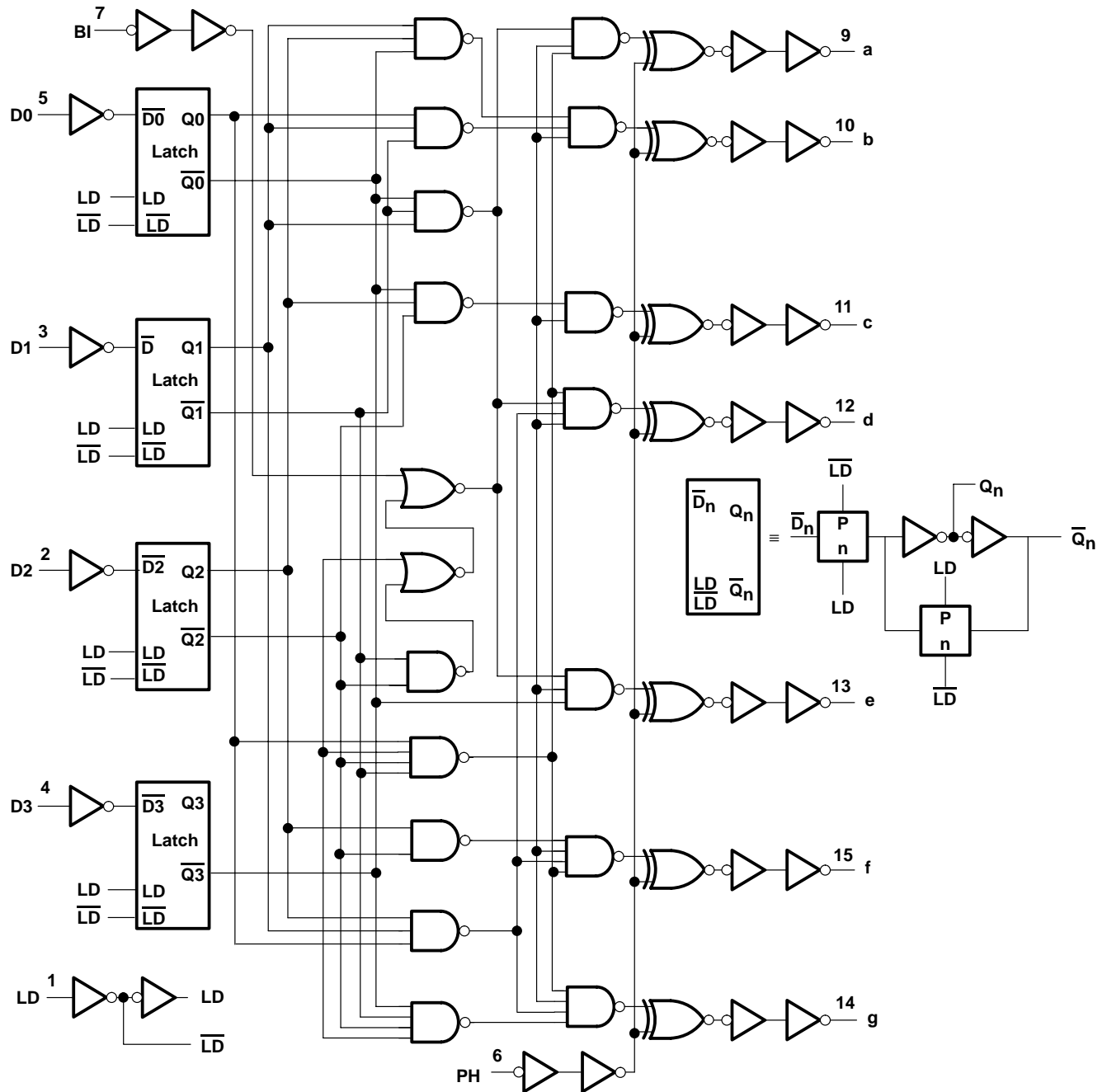
## functional diagram



# CD74HCT4543 BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER

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## logic diagram



# CD74HCT4543

## BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER

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### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input diode current, $I_{IK}$ ( $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) (see Note 1) .....	$\pm 20$ mA
Output diode current, $I_{OK}$ ( $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) (see Note 1) .....	$\pm 20$ mA
Continuous output source or sink current per output, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 50$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2) .....	67°C/W
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum .....	265°C
Unit inserted into a PC board (min. thickness $1/16$ in., 1.59 mm)	
with solder contacting lead tips only .....	300°C
Storage temperature, $T_{stg}$ .....	-65 to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

		$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C}$ TO $125^\circ\text{C}$		$T_A = -40^\circ\text{C}$ TO $85^\circ\text{C}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		2		V
$V_{IL}$	Low-level input voltage	0.8		0.8		0.8		V
$V_I$	Input voltage	$V_{CC}$		$V_{CC}$		$V_{CC}$		V
$V_O$	Output voltage	$V_{CC}$		$V_{CC}$		$V_{CC}$		V
$t_t$	Input transition (rise and fall) time	500		500		500		ns

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -55^\circ\text{C}$ TO $125^\circ\text{C}$		$T_A = -40^\circ\text{C}$ TO $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}$	$I_{OH} = -20 \mu\text{A}$	4.5 V	4.4			4.4		4.4		V
		$I_{OH} = -4 \text{ mA}$		3.98			3.7		3.84		
$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$	$I_{OL} = 20 \mu\text{A}$	4.5 V	0.1			0.1		0.1		V
		$I_{OL} = 4 \text{ mA}$		0.26			0.4		0.33		
$I_I$	$V_I = V_{CC}$ to GND		5.5 V	$\pm 0.1$			$\pm 1$		$\pm 1$		$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or 0, $I_O = 0$		5.5 V	8			160		80		$\mu\text{A}$
$\Delta I_{CC}^\ddagger$	One input at $V_{CC} - 2.1$ V, Other inputs at 0 or $V_{CC}$		4.5 V to 5.5 V	100 360			490		450		$\mu\text{A}$
$C_i$				10			10		10		pF

‡ Additional quiescent supply current per input pin, TTL inputs high, 1 unit load. For dual-supply systems, theoretical worst-case ( $V_I = 2.4$  V,  $V_{CC} = 5.5$  V) specification is 1.8 mA.



**HCT INPUT LOADING TABLE**

INPUT	UNIT LOADS†
D0, D1, D2	1
D3, BI	0.5
PH	1.25
LD	1.5

† Unit Load is  $\Delta I_{CC}$  limit specified in electrical characteristics table, e.g., 360  $\mu$ A maximum at 25°C.

**timing requirements over recommended operating free-air temperature range  $V_{CC} = 4.5$  V (unless otherwise noted) (see Figure 1)**

		$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C}$ TO $125^\circ\text{C}$		$T_A = -40^\circ\text{C}$ TO $85^\circ\text{C}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration, LD high	10		15		13		ns
$t_{su}$	Setup time, BCD inputs before LD↓	12		18		15		ns
$t_h$	Hold time, BCD inputs before LD↓	8		12		10		ns

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -55^\circ\text{C}$ TO $125^\circ\text{C}$		$T_A = -40^\circ\text{C}$ TO $85^\circ\text{C}$		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	$D_n$	Output	$C_L = 50$ pF	4.5 V			80		120		100	ns
			$C_L = 15$ pF	5 V			33					
	LD	Output	$C_L = 50$ pF	4.5 V			77		116		96	
			$C_L = 15$ pF	5 V			32					
	BI	Output	$C_L = 50$ pF	4.5 V			66		99		83	
			$C_L = 15$ pF	5 V			27					
	PH	Output	$C_L = 50$ pF	4.5 V			66		99		83	
			$C_L = 15$ pF	5 V			27					
$t_t$		Any	$C_L = 50$ pF	4.5 V			50		75		63	ns

**operating characteristics,  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$**

PARAMETER	TYP	UNIT
$C_{pd}^\ddagger$ Power dissipation capacitance	54	pF

‡  $C_{pd}$  is used to determine the dynamic power consumption, per package.

$$P_D = C_{pd} V_{CC}^2 f_i + \sum C_L V_{CC}^2 f_o$$

where:  $f_i$  = input frequency

$f_o$  = output frequency

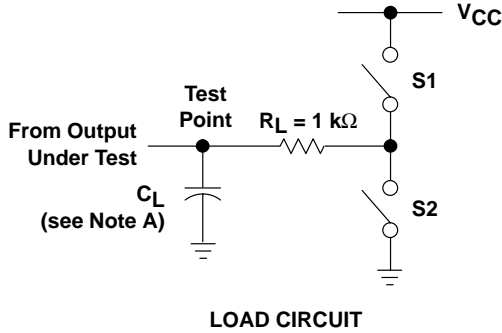
$C_L$  = output load capacitance

$V_{CC}$  = supply voltage

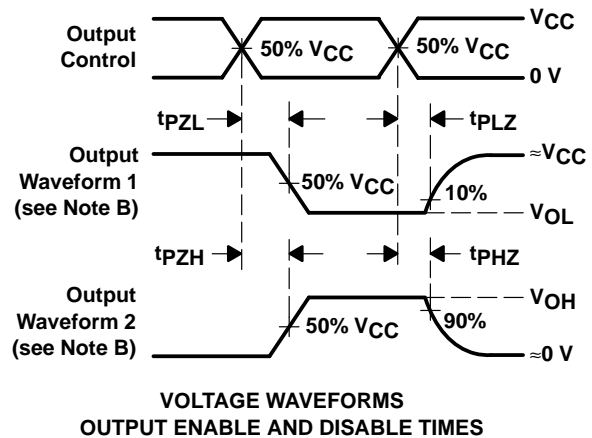
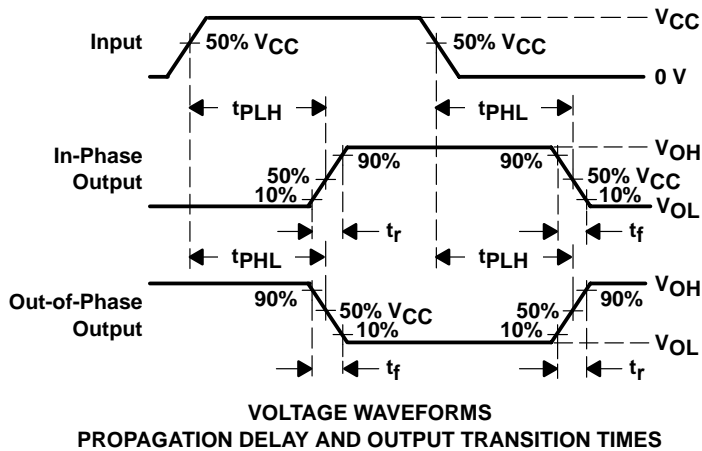
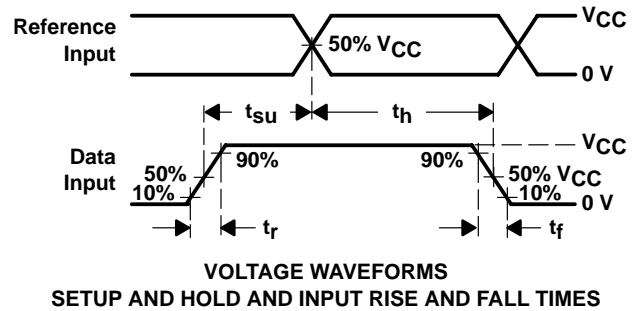
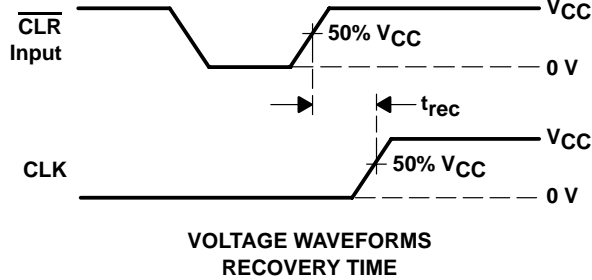
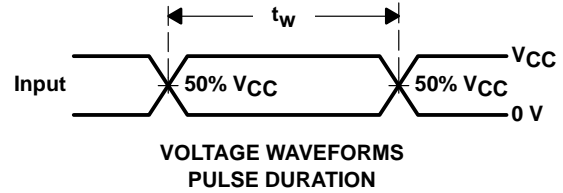
# CD74HCT4543 BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER

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## PARAMETER MEASUREMENT INFORMATION



PARAMETER	S1	S2	
$t_{en}$	$t_{PZH}$	Open	Closed
	$t_{PZL}$	Closed	Open
$t_{dis}$	$t_{PHZ}$	Open	Closed
	$t_{PLZ}$	Closed	Open
$t_{pd}$ or $t_t$	Open	Open	



- NOTES:
- $C_L$  includes probe and test-fixture capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - For clock inputs,  $f_{max}$  is measured with the input duty cycle at 50%.
  - The outputs are measured one at a time with one input transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION CIRCUITS

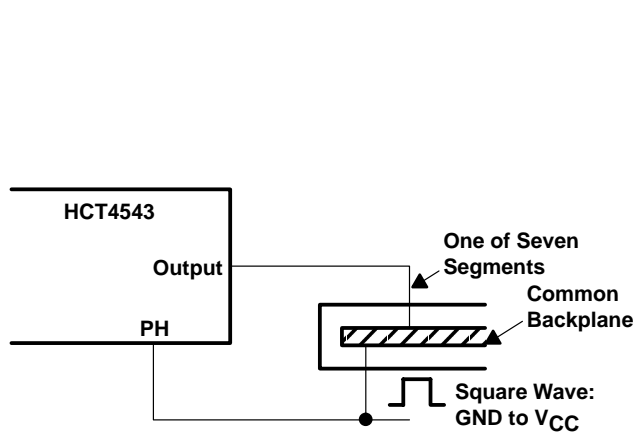


Figure 2. Connection to Liquid-Crystal Display (LCD)

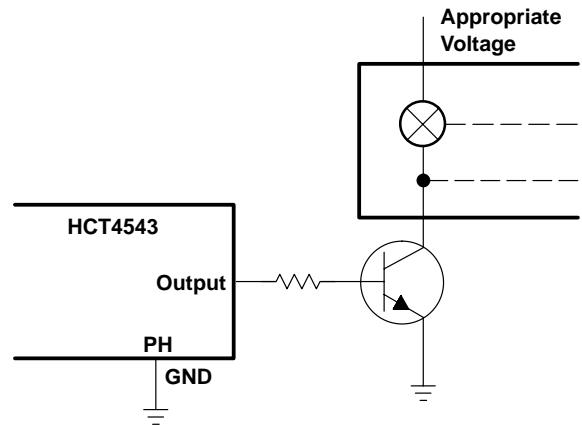


Figure 3. Connection to Incandescent Display

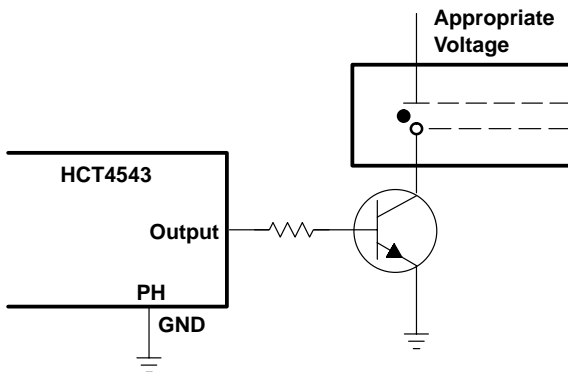


Figure 4. Connection to Gas-Discharge Display

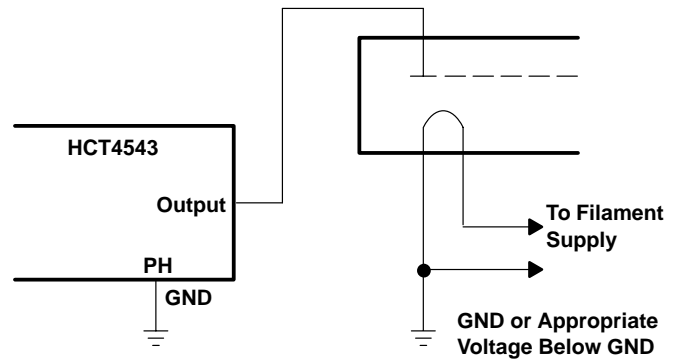


Figure 5. Connection to Fluorescent Display

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD74HCT4543E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT4543EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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