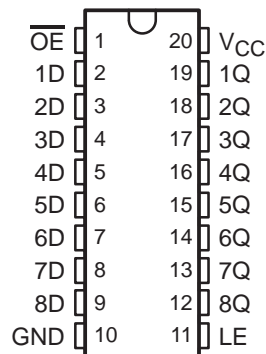


# CD54HCT573, CD74HCT573 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS455C – FEBRUARY 2001 – REVISED MAY 2004

- 4.5-V to 5.5-V  $V_{CC}$  Operation
- Wide Operating Temperature Range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Balanced Propagation Delays and Transition Times
- Standard Outputs Drive Up To 10 LS-TTL Loads
- Significant Power Reduction Compared to LS-TTL Logic ICs
- Inputs Are TTL-Voltage Compatible

CD54HCT573 . . . F PACKAGE  
CD74HCT573 . . . DB, E, OR M PACKAGE  
(TOP VIEW)



## description/ordering information

The 'HCT573 devices are octal transparent D-type latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ( $\overline{\text{OE}}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{\text{OE}}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

| $T_A$  | PACKAGE†  |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|--|-----------|---------------|-----------------------|------------------|
| $-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$ | PDIP – E  | Tube          | CD74HCT573E           | CD74HCT573E      |
|  | SSOP – DB | Tape and reel | CD74HCT573DBR         | HK573            |
|  | SOIC – M  | Tube          | CD74HCT573M           | HCT573M          |
|  |           | Tape and reel | CD74HCT573M96         |                  |
|  | CDIP – F  | Tube          | CD54HCT573F3A         | CD54HCT573F3A    |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

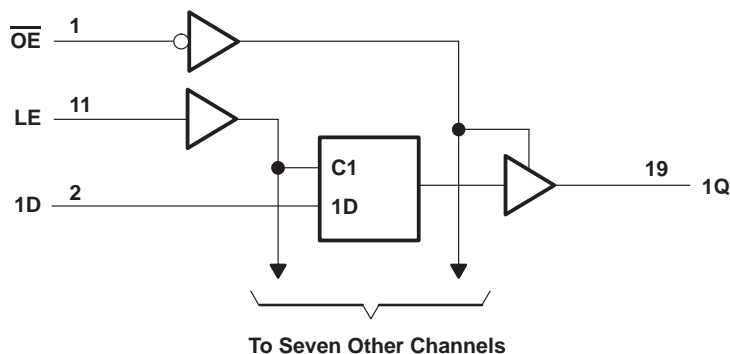
# CD54HCT573, CD74HCT573 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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FUNCTION TABLE  
(each latch)

| INPUTS          |    |   | OUTPUT |
|-----------------|----|---|--------|
| $\overline{OE}$ | LE | D | Q      |
| L               | H  | H | H      |
| L               | H  | L | L      |
| L               | L  | X | $Q_0$  |
| H               | X  | X | Z      |

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|  |                |
|--|----------------|
| Supply voltage range, $V_{CC}$   | -0.5 V to 7 V  |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)           | $\pm 20$ mA    |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)          | $\pm 20$ mA    |
| Continuous output drain current per output, $I_O$ ( $V_O = 0$ to $V_{CC}$ )          | $\pm 35$ mA    |
| Continuous output source or sink current per output, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) | $\pm 25$ mA    |
| Continuous current through $V_{CC}$ or GND   | $\pm 50$ mA    |
| Package thermal impedance, $\theta_{JA}$ (see Note 2):                               |                |
| DB package   | 70°C/W         |
| E package  | 69°C/W         |
| M package  | 58°C/W         |
| Storage temperature range, $T_{stg}$   | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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## recommended operating conditions (see Note 3)

|  | T <sub>A</sub> = 25°C |                 | T <sub>A</sub> = -55°C TO 125°C |                 | T <sub>A</sub> = -40°C TO 85°C |                 | UNIT |
|--|-----------------------|-----------------|---------------------------------|-----------------|--------------------------------|-----------------|------|
|  | MIN                   | MAX             | MIN                             | MAX             | MIN                            | MAX             |      |
| V <sub>CC</sub> Supply voltage           | 4.5                   | 5.5             | 4.5                             | 5.5             | 4.5                            | 5.5             | V    |
| V <sub>IH</sub> High-level input voltage | 2                     |                 | 2                               |                 | 2                              |                 | V    |
| V <sub>IL</sub> Low-level input voltage  |                       | 0.8             |                                 | 0.8             |                                | 0.8             | V    |
| V <sub>I</sub> Input voltage             |                       | V <sub>CC</sub> |                                 | V <sub>CC</sub> |                                | V <sub>CC</sub> | V    |
| V <sub>O</sub> Output voltage            |                       | V <sub>CC</sub> |                                 | V <sub>CC</sub> |                                | V <sub>CC</sub> | V    |
| Δt/Δv Input transition rise or fall rate |                       | 500             |                                 | 500             |                                | 500             | ns   |

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                     | TEST CONDITIONS  |                          | V <sub>CC</sub> | T <sub>A</sub> = 25°C |      | T <sub>A</sub> = -55°C TO 125°C |     | T <sub>A</sub> = -40°C TO 85°C |      | UNIT |
|-------------------------------|--|--------------------------|-----------------|-----------------------|------|---------------------------------|-----|--------------------------------|------|------|
|                               |  |                          |                 | MIN                   | MAX  | MIN                             | MAX | MIN                            | MAX  |      |
| V <sub>OH</sub>               | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>                        | I <sub>OH</sub> = -20 μA | 4.5 V           | 4.4                   |      | 4.4                             |     | 4.4                            |      | V    |
|                               |  | I <sub>OH</sub> = -6 mA  |                 | 3.98                  |      | 3.7                             |     | 3.84                           |      |      |
| V <sub>OL</sub>               | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>                        | I <sub>OL</sub> = 20 μA  | 4.5 V           |                       | 0.1  |                                 | 0.1 |                                | 0.1  | V    |
|                               |  | I <sub>OL</sub> = 6 mA   |                 |                       | 0.26 |                                 | 0.4 |                                | 0.33 |      |
| I <sub>I</sub>                | V <sub>I</sub> = V <sub>CC</sub> or 0                                      |                          | 5.5 V           |                       | ±0.1 |                                 | ±1  |                                | ±1   | μA   |
| I <sub>OZ</sub>               | V <sub>O</sub> = V <sub>CC</sub> or 0                                      |                          | 5.5 V           |                       | ±0.5 |                                 | ±10 |                                | ±5   | μA   |
| I <sub>CC</sub>               | V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0                  |                          | 5.5 V           |                       | 8    |                                 | 160 |                                | 80   | μA   |
| ΔI <sub>CC</sub> <sup>†</sup> | One input at V <sub>CC</sub> - 2.1 V, Other inputs at 0 or V <sub>CC</sub> |                          | 4.5 V to 5.5 V  |                       | 360  |                                 | 490 |                                | 450  | μA   |
| C <sub>i</sub>                |  |                          |                 |                       | 10   |                                 | 10  |                                | 10   | pF   |
| C <sub>o</sub>                |  |                          |                 |                       | 20   |                                 | 20  |                                | 20   | pF   |

<sup>†</sup> Additional quiescent supply current per input pin, TTL inputs high, 1 unit load. For dual-supply systems, theoretical worst-case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

### HCT INPUT LOADING TABLE

| INPUT                  | UNIT LOAD |
|------------------------|-----------|
| $\overline{\text{OE}}$ | 1.25      |
| Any D                  | 0.3       |
| LE                     | 0.65      |

Unit load is ΔI<sub>CC</sub> limit specified in electrical characteristics table (e.g., 360 μA max at 25°C).

**CD54HCT573, CD74HCT573**  
**OCTAL TRANSPARENT D-TYPE LATCHES**  
**WITH 3-STATE OUTPUTS**

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timing requirements over recommended operating free-air temperature range,  $V_{CC} = 4.5\text{ V}$  (unless otherwise noted) (see Figure 1)

|                                      | $T_A = 25^\circ\text{C}$ |     | $T_A = -55^\circ\text{C}$<br>TO $125^\circ\text{C}$ |     | $T_A = -40^\circ\text{C}$<br>TO $85^\circ\text{C}$ |     | UNIT |
|--------------------------------------|--------------------------|-----|---|-----|--|-----|------|
|                                      | MIN                      | MAX | MIN   | MAX | MIN  | MAX |      |
| $t_w$ Pulse duration, LE high        | 16                       |     | 24  |     | 20   |     | ns   |
| $t_{su}$ Setup time, data before LE↓ | 13                       |     | 20  |     | 16   |     | ns   |
| $t_h$ Hold time, data after LE↓      | 10                       |     | 15  |     | 13   |     | ns   |

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 4.5\text{ V}$  (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE  | $T_A = 25^\circ\text{C}$ |     | $T_A = -55^\circ\text{C}$<br>TO $125^\circ\text{C}$ |     | $T_A = -40^\circ\text{C}$<br>TO $85^\circ\text{C}$ |     | UNIT |
|-----------|-----------------|----------------|----------------------|--------------------------|-----|---|-----|--|-----|------|
|           |                 |                |                      | MIN                      | MAX | MIN   | MAX | MIN  | MAX |      |
| $t_{pd}$  | D               | Q              | $C_L = 50\text{ pF}$ | 35                       |     | 53  |     | 44   |     | ns   |
|           | LE              |                |                      | 35                       |     | 53  |     | 44   |     |      |
| $t_{en}$  | $\overline{OE}$ | Q              | $C_L = 50\text{ pF}$ | 35                       |     | 53  |     | 44   |     | ns   |
| $t_{dis}$ | $\overline{OE}$ | Q              | $C_L = 50\text{ pF}$ | 35                       |     | 53  |     | 44   |     | ns   |
| $t_t$     |                 | Q              | $C_L = 50\text{ pF}$ | 12                       |     | 18  |     | 15   |     | ns   |

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

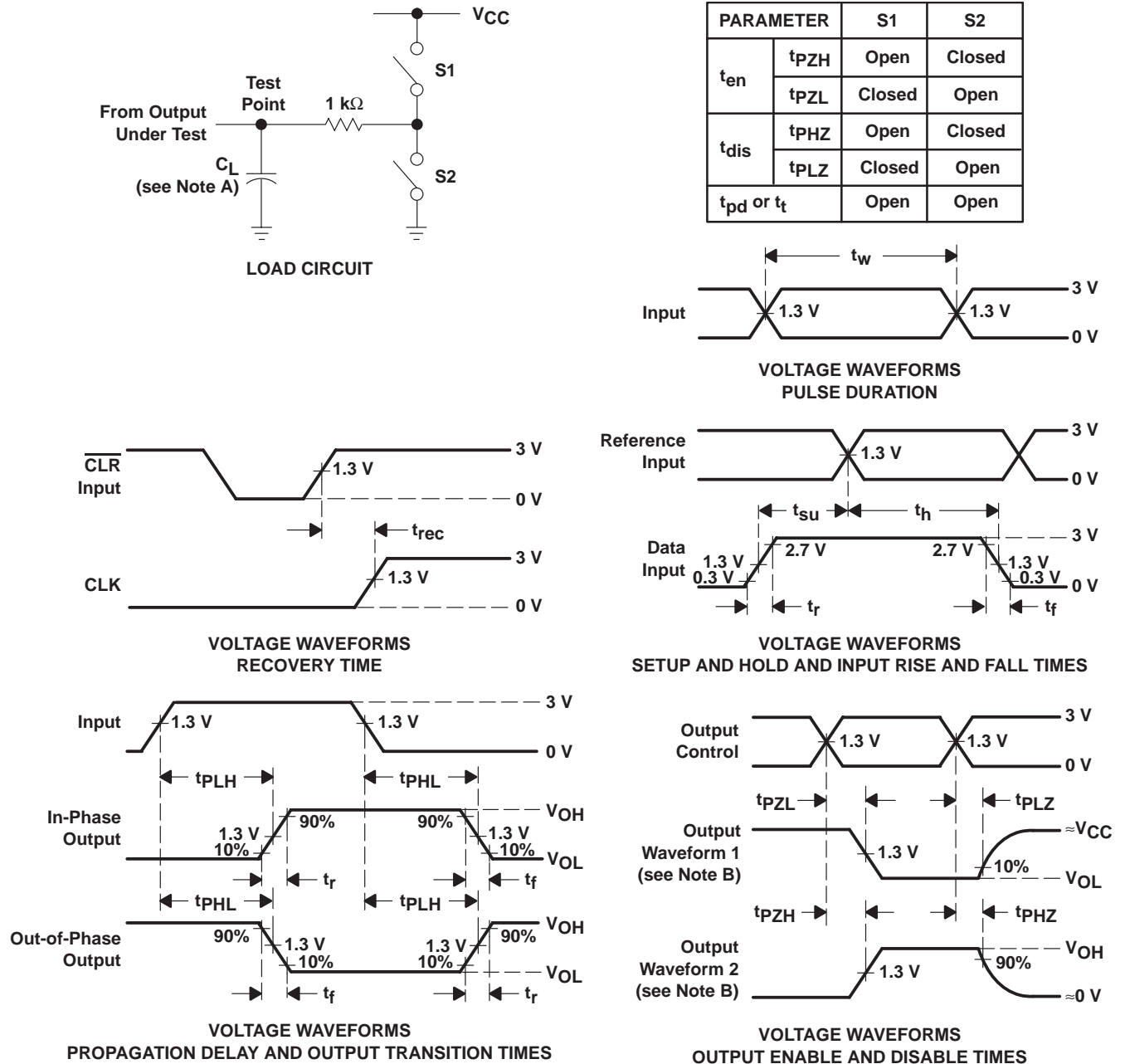
| PARAMETER                              | TYP | UNIT |
|--|-----|------|
| $C_{pd}$ Power dissipation capacitance | 53  | pF   |



# CD54HCT573, CD74HCT573 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- $C_L$  includes probe and test-fixture capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - For clock inputs,  $f_{max}$  is measured with the input duty cycle at 50%.
  - The outputs are measured one at a time, with one input transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-8685601RA   | ACTIVE                | CDIP         | J               | 20   | 1           | TBD                     | A42 SNPB         | N / A for Pkg Type           |
| CD54HCT573F      | ACTIVE                | CDIP         | J               | 20   | 1           | TBD                     | A42 SNPB         | N / A for Pkg Type           |
| CD54HCT573F3A    | ACTIVE                | CDIP         | J               | 20   | 1           | TBD                     | A42 SNPB         | N / A for Pkg Type           |
| CD74HCT573DBR    | ACTIVE                | SSOP         | DB              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT573DBRE4  | ACTIVE                | SSOP         | DB              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT573DBRG4  | ACTIVE                | SSOP         | DB              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT573E      | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| CD74HCT573EE4    | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| CD74HCT573M      | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT573M96    | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT573M96E4  | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT573M96G4  | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT573MG4    | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HCT573DBR | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| CD74HCT573M96 | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.0    | 2.7     | 12.0    | 24.0   | Q1            |



**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HCT573DBR | SSOP         | DB              | 20   | 2000 | 346.0       | 346.0      | 33.0        |
| CD74HCT573M96 | SOIC         | DW              | 20   | 2000 | 346.0       | 346.0      | 41.0        |

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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| DSP                         | <a href="http://dsp.ti.com">dsp.ti.com</a>                         |
| Clocks and Timers           | <a href="http://www.ti.com/clocks">www.ti.com/clocks</a>           |
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