A DIVISION OF CIRRUS LOGIC

CS4226

Surround Sound Codec

Features

- Stereo 20-bit A/D Converters
- Six 20-bit D/A Converters
- S/PDIF Receiver
  - — AC-3 & MPEG Auto-detect Capability
- 108 dB DAC Signal-to-Noise Ratio (EIAJ)
- Mono 20-bit A/D Converter
- Programmable Input Gain & Output Attenuation
- On-chip Anti-aliasing and Output Smoothing Filters
- De-emphasis for 32 kHz, 44.1 kHz, 48 kHz

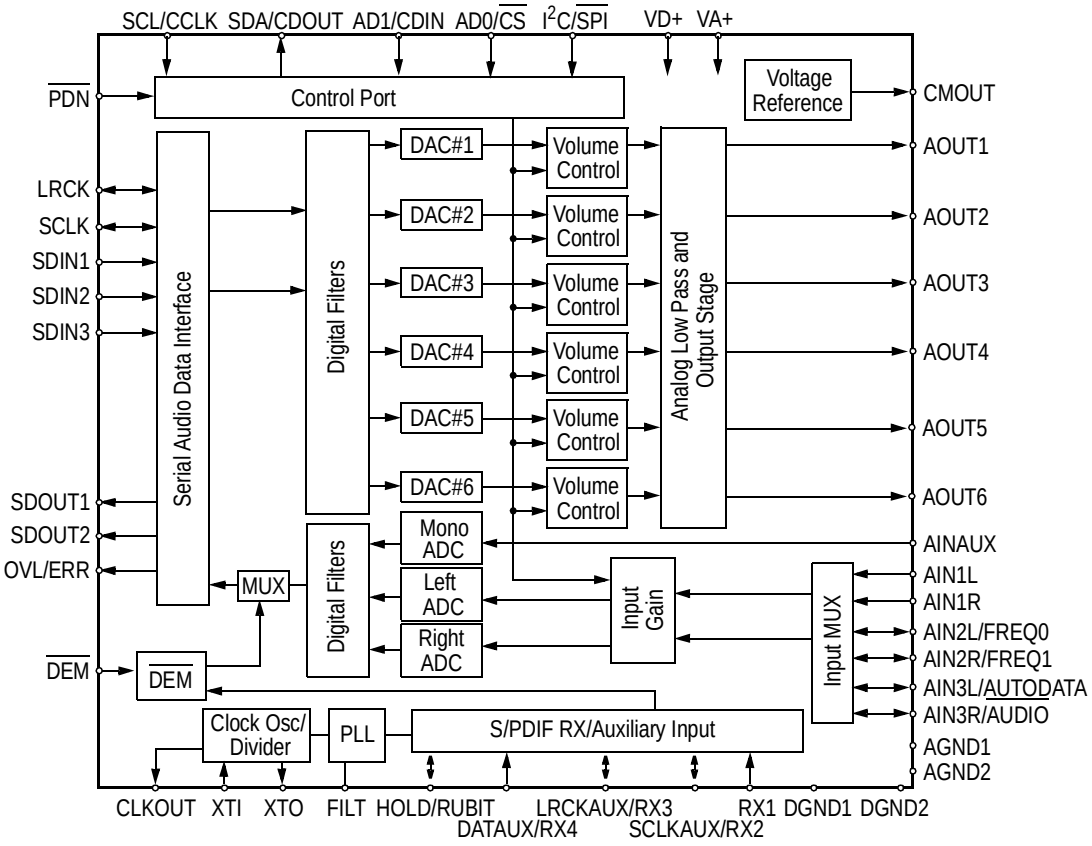
Description

The CS4226 is a single-chip codec providing stereo analog-to-digital and six digital-to-analog converters using delta-sigma conversion techniques. This +5 V device also contains volume control independently selectable for each of the six D/A channels. An S/PDIF receiver is included as a digital input channel. Applications include Dolby Pro-logic, THX, DTS and Dolby Digital AC-3 home theater systems, DSP based car audio systems, and other multi-channel applications.

The CS4226 is packaged in a 44-pin plastic TQFP.

ORDERING INFORMATION

CS4226-KQ	-10° to +70° C	44-pin TQFP
CS4226-BQ	-40° to +85° C	44-pin TQFP
CDB4226		Evaluation Board



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CHARACTERISTICS/SPECIFICATIONS

ANALOG CHARACTERISTICS (T_A = 25°C; VA+, VD+ = +5V; Full Scale Input Sine wave, 990.52 Hz; Fs = 44.1 kHz (PLL in use); Measurement Bandwidth is 20 Hz to 20 kHz; Local components as shown in Figure 1; SPI mode, Format 3, unless otherwise specified.)

Parameter	Symbol	CS4226-KQ			CS4226-BQ			Units
		Min	Typ	Max	Min	Typ	Max	
Analog Input Characteristics - Minimum gain setting (0 dB) Differential Input; unless otherwise specified.								
ADC Resolution Stereo Audio channels		16	-	20	16	-	20	Bits
Mono channel		16	-	20	16	-	20	Bits
Total Harmonic Distortion	THD		0.003	-		0.003	-	%
Dynamic Range (A weighted, Stereo)		92	95	-	90	93	-	dB
(unweighted, Stereo)		-	92	-	-	90	-	dB
(A weighted, Mono)		89	-	-	87	-	-	dB
Total Harmonic -1 dB, Stereo (Note 1)	THD+N	-	-88	-82	-	-86	-80	dB
Distortion + Noise -1 dB, Mono (Note 1)		-	-	-72	-	-	-70	dB
Interchannel Isolation		-	90	-	-	90	-	dB
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Programmable Input Gain Span		8	9	10	8	9	10	dB
Gain Step Size		2.7	3	3.3	2.7	3	3.3	dB
Offset Error (with high pass filter)		-	-	0	-	-	0	LSB
Full Scale Input Voltage (Single Ended):		0.90	1.0	1.10	0.90	1.0	1.10	Vrms
Gain Drift		-	100	-	-	100	-	ppm/°C
Input Resistance (Note 2)		10	-	-	10	-	-	kΩ
Input Capacitance		-	-	15	-	-	15	pF
CMOUT Output Voltage		-	2.3	-	-	2.3	-	V
A/D Decimation Filter Characteristics								
Passband (Note 3)		0.02	-	20.0	0.02	-	20.0	kHz
Passband Ripple		-	-	0.01	-	-	0.01	dB
Stopband (Note 3)		27.56	-	5617.2	27.56	-	5617.2	kHz
Stopband Attenuation (Note 4)		80	-	-	80	-	-	dB
Group Delay (Fs = Output Sample Rate) (Note 5)	t_{gd}	-	15/Fs	-	-	15/Fs	-	s
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0	-	-	0	µs

Notes:
1. Referenced to typical full-scale differential input voltage (2Vrms).
2. Input resistance is for the input selected. Non-selected inputs have a very high (>1MΩ) input resistance. The input resistance will vary with gain value selected, but will always be greater than the min. value specified
3. Filter characteristics scale with output sample rate.
4. The analog modulator samples the input at 5.6448 MHz for an output sample rate of 44.1 kHz. There is no rejection of input signals which are multiples of the sampling frequency (n × 5.6448 MHz ±20.0 kHz where n = 0,1,2,3...).
5. Group delay for Fs = 44.1 kHz, t_{gd} = 15/44.1 kHz = 340 µs

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	CS4226-KQ			CS4226-BQ			Units
		Min	Typ	Max	Min	Typ	Max	
High Pass Filter Characteristics								
Frequency Response: -3 dB (Note 3)		-	3.4	-	-	3.4	-	Hz
-0.13 dB		-	20	-	-	20	-	Hz
Phase Deviation @ 20 Hz (Note 3)		-	10	-	-	10	-	Deg.
Passband Ripple		-	-	0	-	-	0	dB
Analog Output Characteristics - Minimum Attenuation, 10 k, 100 pF load; unless otherwise specified.								
DAC Resolution		16	-	20	16	-	20	Bits
Signal-to-Noise/Idle (DAC muted, A weighted) Channel Noise		101	108	-	99	106	-	dB
Dynamic Range (DAC not muted, A weighted)		93	98	-	91	96	-	dB
(DAC not muted, unweighted)		-	95	-	-	93	-	dB
Total Harmonic Distortion	THD	-	0.003	-	-	0.003	-	%
Total Harmonic Distortion + Noise (Stereo)	THD+N	-	-88	-83	-	-86	-81	dB
Interchannel Isolation		-	90	-	-	90	-	dB
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Attenuation Step Size (All Outputs)		0.7	1	1.3	0.7	1	1.3	dB
Programmable Output Attenuation Span		-84	-86	-	-84	-86	-	dB
Offset Voltage (relative to CMOUT)		-	±15	-	-	±15	-	mV
Full Scale Output Voltage		0.92	1.0	1.08	0.92	1.0	1.08	Vrms
Gain Drift		-	100	-	-	100	-	ppm/°C
Out-of-Band Energy (Fs/2 to 2Fs)		-	-60	-	-	-60	-	dBFs
Analog Output Load Resistance:		10	-	-	10	-	-	kΩ
Capacitance:		-	-	100	-	-	100	pF
Combined Digital and Analog Filter Characteristics								
Frequency Response 10 Hz to 20 kHz		-	±0.1	-	-	±0.1	-	dB
Deviation from Linear Phase		-	±0.5	-	-	±0.5	-	Deg.
Passband: to 0.01 dB corner (Notes 6, 7)		0	-	20.0	0	-	20.0	kHz
Passband Ripple (Note 7)		-	-	±0.01	-	-	±0.01	dB
Stopband (Notes 6 ,7)		24.1	-	-	24.1	-	-	kHz
Stopband Attenuation (Note 8)		70	-	-	70	-	-	dB
Group Delay (Fs = Input Word Rate) (Note 5)	tgd	-	16/Fs	-	-	16/Fs	-	s
Analog Loopback Performance								
Signal-to-noise Ratio (CCIR-2K weighted, -20 dB input)	CCIR-2K	-	71	-	-	71	-	dB
Power Supply								
Power Supply Current Operating		-	90	113	-	90	115	mA
Power Down		-	1	3	-	1	3	mA
Power Supply Rejection (1 kHz, 10 mV_{rms})		-	45	-	-	45	-	dB

Notes: 6. The passband and stopband edges scale with frequency. For input word rates, Fs, other than 44.1 kHz, the 0.01 dB passband edge is 0.4535×Fs and the stopband edge is 0.5465×Fs.

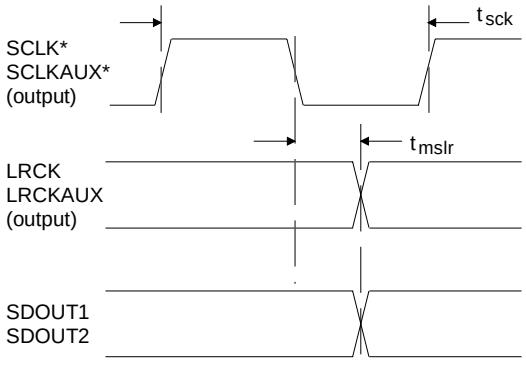
7. Digital filter characteristics.

8. Measurement bandwidth is 10 Hz to 3 Fs.

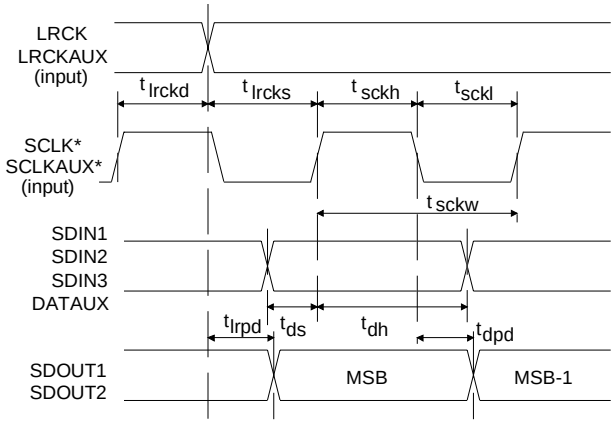
SWITCHING CHARACTERISTICS (T_A = 25°C; VA+, VD+ = +5V ±5%, outputs loaded with 30 pF)

Parameter		Symbol	Min	Typ	Max	Units
Audio ADC's & DAC's Sample Rate		Fs	4	-	50	kHz
XTI Frequency	(XTI = 256, 384, or 512 Fs)		1.024	-	26	MHz
XTI Pulse Width High	XTI = 512 Fs		10	-	-	ns
	XTI = 384 Fs		21	-	-	ns
	XTI = 256 Fs		31	-	-	ns
XTI Pulse Width Low	XTI = 512 Fs		10	-	-	ns
	XTI = 384 Fs		21	-	-	ns
	XTI = 256 Fs		31	-	-	ns
PLL Clock Recovery Frequency	RX, XTI, LRCK, LRCKAUX		30	-	50	kHz
XTI Jitter Tolerance			-	500	-	ps
$\overline{\text{PDN}}$ Low Time	(Note 9)		500	-	-	ns
SCLK Falling Edge to SDOUT Output Valid	(DSCK = 0)	t_{dpd}	-	-	$\frac{1}{(384)Fs} + 20$	ns
LRCK edge to MSB valid		t_{lrpd}	-	-	40	ns
SDIN Setup Time Before SCLK Rising Edge	(DSCK=0)	t_{ds}	-	-	25	ns
SDIN Hold Time After SCLK Rising Edge	(DSCK=0)	t_{dh}	-	-	25	ns
Master Mode						
SCLK Period		t_{sck}	$\frac{1}{(256)Fs}$	-	-	ns
SCLK Falling to LRCK Edge	(DSCK=0)	t_{mslr}	-	±10	-	ns
SCLK Duty Cycle			-	50	-	%
Slave Mode						
SCLK Period		t_{sckw}	$\frac{1}{(128)Fs}$	-	-	ns
SCLK High Time		t_{sckh}	40	-	-	ns
SCLK Low Time		t_{sckl}	40	-	-	ns
SCLK Rising to LRCK Edge	(DSCK=0)	t_{lrckd}	20	-	-	ns
LRCK Edge to SCLK Rising	(DSCK=0)	t_{lrcks}	40	-	-	ns

Notes: 9. After powering up the CS4226, $\overline{\text{PDN}}$ should be held low until the power supply is settled.



Audio Ports Master Mode Timing



*SCLK, SCLKAUX shown for DSCK = 0 and ASCK = 0.
SCLK & SCLKAUX inverted for DSCK = 1 and ASCK = 1, respectively.

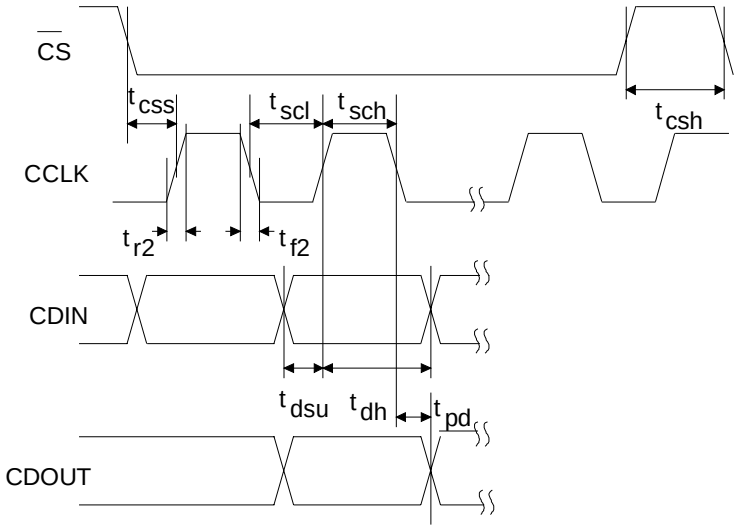
Audio Ports Slave Mode and Data I/O timing

SWITCHING CHARACTERISTICS - CONTROL PORT (TA = 25°C VD+, VA+ = 5V ±5%; Inputs: logic 0 = DGND, logic 1 = VD+, C_L = 30 pF)

Parameter		Symbol	Min	Max	Units
SPI Mode (SPI/I^2C = 0)					
CCLK Clock Frequency		f_{sck}	-	6	MHz
CS High Time Between Transmissions		t_{csh}	1.0		µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20		ns
CCLK Low Time		t_{scl}	66		ns
CCLK High Time		t_{sch}	66		ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40		ns
CCLK Rising to DATA Hold Time	(Note 10)	t_{dh}	15		ns
CCLK Falling to CDOUT stable		t_{pd}		45	ns
Rise Time of CDOUT		t_{r1}		25	ns
Fall Time of CDOUT		t_{f1}		25	ns
Rise Time of CCLK and CDIN	(Note 11)	t_{r2}		100	ns
Fall Time of CCLK and CDIN	(Note 11)	t_{f2}		100	ns

Notes: 10. Data must be held for sufficient time to bridge the transition time of CCLK.

11. For F_{SCK} < 1 MHz

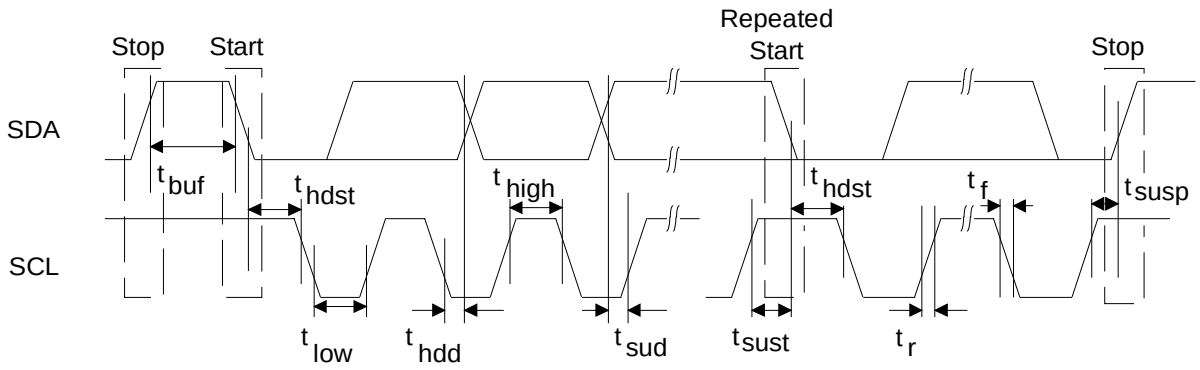


SWITCHING CHARACTERISTICS - CONTROL PORT (T_A = 25°C; VD+, VA+ = 5V ±5%; Inputs: logic 0 = DGND, logic 1 = VD+, C_L = 30 pF)

Parameter	Symbol	Min	Max	Units
I²C® Mode (SPI/I²C = 1) (Note 12)				
SCL Clock Frequency	f_{scl}	-	100	kHz
Bus Free Time Between Transmissions	t_{buf}	4.7		µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0		µs
Clock Low Time	t_{low}	4.7		µs
Clock High Time	t_{high}	4.0		µs
Setup Time for Repeated Start Condition	t_{sust}	4.7		µs
SDA Hold Time from SCL Falling (Note 13)	t_{hdd}	0		µs
SDA Setup Time to SCL Rising	t_{sud}	250		ns
Rise Time of Both SDA and SCL Lines	t_r		1	µs
Fall Time of Both SDA and SCL Lines	t_f		300	ns
Setup Time for Stop Condition	t_{susp}	4.7		µs

Notes: 12. I²C is a registered trademark of Philips Semiconductors.

13. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.



S/PDIF RECEIVER CHARACTERISTICS (RX1, RX2, RX3, RX4 pins only; VD+, VA+ = 5V ±5%)

Parameter	Symbol	Min	Typ	Max	Units
Input Resistance	Z_N	-	10	-	kΩ
Input Voltage	V_{TH}	200	-	-	mVpp
Input Hysteresis	V_{HYST}	-	50	-	mV
Input Sample Frequency	F_S	30	-	50	kHz
CLKOUT Jitter (Note 14)		-	200	-	ps RMS
CLKOUT Duty Cycle (high time/cycle time) (Note 15)		40	50	60	%

Notes: 14. CLKOUT Jitter is for 256×FS selected as output frequency measured from falling edge to falling edge. Jitter is greater for 384×Fs and 512×Fs as selected output frequency.

15. For CLKOUT frequency equal to 1×Fs, 384×Fs, and 512×Fs. See Master Clock Output section.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies	Digital	VD+	-0.3	-	6.0	V
	Analog	VA+	-0.3	-	6.0	V
Input Current	(Note 16)		-	-	±10	mA
Analog Input Voltage	(Note 17)		-0.7	-	(VA+)+0.7	V
Digital Input Voltage	(Note 17)		-0.7	-	(VD+)+0.7	V
Ambient Temperature	(Power Applied)		-55	-	+125	°C
Storage Temperature			-65	-	+150	°C

Notes: 16. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

17. The maximum over or under voltage is limited by the input current.

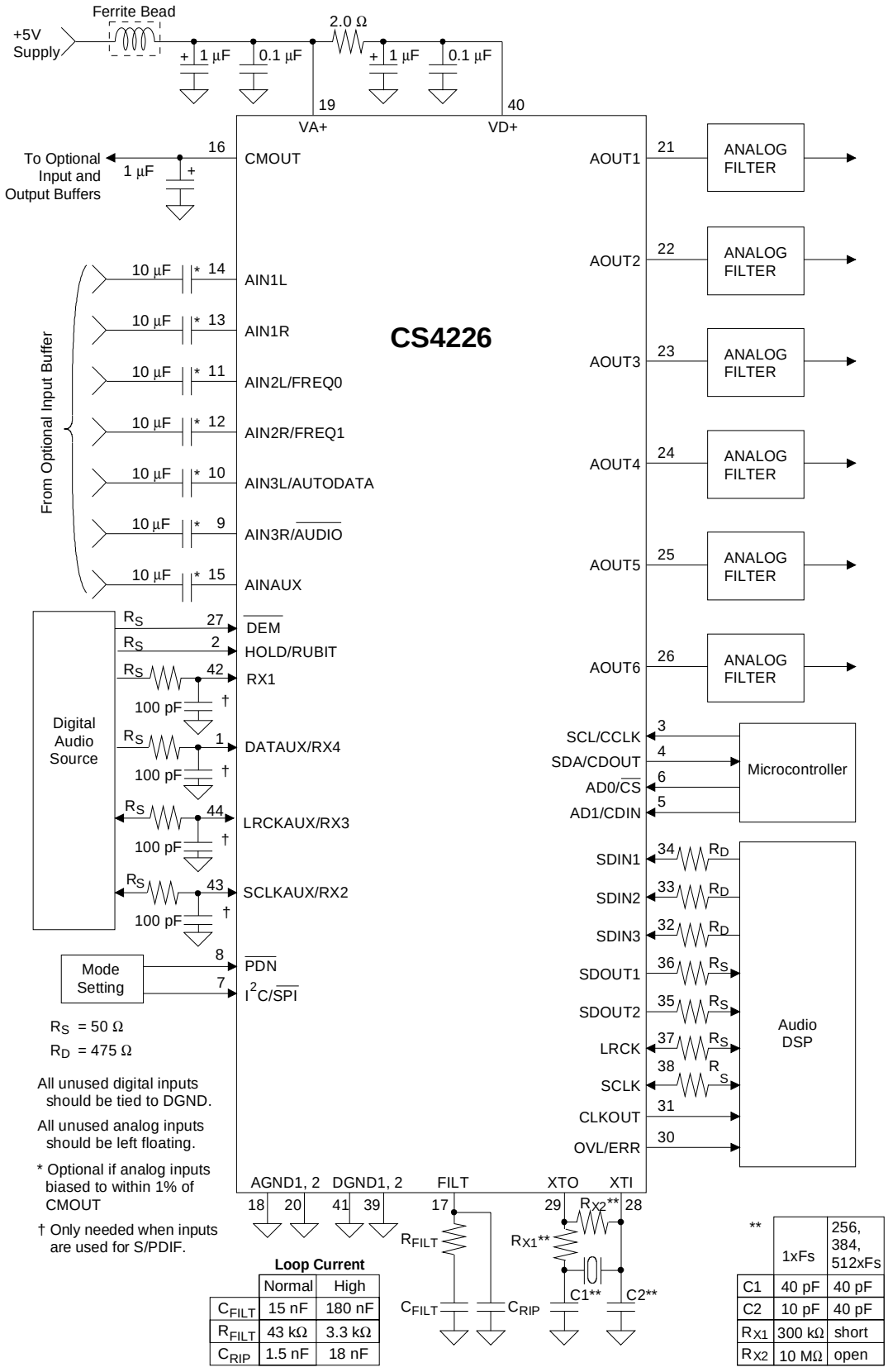
Warning: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies	Digital	VD+	4.75	5.0	5.25	V
|(VA+)-(VD+)|<0.4 V	Analog	VA+	4.75	5.0	5.25	V
Operating Ambient Temperature	CS4226-KQ	T_A	-10	25	70	°C
	CS4226-BQ		-40	25	85	°C

DIGITAL CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5 V ±5%)

Parameter		Symbol	Min	Typ	Max	Units
High-level Input Voltage	(except RX1)	V_{IH}	2.8	-	(VD+)+0.3	V
Low-level Input Voltage	(except RX1)	V_{IL}	-0.3	-	0.8	V
High-level Output Voltage at I_0 = -2.0 mA		V_{OH}	(VD+)-1.0	-	-	V
Low-level Output Voltage at I_0 = 2.0 mA		V_{OL}	-	-	0.4	V
Input Leakage Current	(Digital Inputs)		-	-	10	µA
Output Leakage Current	(High-Impedance Digital Outputs)		-	-	10	µA



Loop Current

	Normal	High
C_{FILT}	15 nF	180 nF
R_{FILT}	43 kΩ	3.3 kΩ
C_{RIP}	1.5 nF	18 nF

**

	1xFs	256, 384, 512xFs
C1	40 pF	40 pF
C2	10 pF	40 pF
R_{X1}	300 kΩ	short
R_{X2}	10 MΩ	open

Figure 1. Recommended Connection Diagram

FUNCTIONAL DESCRIPTION

Overview

The CS4226 has 2 channels of 20-bit analog-to-digital conversion and 6 channels of 20-bit digital-to-analog conversion. A mono 20-bit ADC is also provided. All ADCs and DACs are delta-sigma converters. The stereo ADC inputs have adjustable input gain, while the DAC outputs have adjustable output attenuation. The device also contains an S/PDIF receiver capable of receiving compressed AC-3/MPEG or uncompressed digital audio data.

Digital audio data for the DACs and from the ADCs is communicated over separate serial ports. This allows concurrent writing to and reading from the device. The CS4226 functions are controlled via a serial microcontroller interface. Figure 1 shows the recommended connection diagram for the CS4226.

Analog Inputs

Line Level Inputs

AIN1R, AIN1L, AIN2R, AIN2L, AIN3R, AIN3L and AINAUX are the line level input pins (See Figure 1). These pins are internally biased to the CMOUT voltage. A 10 µF DC blocking capacitor placed in series with the input pins allows signals centered around 0 V to be input to the CS4226. Figure 2 shows an optional dual op amp buffer which combines level shifting with a gain of 0.5 to attenuate the standard line level of 2 Vrms to 1 Vrms. The CMOUT reference level is used to bias the op-amps to approximately one half the supply voltage. With this input circuit, the 10 µF DC blocking caps in Figure 1 may be omitted. Any remaining DC offset will be removed by the internal high-pass filters.

Selection of stereo the input pair (AIN1L/R, AIN2L/R or AIN3L/R) for the 20-bit ADC's is accomplished by setting the AIS1/0 bits (ADC analog input mux control), which are accessible in the

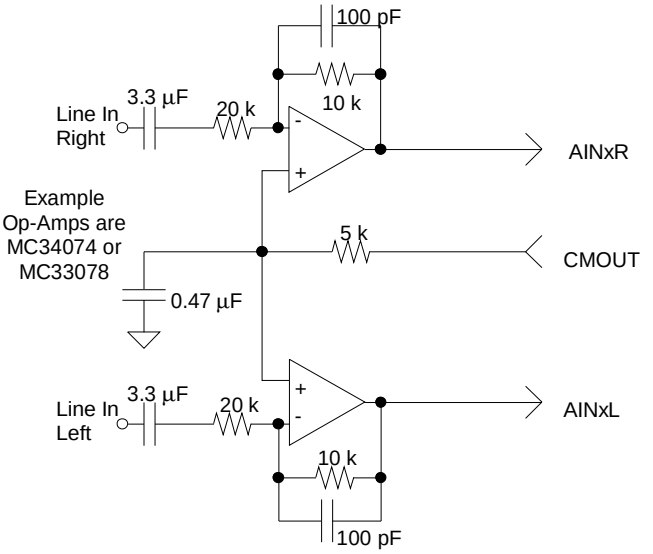


Figure 2. Optional Line Input Buffer

ADC Control Byte. On-chip anti-aliasing filters follow the input mux providing anti-aliasing for all input channels.

The analog inputs may also be configured as differential inputs. This is enabled by setting bits AIS1/0=3. In the differential configuration, the left channel inputs reside on pins 10 and 11, and the right channel inputs reside on pins 12 and 13 as described in Table 1 below. In differential mode, the full scale input level is 2 Vrms.

Single-ended	Pin #	Differential Inputs
AIN3L	Pin 10	AINL+
AIN3R	Pin 9	unused
AIN2L	Pin 11	AINL-
AIN2R	Pin 12	AINR-
AIN1L	Pin 14	unused
AIN1R	Pin 13	AINR+

Table 1. Single-ended vs Differential Input Pin Assignments

The analog signal is input to the mono ADC via the AINAUX pin.

Independent Muting of both the stereo ADC's and the mono ADC is possible through the ADC Control Byte with the MUTR, MUTL and MUTM bits.

Adjustable Input Gain

The signals from the line inputs are routed to a programmable gain circuit which provides up to 9 dB of gain in 3 dB steps. The gain is adjustable through the Input Control Byte. Right and left channel gain settings are controlled independently with the GNR1/0 and GNL1/0 bits. Level changes occur immediately on register updates. To minimize audible artifacts, level changes should be done with the channel muted.

The ADC Status Report Byte provides feedback of input level for each ADC channel. This register continously monitors the ADC output and records the peak output level since the last register read. Reading this register causes it to reset to 0 and peak monitoring begins again.

High Pass Filter

The operational amplifiers in the input circuitry driving the CS4226 may generate a small DC offset into the A/D converter. The CS4226 includes a high pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multichannel system.

The characteristics of this first-order high pass filter are outlined Table 2 below for an output sample rate of 44.1 kHz. This filter response scales linearly with sample rate.

Frequency Response	-3dB @ 3.4 Hz -0.13 dB @ 20 Hz
Phase Deviation	10 degrees @ 20 Hz
Passband Ripple	None

Table 2. High Pass Filter Characteristics

Analog Outputs

Line Level Outputs

The CS4226 contains an on-chip buffer amplifier producing single-ended outputs capable of driving 10 kΩ loads. Each output (A_{OUT} 1-6) will produce a nominal 2.83 Vpp (1 Vrms) output with a 2.3 volt quiescent voltage for a full scale digital input. The recommended off-chip analog filter is a 2nd order Butterworth with a -3 dB corner at Fs, see Figure 3. This filter provides out-of-band noise attenuation along with a gain of 2, providing a 2 Vrms output signal. A 3rd order Butterworth filter with a -3dB corner at 0.75 Fs can be used if greater out of band noise filtering is desired. The CS4226 DAC interpolation filter is a linear phase design which has been pre-compensated for an external 2nd order Butterworth filter to provide a flat frequency response and linear phase response over the passband. If this filter is not used, small frequency response magnitude and phase errors will occur.

Output Level Attenuator

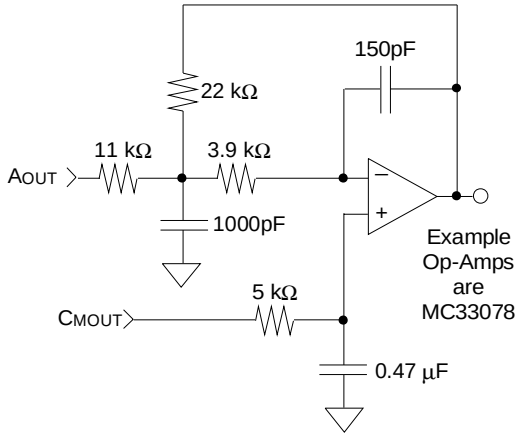
The DAC outputs are each routed through an attenuator which is adjustable in 1 dB steps. Output attenuation is available through the Output Attenuator Data Bytes. Level changes are implemented in the analog domain such that the noise is attenuated by the same amount as the signal , until the residual output noise is equal to the noise floor in the mute state; at this point attenation is implemented in the digital domain. The change from analog to digital attenuation occurs at -23 dB. Level changes only take effect on zero crossings to minimize audible artifacts. If there is no zero crossing, then the requested level change will occur after a time-out period between 512 and 1024 frames (11.6 ms to 23.2 ms at 44.1 kHz frame rate). There is a separate zero crossing detector for each channel. Each ACC bit (Acceptance bit) in the DAC Status Report Byte gives feedback on when a volume control change has taken effect. This bit goes high when a new setting is loaded and returns low when it has taken effect. Volume control changes can be instantaneous by setting the Zero Crossing Disable (ZCD) bit in the DAC Control Byte to 1.

Each output can be independently muted via mute control bits, MUT6-1, in the DAC Control Byte.

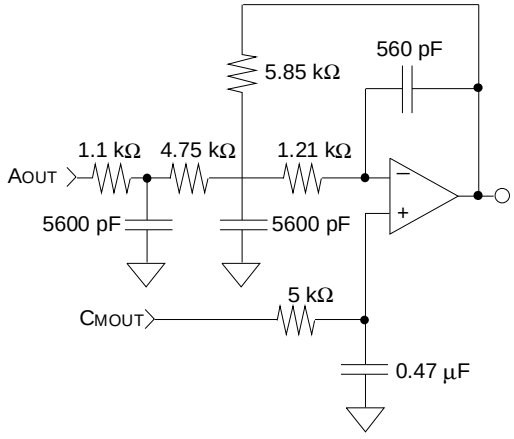
The mute also takes effect on a zero-crossing or after a timeout. In addition, the CS4226 has an optional mute on consecutive zeros feature, where all DAC outputs will mute if they receive between 512 and 1024 consecutive zeros (or -1 code) on all six channels. A single non-zero value will unmute the DAC outputs. This feature can be disabled with the MUTC bit in the DAC Control Byte. When using the internal PLL as the clock source, all DACs will instantly mute when the PLL detects an error.

Clock Generation

The master clock to operate the CS4226 may be generated by using the on-chip inverter and an external crystal, by using the on-chip PLL, or by using an external clock source. In all modes it is required to have SCLK and LRCK synchronous to the selected master clock.



2-Pole Butterworth Filter



3-Pole Butterworth Filter

Figure 3.

Clock Source

The CS4226 requires a high frequency master clock to run the internal logic. The Clock Source bits, CS0/1/2 in Clock Mode Byte, determine the source of the clock. A high frequency crystal can be connected to XTI and XTO, or a high frequency clock can be applied to XTI. In both these cases, the internal PLL is disabled, and the VCO turns off. The externally supplied high frequency clock can be 256 Fs, 384 Fs or 512 Fs; this is set by the CI0/1 bits in the Clock Mode Byte. When using the on-chip crystal oscillator, external loading capacitors are required, see Figure 1. High frequency crystals (>8MHz) should be parallel resonant, fundamental mode and designed for 20 pF loading (equivalent to 40 pF to ground on each leg).

Alternatively, the on-chip PLL may be used to generate the required high frequency clock. The PLL input clock is 1 Fs, and may be input from LRCK-AUX, LRCK, or from XTI/XTO. In this last case, a 1 Fs clock may be input into XTI, or a 1 Fs crystal attached across XTI/XTO. When an external 1 Fs crystal is attached, extra components will be required, see Figure 1. The PLL will lock onto a new 1 Fs clock in about 90 ms. If the PLL input clock is removed, the VCO will drift to the low frequency end of its frequency range.

The PLL can also be used to lock to an S/PDIF data source on RX1, RX2, RX3, or RX4. Source selection is accomplished with the CS2/1/0 bits in the Clock Mode Byte. The PLL will lock to an S/PDIF source in about 90 ms.

Finally, the PLL has two filter loop current modes, normal and high current, that are selected via the LC bit in the Converter Control Byte. In the normal mode, the loop current is 25 µA. In the high current

mode, the loop current is 300 μA. The high current mode allows the use of lower impedance filter components which minimizes the influences of board contamination. See the table in Figure 1 for filter component values in each mode.

Master Clock Output

CLKOUT is a master clock output provided to allow synchronization of external components. Available CLKOUT frequencies of 1 Fs, 256 Fs, 384 Fs, and 512 Fs, are selectable by the CO0/1 bits of the Clock Mode Byte.

Generation of CLKOUT for 384 Fs and 512 Fs is accomplished with an on chip clock multiplier and may contain clock jitter. The source of the 256 Fs CLKOUT is the output of the PLL or a divided down clock from the XTI/XTO input. If 384 Fs is chosen as the input clock at XTI and 256 Fs is chosen as the output, CLKOUT will have approximately a 33% duty cycle. In all other cases CLKOUT will typically have a 50% duty cycle.

Synchronization

The DSP port and Auxiliary port must operate synchronously to the CS4226 clock source. The serial port will force a reset of the data paths in an attempt to resynchronize if non-synchronous data is input to the CS4226. It is advisable to mute the DACs when changing from one clock source to another to avoid the output of undesirable audio signals as the CS4226 resynchronizes.

Digital Interfaces

There are 3 digital audio interface ports: the audio DSP port, the auxiliary digital audio port, and the S/PDIF reciever. The serial data is represented in 2's complement format with the MSB-first in all formats.

Audio DSP Serial Interface Signals

The serial interface clock, SCLK, is used for transmitting and receiving audio data. The active edge of SCLK is chosen by setting the DSCK bit in the DSP Port Mode Byte. SCLK can be generated by the CS4226 (master mode) or it can be input from an external SCLK source (slave mode). Mode selection is set with the DMS1/0 bits in the DSP Port Mode Byte. The number of SCLK cycles in one system sample period is programmable to be 32, 48, 64, or 128 by setting the DCK1/0 bits in the DSP Port Mode Byte.

The Left/Right clock (LRCK) is used to indicate left and right data and the start of a new sample period. It may be output from the CS4226, or it may be generated from an external controller. The frequency of LRCK must be equal to the system sample rate, Fs.

SDIN1, SDIN2, and SDIN3 are the data input pins, each of which drive a pair of DACs. SDOUT1 and SDOUT2 can carry the output data from the two 20-bit ADC's, the mono ADC, the auxiliary digital audio port, and the S/PDIF receiver. Selection depends on the IS1/0 bits in the ADC control byte. The audio DSP port may also be configured so that all 6 DAC's data is input on SDIN1, and all 3 ADC's data is output on SDOUT1. Table 3 outlines the serial interface ports.

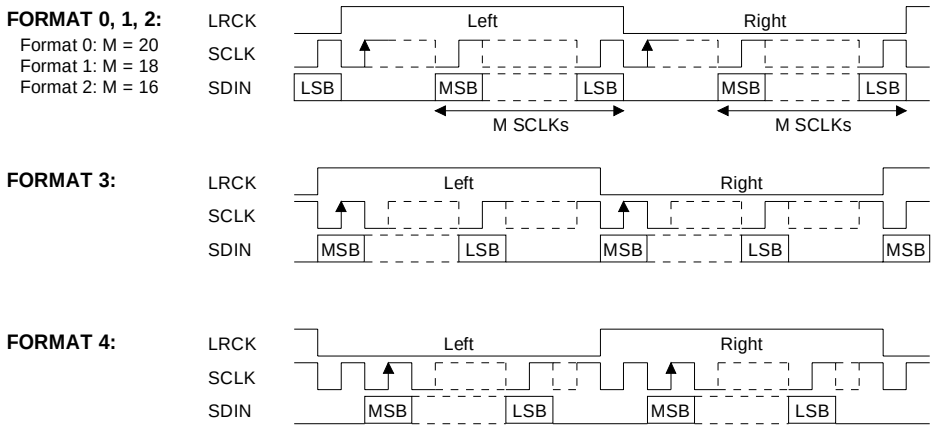
DAC Inputs		
SDIN1	left channel	DAC #1
	right channel	DAC #2
	single line	All 6 DAC channels
SDIN2	left channel	DAC #3
	right channel	DAC #4
SDIN3	left channel	DAC #5
	right channel	DAC #6

Table 3. DSP Serial Interface Ports

Audio DSP Serial Interface Formats

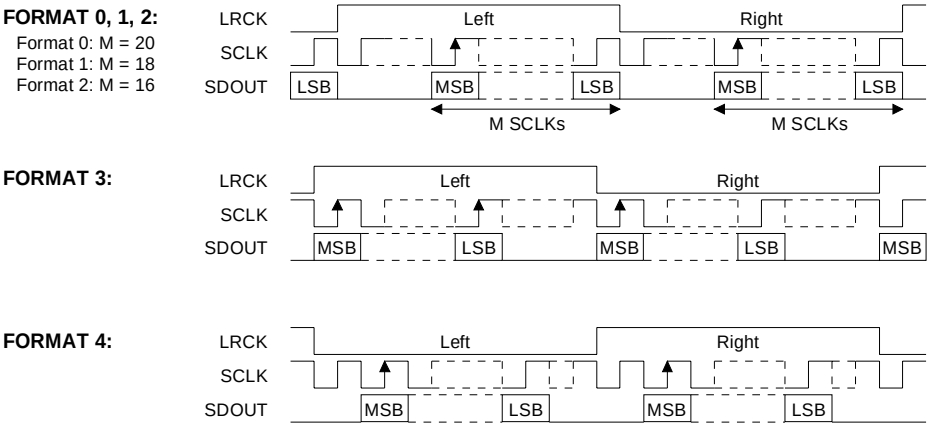
The audio DSP port supports 7 alternate formats, shown in Figures 4, 5, and 6. These formats are chosen through the DSP Port Mode Byte with the DDF2/1/0 bits.

Formats 5 and 6 are single line data modes where all DAC channels are combined onto a single input



Note: SCLK shown for DSCK = 0. SCLK inverted for DSCK = 1.

Figure 4. Audio DSP and Auxiliary Port Data Input Formats



Note: SCLK shown for DSCK = 0. SCLK inverted for DSCK = 1.

Figure 5. Audio DSP Port Data Output Formats

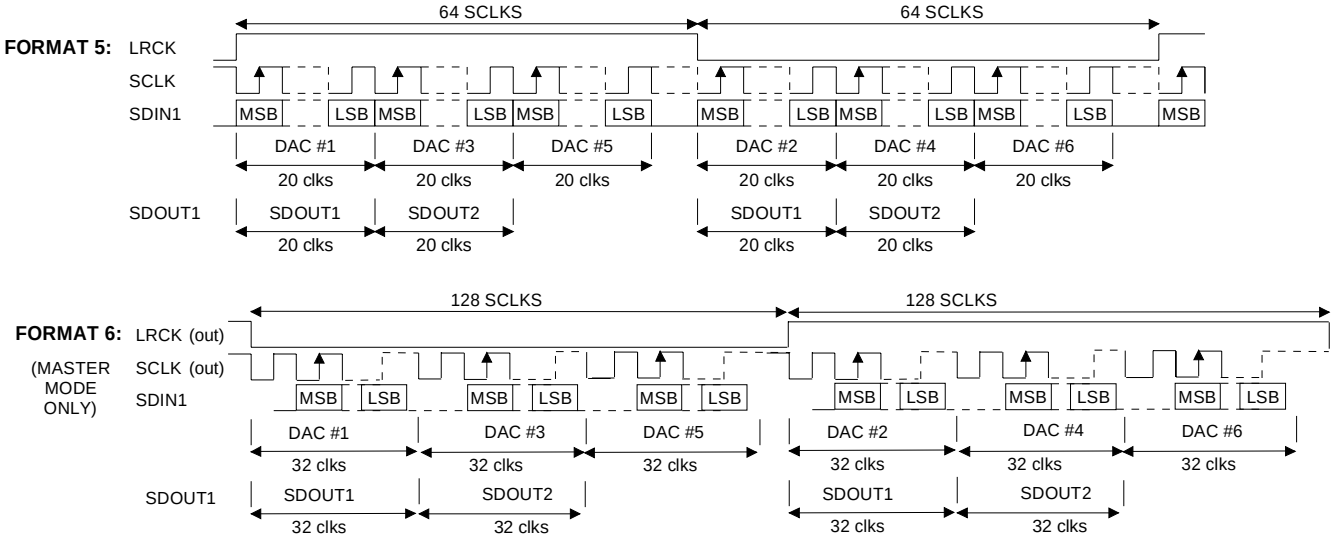


Figure 6. One data line modes

and all ADC channels are combined onto a single output. Format 6 is available in Master Mode only. See figure 6 for details.

Auxiliary Audio Port Signals

The auxiliary port provides an alternate way to input digital audio signals into the CS4226, and allows the CS4226 to synchronize the system to an external digital audio source. This port consists of serial clock, data and left/right clock pins named, SCLKAUX, DATAUX and LRCKAUX. The Auxiliary Audio Port input is output on SDOUT1 when the IS bits are set to 1 or 2 in the ADC Control Byte. Additionally, setting IS to 2 routes the stereo ADC outputs to SDOUT2. There is approximately a two frame delay from DATAUX to SDOUT1. When the auxiliary port is used, the frequency of LRCKAUX must equal to the system sample rate, Fs, but no particular phase relationship is required.

De-emphasis and muting on error conditions can be performed on input data to the auxiliary audio port; this is controlled by the Auxiliary Port Control Byte.

Auxiliary Audio Port Formats

Data input on DATAUX is clocked into the part by SCLKAUX using the format selected in the Auxiliary Port Mode Byte. The auxiliary audio port supports the same 5 formats as the audio DSP port in multi-data line mode. LRCKAUX is used to indicate left and right data samples, and the start of a new sample period. SCLKAUX and LRCKAUX may be output from the CS4226, or they may be generated from an external source, as set by the AMS1/0 control bits in the Auxiliary Port Mode Byte.

S/PDIF Receiver

The CS4226 reconfigures its auxiliary digital audio port as an S/PDIF receiver if CS2/1/0 in the Clock Mode Byte are set to be 4, 5, 6, or 7. In this mode RX1, RX2, RX3, or RX4 can be chosen as the S/PDIF input source.

The PLL will lock to the requested data source and setting IS1/0 = 1 or 2 in the ADC Control Byte routes the recovered output to SDOUT1 (channel A to left, channel B to right). All 24 received data bits will pass through the part to SDOUT1 except when the serial port is configured with 32 SCLK's per frame or in Format 5. For these cases, the 16 or 20 MSB's respectively will be output.

The error flags are reported in the Receiver Status Byte. The LOCK bit indicates whether the PLL is locked to the incoming S/PDIF data. Parity, Biphase, or Validity errors (PAR=1, BIP=1 or V=1) will cause the last valid data sample to be held at the receiver input until the error condition no longer is present (see Hold section). Mute on extended hold can also be enabled through the Auxiliary Port Control Byte (see Hold section).

Other error flags include confidence, CONF, and cyclic redundancy check, CRC. The CONF flag occurs when the received data eye opening is less than half a bit period. This indicates that the quality of the transmission link is poor and does not meet the digital audio interface standards. The CRC flag is updated at the beginning of a channel status block and is only valid when the professional format of channel status data is received. This error indicates when the CS4226 calculated CRC value does not match the CRC byte of the received channel status block.

The OVL/ERR pin will go high to flag an error. It is a latched logical OR of the Parity, Biphase, Validity, and Lock error flags in the Receiver Status Byte which is reset at the end of each frame. However, Parity, Biphase, or Validity errors can be masked from the pin by clearing the PM, BM, and VM bits respectively, of the Input Control Byte.

The first four bytes of the Channel Status block for both channel A and B can be accessed in the Receiver Channel Status Bytes. When the CV bit is

high, these bytes are being updated and may be invalid. Additionally, the audio/non-audio, AC-3/MPEG data stream indicator and sampling frequency channel status bits may be output to pins 9, 10, 11 and 12, respectively, see Table 4. This is accomplished by setting the CSP bit to 1 in the Auxiliary Status Output Byte. The FREQ0/1 channel status bit outputs are decoded from the sampling frequency channel status bits after first referencing channel status byte 0, bit 0 (PRO or consumer bit) which indicates the appropriate location of these bits in the channel status data stream.

The received user bit is output on the HOLD/RUBIT pin if the HPC bit in the AUX Port Control Byte is set to 1. It can be sampled with the rising or falling edge of LRCK if the audio DSP port is in Master Mode.

$\overline{\text{AUDIO}}$	Pin 9	0 - Audio data 1 - Non-audio data
AUTODATA	Pin 10	0 - No preamble detected in last 4096 frames 1 - Preamble detected
FREQ0/1	Pin 11/12	00 - 44.1 kHz 01 - 48 kHz 10 - Reserved 11 - 32 kHz

Table 4. S/PDIF Receiver Status Outputs

AC-3/MPEG Auto Detection

For AC-3/MPEG applications, it is important to know whether the incoming S/PDIF data stream is digital audio or compressed AC-3/MPEG data. This information is typically conveyed by setting channel status bit 1 (audio/non-audio bit), but some AC-3/MPEG sources may not strictly adhere to this convention and the bit may not be properly set. The CS4226 S/PDIF receiver has the capability to automatically detect whether the incoming data is a compressed AC-3/MPEG input. This is accomplished by looking for an AC-3/MPEG 96-bit sync code consisting of six 16-bit words. The 96-bit sync code consists of: 0x0000, 0x0000, 0x0000, 0x0000, 0xF872, and 0x4E1F. When the sync code is detected, the AUTODATA indicator (pin 10) will go high. If no additional sync codes are detected within the next 4096 frames, the AUTODATA indicator pin will return low until another sync code is detected.

Control Port Signals

The control port is used to load all the internal settings. The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has 2 modes: SPI and I^2C, with the CS4226 as a slave device. The SPI mode is selected by setting the $I^2C/\overline{SPI}$ pin low, and I^2C is selected by setting the $I^2C/\overline{SPI}$ pin high. The state of this pin is continuously monitored.

SPI Mode

In SPI mode, $\overline{CS}$ is the CS4226 chip select signal, CCLK is the control port bit clock, (input into the CS4226 from the microcontroller), CDIN is the input data line from the microcontroller, CDOUT is the output data line to the microcontroller, and the chip address is 0010000. Data is clocked in on the rising edge of CCLK and out on the falling edge.

Figure 7 shows the control port timing in SPI mode. To write to a register, bring $\overline{CS}$ low. The first 7 bits on CDIN form the chip address, and they must be 0010000. The eighth bit is a read/write indicator ($R/\overline{W}$), which should be low to write. The next 8 bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into register designated by the MAP. During writes, the CDOUT output stays in the high impedance state. It may be externally pulled high or low with a 47 kΩ resistor.

The CS4226 has a MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, then the MAP will stay constant for

successive reads or writes. If INCR is set to a 1, then MAP will auto increment after each byte is read or written, allowing block reads or writes of successive registers.

To read a register, the MAP has to be set to the correct address by executing a partial write cycle which finishes ($\overline{CS}$ high) immediately after the MAP byte. The auto MAP increment bit (INCR) may be set or not, as desired. To begin a read, bring $\overline{CS}$ low, send out the chip address and set the read/write bit (R/$\overline{W}$) high. The next falling edge of CCLK will clock out the MSB of the addressed register (CDOUT will leave the high impedance state). If the MAP auto increment bit is set to 1, the data for successive registers will appear consecutively.

I²C Mode

In I²C mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL, with the clock to data relationship as shown in Figure 8. There is no $\overline{CS}$ pin. Pins AD0, AD1 form the partial chip address. The upper 5 bits of the 7 bit address field must be 00100. To communicate with a CS4226, the LSBs of the chip address field, which is the first byte sent to the CS4226, should match the settings of the AD1, AD0 pins. The eighth bit of the address bit is the R/$\overline{W}$ bit (high for a read, low for a write). The next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a write, the next byte is the data to be written to the register pointed to by the MAP. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto increment bit in MAP, allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. I²C bus is a registered trademark of Philips Semiconductors.

Control Port Bit Definitions

All registers can be written and read back, except the DAC Status Report Byte, ADC Status Report Byte, Receiver Status Byte, and the Receiver Channel Status Bytes, which are read only. See the bit definition tables for bit assignment information.

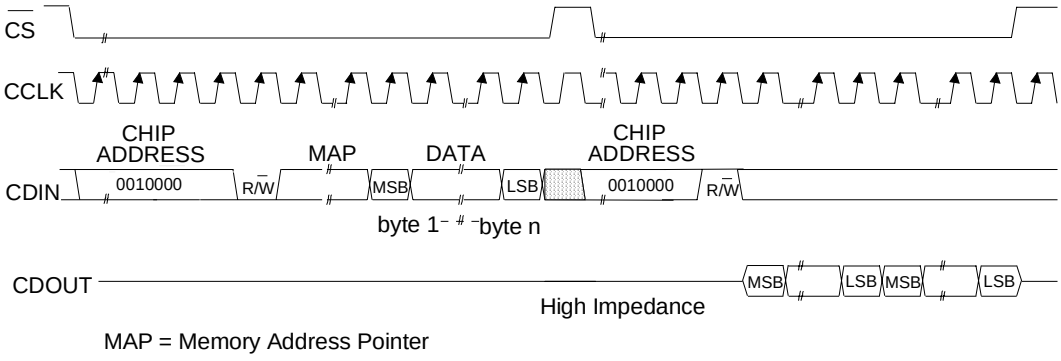
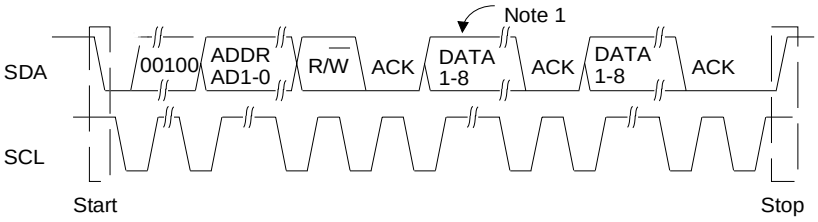


Figure 7. Control Port Timing, SPI mode



Note 1: If operation is a write, this byte contains the Memory Address Pointer, MAP.

Figure 8. Control Port Timing, I²C Mode

Power-up/Reset/Power Down Mode

Upon power up, the user should hold $\overline{PDN}$=0 until the system's power supply has stabilized. In this state, the control port is reset to its default settings. When $\overline{PDN}$ goes high, the device remains in a low power mode in which the control port is active, but CMOUT will not supply current. The desired settings should be loaded in while keeping the RS bit set to 1. Normal operation is achieved by setting the RS bit to zero in the Converter Control Byte. Once set to 0, the part powers up and an offset calibration occurs. This process lasts approximately 50 ms.

Reset/power down is achieved by lowering the $\overline{PDN}$ pin causing the part to enter power down. Once $\overline{PDN}$ goes high, the control port is functional and the desired settings should be loaded in while keeping the RS bit set to 1. The remainder of the chip remains in a low power reset state until the RS bit in the Converter Control Byte is set to 0.

The CS4226 will also enter a stand-by mode if the master clock source stops for approximately 10 µs or if the LRCK is not synchronous to the master clock. The control port will retain its current settings when in stand-by mode.

DAC Calibration

Output offset voltage is minimized by an internal calibration cycle. A calibration will automatically occur anytime the part comes out of reset, including the power-up reset, when the master clock source to the part changes by changing the CS or CI bits in the Clock Mode Byte or when the PLL goes out of lock and then re-locks.

The CS4226 can be re-calibrated whenever desired. A control bit, CAL, in the Converter Control Byte, is provided to initiate a calibration. The sequence is:

1) Set CAL to 1, the CS4226 sets CALP to 1 and begins to calibrate.
2) CALP will go to 0 when the calibration is completed.

Additional calibrations can be implemented by setting CAL to 0 and then to 1.

De-Emphasis

The S/PDIF receiver can be enabled to process 24 bits of received data (20 bits of audio data and four auxiliary bits) or process 20 bits of audio data (no auxiliary bits). Setting DEM24=0 in the Auxiliary Port Control Byte, will enable all 24 received data bits to be processed with de-emphasis when de-emphasis is enabled. When setting DEM24=1, the four auxiliary bits in the receiver data stream will pass through unchanged and only the 20 audio data bits will be processed.

The CS4226 is capable of digital de-emphasis for 32, 44.1, or 48 kHz sample rates. Implementation of digital de-emphasis requires reconfiguration of the digital filter to maintain the filter response shown in Figure 9 at multiple sample rates. The Auxiliary Port Control Byte selects the de-emphasis control method. De-emphasis may be enabled under hardware control, using the DEM pin (DEM2/1/0=4,5,6), by software control using the DEM bit (DEM2/1/0=0,1,2,3), or by the emphasis bits in the channel status data when the S/PDIF receiver is chosen as the clock source (DEM2/0/1=7). If no frequency information is present, the filter defaults to 44.1 kHz.

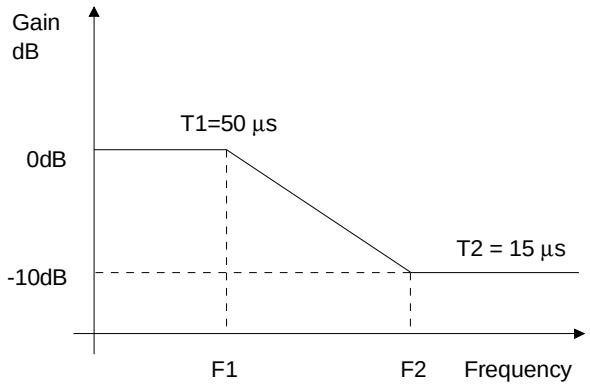


Figure 9. De-emphasis Curve

HOLD Function

If the digital audio source presents invalid data to the CS4226, the CS4226 may be configured to cause the last valid digital input sample to be held constant. Holding the previous output sample occurs when the user asserts the HOLD pin (HOLD=1) at any time during the stereo sample period, or if a parity, biphase, or validity error occurs when receiving S/PDIF data. Parity, biphase, and validity errors can be independently masked so that no hold occurs. This is done using the VM, PM, and BM bits in the Input Control Byte. During a HOLD condition, AUXPort (S/PDIF) input data is ignored.

DAC outputs can be automatically muted after an extended HOLD period (>15 samples) by setting the MOH (Mute On Hold) bit = 0 in the Auxiliary Port Control Byte. DACs will not be automatically muted when MOH=1. When the S/PDIF error condition is removed or the HOLD pin is de-asserted (HOLD=0), the DAC outputs will return to one of two different states controlled by the UMV (Unmute on Valid Data) bit in the Auxiliary Port Control Byte. When UMV=0, the DAC outputs will unmute when the error is removed. When UMV=1, the DACs must be unmuted in the DAC Control Byte after the error is removed. This allows the user to unmute the DAC after the invalid data has passed through the DSP.

Power Supply, Layout, and Grounding

As with any high resolution converter, the CS4226 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 1 shows the recommended power arrangement with VA connected to a clean +5V supply. VD should be derived from VA through a 2 ohm resistor. VD should not be used to power additional circuitry. Pins 18, 20, 39 and 41, AGND and DGND should be connected together at the CS4226. DGND for the CS4226 should not be confused with the ground for the digital section of the system. The CS4226 should be positioned over the analog ground plane near the digital/analog ground plane split. The analog and digital ground planes must be connected elsewhere in the system. The CS4226 evaluation board, CDB4226, demonstrates this layout technique. This technique minimizes digital noise and insures proper power supply matching and sequencing. Decoupling capacitors for VA, VD, and CMOUT should be located as close to the device package as possible. See Crystal's Application Note AN018: Layout and Design Rules for Data Converters and Other Mixed Signal Devices, and the CDB4226 evaluation board data sheet for recommended layout of the decoupling components.

The CS4226 will mute the analog outputs and enter the Power Down Mode if the supply drops below approximately 4 volts.

ADC and DAC Filter Response Plots

Figures 10 through 15 show the overall frequency response, passband ripple and transition band for the CS4226 ADC's and DAC's.

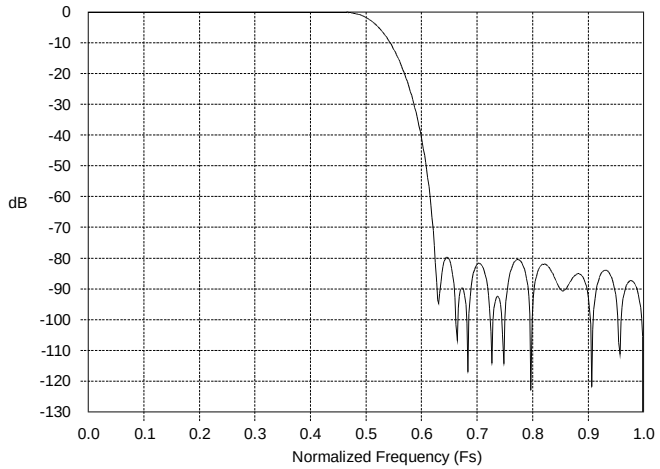


Figure 10. 20-bit ADC Filter Response

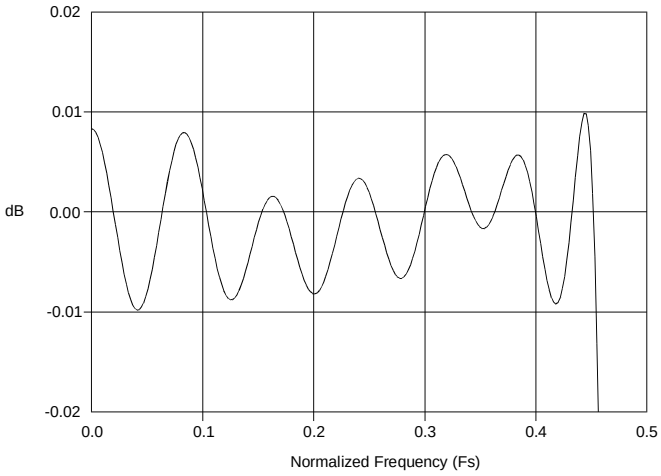


Figure 11. 20-bit ADC Passband Ripple

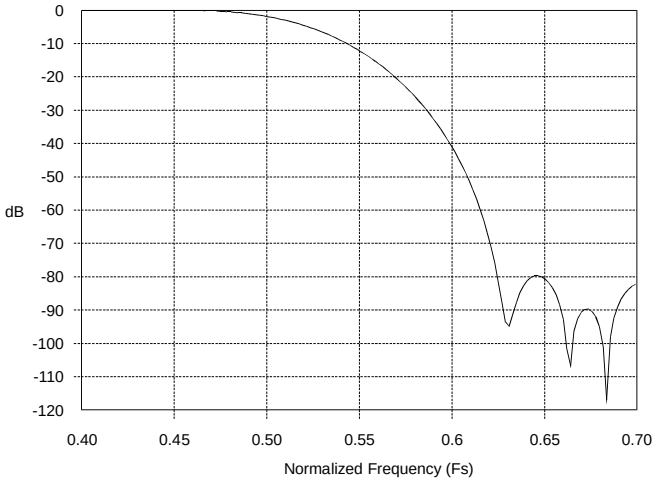


Figure 12. 20-bit ADC Transition Band

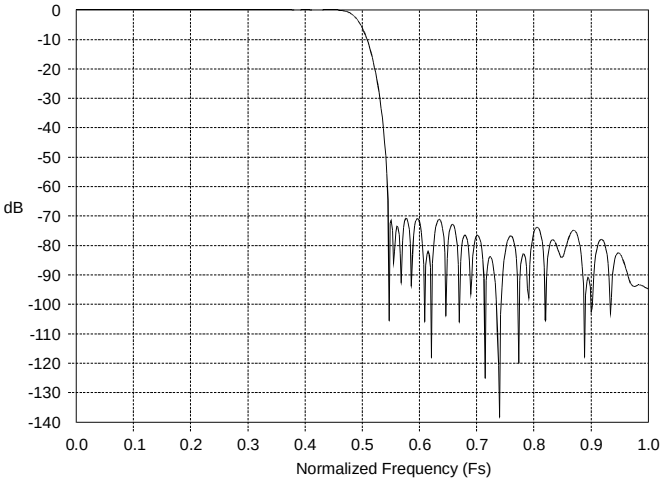


Figure 13. DAC Frequency Response

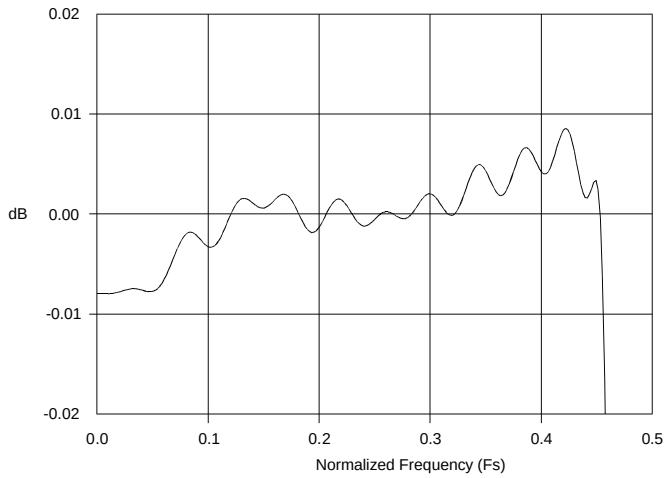


Figure 14. DAC Passband Ripple

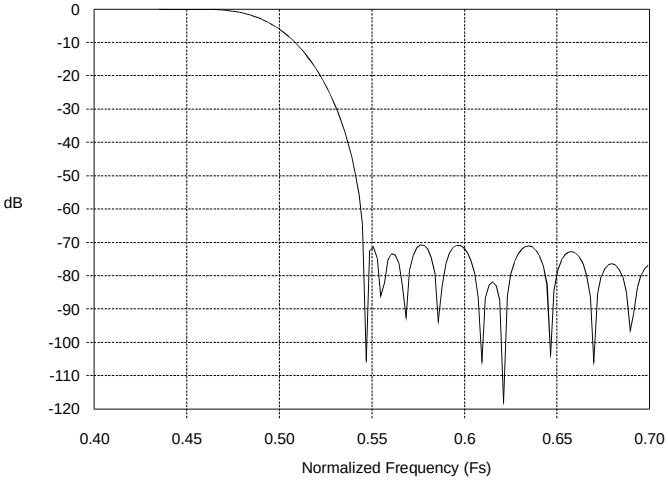


Figure 15. DAC Transition Band

REGISTER DESCRIPTION

Memory Address Pointer (MAP)

B7	B6	B5	B4	B3	B2	B1	B0
INCR	0	0	MAP4	MAP3	MAP2	MAP1	MAP0

MAP4-MAP0 Register Pointer

INCR Auto Increment Control Bit
0 - No auto increment
1 - Auto increment on

This register defaults to 01h.

Reserved Byte (0)

This byte is reserved for internal use and must be set to 00h for normal operation.

This register defaults to 00h.

Clock Mode Byte (01h)

B7	B6	B5	B4	B3	B2	B1	B0
0	CO1	CO0	CI1	CI0	CS2	CS1	CS0

CS2-CS0 Sets the source of the master clock.
0 - Crystal Oscillator or XTI at high frequency (PLL disabled)
1 - PLL driven by LRCKAUX at 1 Fs
2 - PLL driven by LRCK at 1 Fs
3 - PLL driven by XTI at 1 Fs
4 - PLL driven by RX1 data. This changes AUX port to S/PDIF port.
5 - PLL driven by RX2 data. This changes AUX port to S/PDIF port.
6 - PLL driven by RX3 data. This changes AUX port to S/PDIF port.
7 - PLL driven by RX4 data. This changes AUX port to S/PDIF port.

CI1-CI0 Determines frequency of XTI when PLL is disabled (not used if CS $\neq$ 0)
0 - 256 Fs
1 - 384 Fs
2 - 512 Fs
3 - not used

CO1-CO0 Sets CLKOUT frequency
0 - 256 Fs
1 - 384 Fs
2 - 512 Fs
3 - 1 Fs

This register defaults to 01h.

NOTE: If the sample rate on an input pin changes while using the PLL with RX1, RX2, RX3 or RX4, the PLL will not resynchronize to the new sample rate. You must either change input pins or change the Clock Mode Byte to something else and then change it back to the correct value. This will cause the PLL to resync.

Converter Control Byte (02h)

B7	B6	B5	B4	B3	B2	B1	B0
CALP	CLKE	DU	AUTO	LC	0	CAL	RS

RS — Chip reset (Do not clear this bit until all registers have been configured as desired)
0 - No Reset
1 - Reset

CAL — Calibration control bit
0 - Normal operation
1 - Rising edge initiates calibration

LC — Loop Current
0 - Normal Mode, 25µA PLL loop current (See Figure 1 for filter component values)
1 - High Current Mode, 300 µA PLL loop current (See Figure 1 for filter component values)

The following bits are read only:

AUTO — AC3 and MPEG Automatic Detection
0 - No AC3/MPEG Detected
1 - AC3/MPEG detected on RX/AUX

DU — Shows selected De-Emphasis setting used by DAC's
0 - Normal Flat DAC frequency response
1 - De-Emphasis selected

CLKE — Clocking system status
0 - No errors
1 - PLL is not locked, crystal is not oscillating, or requesting clock change in progress

CALP — Calibration status
1 - Calibration in progress
0 - Calibration doneThis register defaults to 01h

This register defaults to 01h

NOTE: The AC3 and MPEG detection for the AUTO bit does not look at the channel status bits. This bit is determined by looking for the AC3/MPEG header in the data stream. See the "AC3/MPEG Auto Detection" section earlier in the datasheet for more details.

DAC Control Byte (03h)

B7	B6	B5	B4	B3	B2	B1	B0
ZCD	MUTC	MUT6	MUT5	MUT4	MUT3	MUT2	MUT1

MUT6-MUT1 — Mute control bits
0 - Normal output level
1 - Selected DAC output muted

MUTC — Controls mute on consecutive zeros function
0 - 512 consecutive zeros will mute DAC
1 - DAC output will not mute on zeros

ZCD — Zero crossing disable
0 - DAC mutes and volume control changes occur on zero-crossings.
1 - DAC mutes and volume control changes occur immediately.

This register defaults to 3Fh.

Output Attenuator Data Byte (04h, 05h, 06h, 07h, 08h, 09h)

B7	B6	B5	B4	B3	B2	B1	B0
0	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

ATT6-ATT0 Sets attenuator level
0 - No attenuation
127 - 127 dB attenuation
ATT0 represents 1.0 dB of attenuation

This register defaults to 7Fh.

DAC Status Report Byte (Read Only) (0Ah)

B7	B6	B5	B4	B3	B2	B1	B0
0	-	ACC6	ACC5	ACC4	ACC3	ACC2	ACC1

ACC6-ACC1 Acceptance Bit
1 - New setting is waiting for zero-crossing to be accepted.
0 - ATT6-ATT0 has been accepted.

This register is read-only.

ADC Control Byte (0Bh)

B7	B6	B5	B4	B3	B2	B1	B0
IS1	IS0	0	AIS1	AIS0	MUTM	MUTR	MUTL

MUTL, MUTR, MUTM - Left, right and mono channel mute control
0 - Normal output level
1 - Selected ADC output muted

AIS1-AIS0 ADC analog input mux control
0 - Selects stereo pair 1
1 - Selects stereo pair 2
2 - Selects stereo pair 3
3 - Differential Input

IS1-IS0 Input mux selection
0 - Stereo ADC output to SDOUT1, Mono ADC output to SDOUT2
1 - Auxiliary Digital Input Port or S/PDIF Reciever to SDOUT1, Mono ADC output to SDOUT2
2 - Auxiliary Digital Input Port or S/PDIF Receiver to SDOUT1, Stereo ADC output to SDOUT2
3 - Not used.

This register defaults to 00h.

Input Control Byte (0Ch)

B7	B6	B5	B4	B3	B2	B1	B0
OVRM	VM	BM	PM	GNR1	GNR0	GNL1	GNL0

OVRM — ADC Overflow Mask
0- Error condition is masked at OLV/ERR pin and no DAC muting on extended hold
1- No Masking

VM — Validity Error Mask
0- Error condition is masked at OLV/ERR pin and no DAC muting on extended hold
1- No Masking

BM — Biphase Error Mask
0- Error condition is masked at OLV/ERR pin and no DAC muting on extended hold
1- No Masking

PM — Parity Error Mask
0- Error condition is masked at OLV/ERR pin and no DAC muting on extended hold
1- No Masking

GNL1-GNL0 — Sets left input gain
0 - 0 dB
1 - 3 dB
2 - 6 dB
3 - 9 dB

GNR1-GNR0 — Sets right input gain
0 - 0 dB
1 - 3 dB
2 - 6 dB
3 - 9 dB

This register defaults to 00h.

ADC Status Report Byte (Read Only) (0Dh)

B7	B6	B5	B4	B3	B2	B1	B0
LVM1	LVM0	LVR2	LVR1	LVR0	LVL2	LVL2	LVL0

LVL2-LVL0, LVR2-0 — Left and Right ADC output level
0 - Normal output levels
1 - -6 dB level
2 - -5 dB level
3 - -4 dB level
4 - -3 dB level
5 - -2 dB level
6 - -1 dB level
7 - Clipping

LVLM1-LVLM0 — Mono ADC output level
0 - Normal output level
1 - -6 dB level
2 - -3 dB level
3 - Clipping

These bits are 'sticky'. They constantly monitor the ADC output for the peak levels and hold the maximum output. They are reset to 0 when read.

This register is read only.

DSP Port Mode Byte (0Eh)

B7	B6	B5	B4	B3	B2	B1	B0
DCK1	DCK0	DMS1	DMS0	DSCK	DDF2	DDF1	DDF0

DDF2-DDF0 Data format
0 - Right justified, 20-bit
1 - Right justified, 18-bit
2 - Right justified, 16-bit
3 - Left justified, 20-bit in / 24-bit out
4 - I^2S compatible, 20-bit in / 24-bit out
5 - One Data Line Mode (Fig. 6)
6 - One Data Line (Master Mode only, Fig. 6)
7 - Not used

DSCK Set the polarity of clocking data
0 - Data clocked in on rising edge of SCLK, out on falling edge of SCLK
1 - Data clocked in on falling edge of SCLK, out on rising edge of SCLK

DMS1-DMS0 Sets the mode of the port
0 - Slave
1 - Master Burst - SCLKs are gated 128 fs clocks
2 - Master Non-Burst - SCLKs are evenly distributed (No 48 fs SCLK)
3 - not used - default to Slave

DCK1-DCK0 * Set number of bit clocks per Fs period
0 - 128
1 - 48 - Master Burst or Slave mode only
2 - 32 - All formats will default to 16 bits
3 - 64

This register defaults to 00h.

* DCK1-DCK0 are ignored in formats 5 and 6.

Auxiliary Port Mode Byte (0Fh)

B7	B6	B5	B4	B3	B2	B1	B0
ACK1	ACK0	AMS1	AMS0	ASCK	ADF2	ADF1	ADF0

This byte is not available when the receiver is functioning.

ADF2-ADF0 Data format
0 - Right justified, 20-bit data
1 - Right justified, 18-bit data
2 - Right justified, 16-bit data
3 - Left justified, 20-bit
4 - I^2S compatible, 20-bit
5 - Not used
6 - Not used
7 - Not used

ASCK Sets the polarity of clocking data
0 - Data clocked in on rising edge of SCLKAUX
1 - Data clocked in on falling edge of SCLKAUX

AMS1-AMS0 Sets the mode of the port.
0 - Slave
1 - Master Burst - SCLKAUXs are gated 128 fs clocks
2 - Master Non-Burst - SCLKAUXs are evenly distributed in LRCKAUX frame
3 - Not used - default to slave

ACK1-ACK0 Set number of bit clocks per Fs period.
0 - 128
1 - 48 - Master Burst or Slave mode only
2 - 32 - All input formats will default to 16 bits.
3 - 64

This register defaults to 00h.

Auxilliary Port Control Byte (10h)

B7	B6	B5	B4	B3	B2	B1	B0
CSP	HPC	UMV	MOH	DEM24	DEM2	DEM1	DEM0

DEM 2-0 Selects de-emphasis response/source
0 - De-emphasis off
1 - De-emphasis on 32 kHz
2 - De-emphasis on 44.1 kHz
3 - De-emphasis on 48 kHz
4 - De-emphasis pin 32 kHz
5 - De-emphasis pin 44.1 kHz
6 - De-emphasis pin 48 kHz
7 - S/PDIF receiver channel status bits

DEM24 Process AUX data LSBs
0 - All received data bits (24 max) are processed
1 - Top 20 bits processed with De-emphasis filter. 4 AUX LSBs are passed unchanged.

MOH Mute On Hold
0 - Extended Hold (16 frames) mutes DAC outputs
1 - DACs not muted

UMV Unmute on Valid Data
0 - DACs unmute when ERROR is removed
1 - DACs must be unmuted in DAC control byte after ERROR is removed.

HPC HOLD/RUBIT Pin Control
0 - HOLD/RUBIT is an input (HOLD)
1 - HOLD/RUBIT is an output(RUBIT)

CSP Channel Status output to pins.
0 - Analog inputs to pins. AIN2R, AIN2L, AIN3R, AIN3L
1 - Channel status to pins. (This forces AIS1/0=0)

This register defaults to 00h.

Receiver Status Byte (Read Only) (11h)

B7	B6	B5	B4	B3	B2	B1	B0
CV	0	CRC	LOCK	V	CONF	BIP	PAR

PAR — Parity bit
0 - No error
1 - Error

BIP — Biphase bit
0 - No error
1 - Error

CONF — Confidence bit
0 - No error
1 - Error

V — Validity bit
0 - No error
1 - Error

LOCK — PLL lock bit
0 - PLL locked
1 - Out of lock

CRC — Cyclic Redundancy check bit
0 - No error
1 - Error on either channel

CV — Channel status validity
0 - Valid
1 - Not valid, data is updating

This register is read only.

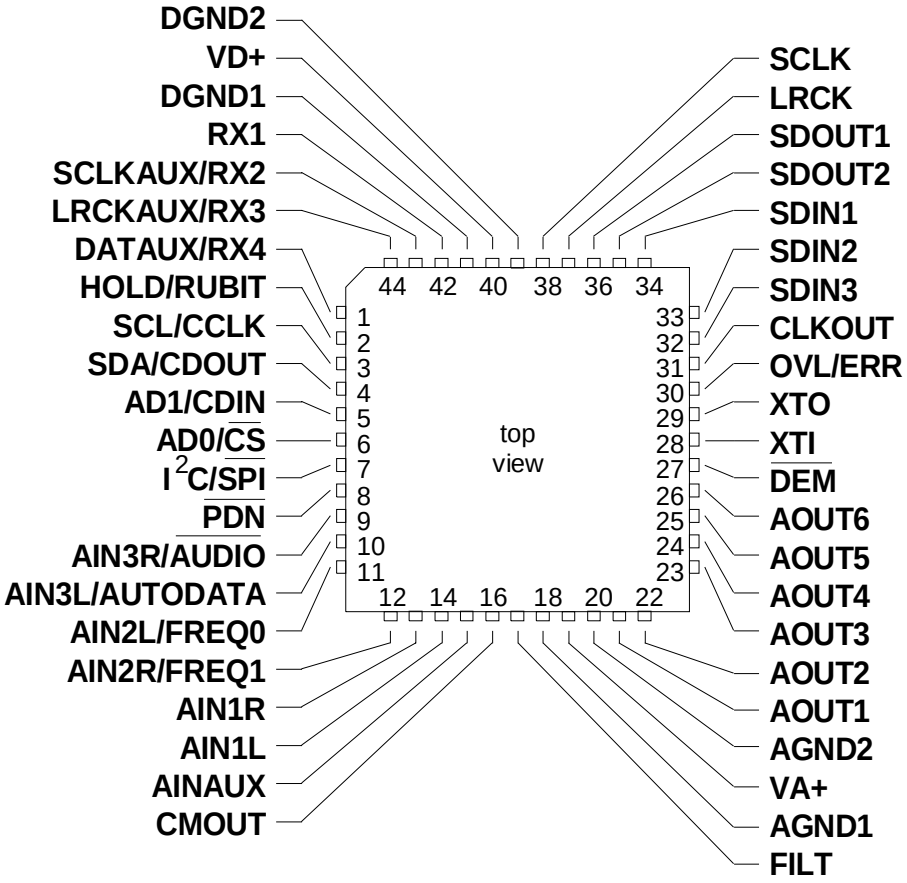
Receiver Channel Status Byte (Read Only) (12h, 13h, 14h, 15h, 16h, 17h, 18h, 19h)

B7	B6	B5	B4	B3	B2	B1	B0
CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0

Byte 12h	Channel A	Status Byte 1
Byte 13h	Channel A	Status Byte 2
Byte 14h	Channel A	Status Byte 3
Byte 15h	Channel A	Status Byte 4
Byte 16h	Channel B	Status Byte 1
Byte 17h	Channel B	Status Byte 2
Byte 18h	Channel B	Status Byte 3
Byte 19h	Channel B	Status Byte 4

Bit definition changes depending upon PRO bit setting. When CV = 1, these bits are updating and may be invalid.

PIN DESCRIPTION



Power Supply

VA+ - Analog Power Input, PIN 19.

+5 V analog supply.

AGND1, AGND2 - Analog Ground, PINS 18, 20.

Analog grounds.

VD+ - Digital Power Input, PIN 40.

+ 5 V digital supply.

DGND1, DGND2 - Digital Ground, PINS 41, 39.

Digital grounds.

Analog Inputs

AIN1L, AIN1R - Left and Right Channel Mux Input 1, PINS 14, 13.

Analog signal input connections for the right and left channels for multiplexer input 1.

AIN2L/FREQ0, AIN2R/FREQ1 - Left & Right Channel Mux Input 2/Channel Status Freq. Bits, PINS 11, 12.

Analog signal input connections for the right and left channels for multiplexer input 2. When CSP = 1, these pins are configured as channel status outputs indicating the sampling frequency.

AIN3L/AUTODATA, AIN3R/$\overline{\text{AUDIO}}$ - Left & Right Channel Mux Input 3/AC3 and MPEG Detect Output, PINS 10, 9.

Analog signal input connections for the right and left channels for multiplexer input 3. When CSP = 1, AIN3L is configured as an output indicating the presence of an AC-3 or MPEG data stream at the RX input and AIN3R is configured as a channel status output indicating audio/non-audio data at the RX input.

AINAUX - Auxiliary Line Level Input, PIN 15.

Analog signal input for the mono A/D converter.

Analog Outputs

AOUT1, AOUT2, AOUT3, AOUT4, AOUT5, AOUT6 - Audio Outputs, PINS 21 - 26.

The analog outputs from the 6 D/A converters. Each output can be independently controlled for output amplitude.

CMOUT - Common Mode Output, PIN 16.

This common mode voltage output may be used for level shifting when DC coupling is desired. The load on CMOUT must be DC only, with an impedance of not less than 50 kΩ. CMOUT should be bypassed with a 1.0 µF to AGND.

Digital Audio Interface Signals

SDIN1 - Serial Data Input 1, PIN 34.

Digital audio data for the DACs 1 and 2 is presented to the CS4226 on this pin. This pin is also used for one-line data input modes.

SDIN2 - Serial Data Input 2, PIN 33.

Digital audio data for the DACs 3 and 4 is presented to the CS4226 on this pin.

SDIN3 - Serial Data Input 3, PIN 32.

Digital audio data for the DACs 5 and 6 is presented to the CS4226 on this pin.

SDOUT1- Serial Data Output 1, PIN36.

Digital audio data from the 20-bit stereo audio ADCs is output from this pin. When IS = 1 or 2, DATAAUX or the S/PDIF receiver is output on SDOUT1. This pin is also used for one line data output modes.

SDOUT2 - Serial Data Output 2, PIN 35.

Digital audio data from the mono audio ADC is output from this pin. When IS = 2, the stereo audio ADC's are output from this pin

SCLK - Serial Port Clock I/O, PIN 38.

SCLK clocks digital audio data into the DACs via SDIN1/2/3, and clocks data out of the ADCs on SDOUT1/2. Active clock edge depends on the DSCK bit.

LRCK - Left/Right Select Signal I/O, PIN 37.

The Left/Right select signal. This signal has a frequency equal to the sample rate. The relationship of LRCK to the left and right channel data depends on the selected format.

$\overline{\text{DEM}}$ - De-emphasis Control, PIN 27.

When low, DEM controls the activation of the standard 50/15 µs de-emphasis filter for either 32, 44.1, or 48 kHz sample rates. This pin is enabled by the DEM2-0 bits in the Auxiliary Port Control Byte.

OVL/ERR - Overload Indicator, PIN 30.

This pin goes high if either of the stereo audio ADCs or the mono ADC is clipping. If the S/PDIF receiver is chosen as the clock source (CS = 4, 5, 6, 7), then the pin also goes high if there is an error in the Receiver Status Byte. Error and overloading can be masked using bits in the Input Control Byte.

Auxillary Digital Audio and S/PDIF Receiver Signals

RX1 - Receiver Channel 1, PIN 42.

This pin is a dedicated S/PDIF input channel configured as the clock source for the device via the CS2-0 bits.

DATAUX/RX4 - Auxiliary Data Input / Receiver Channel 4, PIN 1.

DATAUX is the auxiliary audio data input line, usually connected to an external digital audio source. As RX4, this pin is configured as S/PDIF input channel 4 via the control port.

LRCKAUX/RX3 - Auxiliary Word Clock Input or Output / Receiver Channel 3, PIN 44.

In auxiliary slave mode, LRCKAUX is a word clock (at Fs) from an external digital audio source. LRCKAUX can be used as the clock reference for the internal PLL. In auxiliary master mode, LRCKAUX is a word clock output (at Fs) to clock an external digital audio source. As RX3, this pin is configured as S/PDIF input channel 3 via the control port.

SCLKAUX/RX2 - Auxiliary Bit Clock Input or Output / Receiver Channel 2, PIN 43.

In auxiliary slave mode, SCLKAUX is the serial data bit clock from an external digital audio source, used to clock in data on DATAAUX. In auxiliary master mode, SCLKAUX is a serial data bit clock output. As RX2, this pin is configured as S/PDIF input channel 2 via the control port.

HOLD/RUBIT - S/PDIF Received User Bit / HOLD Control, PIN 2.

When the S/PDIF receiver is chosen as the clock source (CS = 4, 5, 6 and HPC = 1), then this pin outputs the received user bit. When HPC = 0, this pin is sampled on the active edge of SCLKAUX. If it is high any time during the frame, DATAUX data is ignored and the previous "good" sample is output to the serial output port.

Control Port Signals

$I^2C/\overline{SPI}$ - Control Port Format, PIN 7.

Setting this pin high configures the control port for the I^2C interface; a low state configures the control port for the SPI interface . The state of this pin sets the function of the control port input/output pins .

SCL/CCLK - Serial Control Interface Clock, PIN 3.

SCL/CCLK is the serial control interface clock, and is used to clock control bits into and out of the CS4226.

AD0/$\overline{CS}$ - Address Bit / Control Port Chip Select, PIN 6.

In I^2C mode, AD0 is a chip address bit. In SPI software control mode, $\overline{CS}$ is used to enable the control port interface on the CS4226.

AD1/CDIN - Address Bit / Serial Control Data In, PIN 5.

In I^2C mode, AD1 is a chip address bit. In SPI software control mode, CDIN is the input data line for the control port interface.

SDA/CDOUT - Serial Control Data Out, PIN 4.

In I^2C mode, SDA is the control data I/O line. In SPI software control mode, CDOUT is the output data from the control port interface on the CS4226.

Clock and Crystal Pins

XTI, XTO - Crystal connections, PIN 28, 29.

Input and output connections for the crystal which may be used to operate the CS4226. Alternatively, a clock may be input into XTI.

CLKOUT - Master Clock Output, PIN 31.

CLKOUT allows external circuits to be synchronized to the CS4226. Alternate output frequencies are selectable by the control port.

Miscellaneous Pins

FILT - PLL Loop Filter Pin, PIN 15.

A capacitor, $C_{FILT,}$ in series with a resistor, R_{FILT}, should be connected from FILT to AGND. Additionally a capacitor, C_{RIP}, should be placed in parallel with C_{FILT} and R_{FILT}. See Figure 1 for recommended component values.

$\overline{\text{PDN}}$ - Powerdown Pin, PIN 8.

When low, the CS4226 enters a low power mode and all internal states are reset, including the control port. When high, the control port becomes operational and the RS bit must be cleared before normal operation will occur.

PARAMETER DEFINITIONS

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dbFs signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 20 Hz to 20 kHz), including distortion components. Expressed in decibels. ADCs are measured at -1dBFs as suggested in AES 17-1991 Annex A.

Idle Channel Noise / Signal-to-Noise-Ratio

The ratio of the rms analog output level with 1 kHz full scale digital input to the rms analog output level with all zeros into the digital input. Measured A-weighted over a 10 Hz to 20 kHz bandwidth. Units in decibels. This specification has been standardized by the Audio Engineering Society, AES17-1991, and referred to as Idle Channel Noise. This specification has also been standardized by the Electronic Industries Association of Japan, EIAJ CP-307, and referred to as Signal-to-Noise-Ratio.

Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the rms sum of all the in-band harmonics of the test signal. Units in decibels.

Interchannel Isolation

A measure of crosstalk between channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Frequency Response

A measure of the amplitude response variation from 20Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units are in decibels.

Gain Error

The deviation from the nominal full scale output for a full scale input.

Gain Drift

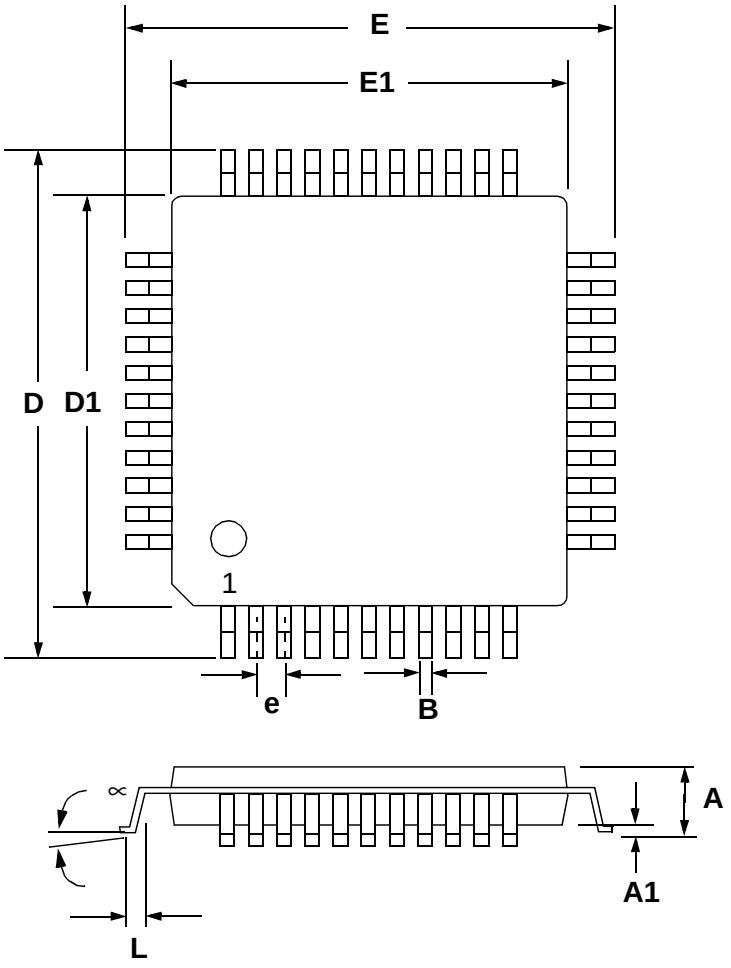
The change in gain value with temperature. Units in ppm/°C.

Offset Error

For the ADCs, the deviation in LSBs of the output from mid-scale with the selected input grounded. For the DACs, the deviation of the output from zero (relative to CMOUT) with mid-scale input code. Units are in volts.

PACKAGE DIMENSIONS

44L TQFP PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.000	0.065	0.00	1.60
A1	0.002	0.006	0.05	0.15
B	0.012	0.018	0.30	0.45
D	0.478	0.502	11.70	12.30
D1	0.404	0.412	9.90	10.10
E	0.478	0.502	11.70	12.30
E1	0.404	0.412	9.90	10.10
e	0.029	0.037	0.70	0.90
L	0.018	0.030	0.45	0.75
∝	0.000	7.000	0.00	7.00

JEDEC # : MS-026

• Notes •

Evaluation Board for CS4226

Features

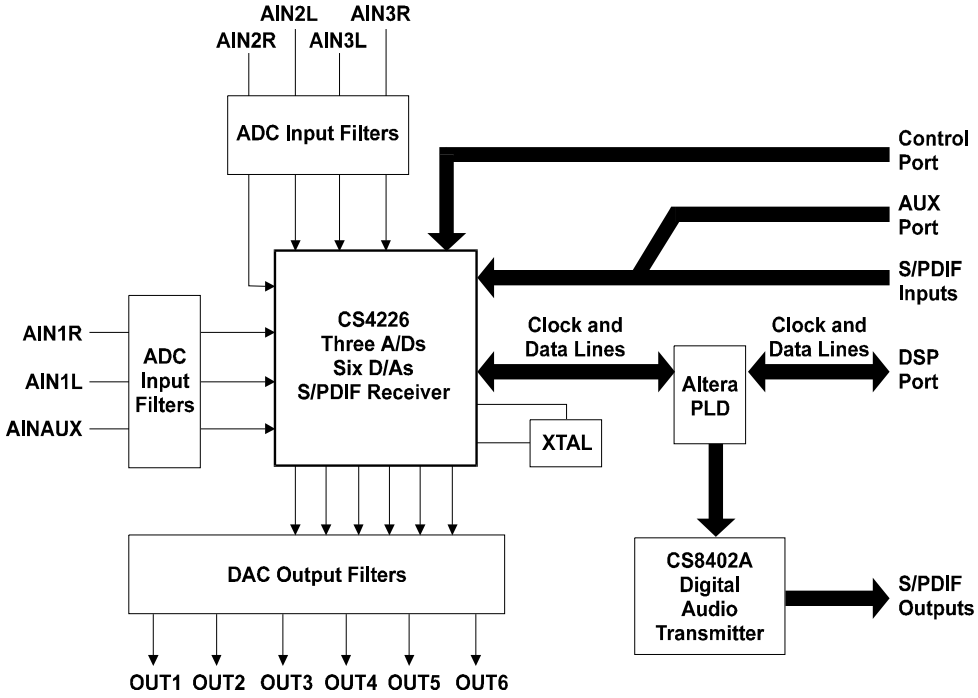
- CS4226 - Six 20-bit D/A Converters, Stereo 20-bit A/D Converters, Mono 20 bit A/D Converter, S/PDIF Receiver
- Multiple Stereo Input Source Selection
- Input and Output of Serial Audio Data Through Auxiliary and DSP Ports
- Input and Output of S/PDIF Interface Signals Through Coaxial and Optical Connections
- Control of CS4226 via SPI Software Interface
- Multiple Clock Options Available

General Description

The CDB4226 is useful for evaluating the performance of the CS4226. Up to three stereo input sources can be connected to the evaluation board, one of which is selected for A/D conversion. Six channels of D/A conversion allow for multi-channel applications such as Dolby Pro-Logic, Dolby Digital (AC-3), THX, and DSP-based soundfield applications. S/PDIF I/O support is provided by the CS4226's on-chip S/PDIF receiver and a CS8402A S/PDIF transmitter. For serial audio connections, access to the part's auxiliary and DSP ports is also provided. The board can be configured and controlled by a peripheral serial control port. The peripheral control options are SPI and I^2C. PC software which supports the board's SPI interface is provided, and can be used to set the internal control registers of the CS4226.

ORDERING INFORMATION

CDB4226	Evaluation Board



Cirrus Logic, Inc.
Crystal Semiconductor Products Division
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.crystal.com

CDB4226 SYSTEM OVERVIEW

The CDB4226 evaluation board is designed to allow thorough evaluation of the CS4226 surround sound codec. Six RCA jacks allow input of up to three stereo signal sources to the analog input multiplexer of the CS4226, plus one RCA jack for a monaural auxiliary input. One of the stereo pairs can be selected for the stereo 20 bit ADCs, while the auxiliary input is sent to the mono 20-bit ADC. The CS4226 also has six 20-bit DACs, whose outputs are filtered, buffered, and routed to six RCA jacks. Digital audio S/PDIF signals can be input to the CS4226's S/PDIF receiver through optical and coaxial connectors. A CS8402A digital audio transmitter provides optical and coaxial S/PDIF outputs. Serial audio data I/O is provided by the AUX port and the DSP port. Both ports can be configured to operate with numerous interface formats.

The CS4226 supports software control via the SPI and I^2C interfaces. A DB-25 connector is provided to allow connection to the serial control port. PC software is provided which establishes an SPI interface using the PC's printer port. This software provides a means for the user to read and write the control registers on the CS4226.

The CDB4226 schematic has been partitioned into 10 small schematics shown in Figures 3 through 12.

POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by six binding posts as shown in Figure 3. +5 VA and AGND provide 5 Volt power to the CS4226. The +/-12 V binding posts provide power to the analog input and output buffers. The +5 VD and GND binding posts supply 5 Volt power to the digital section of the board. All power supply connections are equipped with transient suppression diodes and bulk filtering capacitors.

ANALOG INPUTS

The CS4226 is capable of switching between three stereo pairs of line level inputs, and is equipped with a mono auxiliary input. The desired input is selected by setting the AIS1/0 bits in the ADC Control Byte and the CSP bit in the AUX Port Control Byte (consult the CS4226 data sheet for details on the configuration registers). The seven analog inputs (AIN1L, AIN1R, AIN2L, AIN2R, AIN3L, AIN3R, and AINAUX) are low-pass filtered and buffered, as shown in Figures 4 and 5 (-3 dB at 200 kHz). The AC coupling caps (C56-C62) allow the input pins of the CS4226 to self-bias to approximately 2.3 Volts. A nominal amplitude of 1 Vrms to these inputs will achieve a full scale digital output from the A/D converters in the CS4226. All inputs are noninverting.

AIN1L, AIN1R, and AINAUX are dedicated analog input connections to the CS4226. However, AIN2L, AIN2R, AIN3L, and AIN3R can also function as digital outputs (Figure 5). The output names are FREQ0, FREQ1, AUTODATA, and /AUDIO, respectively. When configured as outputs, these pins provide channel status information from the on-chip S/PDIF receiver (consult the CS4226 data sheet for details on pinout functionality). The status of these pins can be monitored with the LED's provided (D8-D9). The four jumpers HDR5-HDR8, defined in Table 1, are used in conjunction with the CSP bit in the Auxiliary Port Control Byte to configure these pins. When the CSP bit is a logic low, the pins become analog inputs. In this configuration, HDR5-HDR8 should be placed in the AIN position. When the CSP bit is a logic high, the pins become digital outputs; in this case HDR5-HDR8 should be placed in the CSOUT position. Note that the four jumpers should each be set to the same corresponding position.

The CS4226 also supports a differential input mode in which the single-ended inputs AIN3L and AIN2L become differential inputs AINL+ and AINL-, respectively. Likewise, the single-ended

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
HDR5, HDR6, HDR7, HDR8	Sets the direction of AIN3R/AUDIO, AIN3L/AUTODATA, AIN2L/FREQ0, and AIN2R/FREQ1. All four jumpers must be set to the same position, and correspond with the CSP bit in AUX Port Control Byte.	AIN CSOUT	Pins 9-12 on CS4226 are analog inputs (CSP=0). Pins 9-12 on CS4226 are channel status outputs (CSP=1).
XT_SEL	Selects the configuration for the XT pin on the DSP port. Jumper position must correspond with the DMS1/0 bits in the DSP Port Mode Byte and with the direction of the transceiver, U16.	XTIN XTAL XTOUT	XT is input to XTI. Y1 must be removed. U16 must be configured as input. XT is disconnected from XTI/XTO and is grounded through 47K resistor. XT outputs XTO clock from CS4226. U16 must be configured as output.
RX_SEL	Routes S/PDIF datastream from RX_OPT to one of three S/PDIF receiver input pins on the CS4226, RX2, 3, or 4. Jumper position must correspond with the CS2/1/0 bits in the Clock Mode Byte.	RX2 RX3 RX4 RX_AUXB	Sends optical input to RX2 of CS4226. Sends optical input to RX3 of CS4226. Sends optical input to RX4 of CS4226. Configures board for AUX port input.
CLK_SEL	Tristates CLKOUT1 on AUX_HDR, allowing AUX_HDR to be compatible with 10-pin serial data connectors found on other Crystal CDB capture boards.	CLKOFF CLKOUT1	Tristates CLKOUT1 buffer on U3. Enables CLKOUT1 buffer on U3.

Table 1. Jumper-selectable Options

inputs AIN2R and AIN1R become differential inputs AINR- and AINR+, respectively. Selection of the differential mode is made with the AIS1/0 bits in the ADC Control Byte. The balanced input configuration can be tested using special cables which have a male XLR connector on one end and a pair of RCA connectors on the other end.

ANALOG OUTPUTS

The six DAC outputs, AOUT1-AOUT6, are passed through a 2-pole Butterworth low-pass filter and are AC coupled, as shown in Figure 6 (-3 dB at 44.1 kHz). Each output will produce a nominal 1 Vrms output for a full scale digital input. Note that the filter outputs, OUT1-OUT6, are noninverting.

The output filters in Figure 6 have additional resistor and capacitor sockets to accomodate a 3-pole Butterworth filter This may be useful if increased out-of-band noise filtering is desired.

The CS4226 provides a common mode biasing voltage of approximately 2.3 V on its CMOUT pin. The CDB4226 analog inputs and outputs are AC coupled, and hence CMOUT is not required on the input and output filter stages. Since other filter topologies may need a common mode bias voltage, a buffered version of CMOUT is available on the test point labeled CMOUTFO (Figure 4).

CLOCK CONFIGURATIONS

The timing on the board should be generated by a single clock source, with the DSP port and AUX port operating synchronously to the selected clock source. Operating the serial audio interfaces at clock frequencies which deviate from each other will cause the CS4226 to reset its data paths in an attempt to resynchronize. Potential clock sources are:

1) the recovered clock from the S/PDIF receiver on the CS4226,

2) the LRCK or LRCKAUX inputs to the CS4226,
3) a 1 Fs, 256 Fs, 384 Fs, or 512 Fs crystal connected between XTI and XTO on the CS4226, or
4) a 1 Fs, 256 Fs, 384 Fs, or 512 Fs clock connected to XTI on the CS4226 from the XT clock line on the DSP port, DSP_HDR.

The clock source is chosen by setting the Clock Source bits, CS2/1/0 in the Clock Mode Byte, and by configuring the XT_SEL jumper, defined in Table 1, to the appropriate position, as described below.

XT_SEL Jumper and XT Clock Line

When the master clock for the board is derived from methods (1), (2), or (3), the XT_SEL jumper may be set to the XTAL position. This position disconnects the XT clock line on the DSP port (Figure 9) from the XTI/XTO clock and crystal pins of the CS4226 (Figure 7).

In case (3), the XT line can be set up to output the XTO signal from the CS4226. This configuration makes a buffered version of the crystal clock frequency available on the DSP port. This is accomplished by setting XT_SEL to the XTOUT position, and by configuring the bidirectional clock lines, XT, SCLK, and LRCK, to be outputs. The PC software can be used to set the DMS 1/0 bits in the DSP Port Mode Byte to 01 or 10, making the clock lines outputs on the CS4226. The PC software also generates a control line called SP_BUF, which controls the direction of the bidirectional transceiver, U16 (Figure 8). Care must be taken to ensure that the DMS bit settings correspond to the direction set by the software control line. Details on the software are given in the last section of this datasheet.

In case (4), the XT line can serve as the master clock source for the CDB4226. To configure the board in this manner, set the XT_SEL jumper to the XTIN position. Additionally, the XT, SCLK, and LRCK lines on the DSP port must be configured as inputs to the evaluation board. The PC software is used to set the DMS1/0 bits to 00 (LRCK and SCLK are inputs). Also, the software is used to set the direction of the bidirectional buffer, U16, so that XT, SCLK, and LRCK are buffered onto the board.

Notice that when XT is used as an external master clock source for the board, the SCLK and LRCK lines cannot be outputs. SCLK and LRCK must be sourced externally.

DIGITAL INPUTS

The CS4226 can accept digital audio signals in either serial form or S/PDIF form. The CS2/1/0 bits in the Clock Mode Byte are used in conjunction with the RX_SEL jumper (defined in Table 1) to configure the board for serial or S/PDIF data sources.

Serial Input Interface

Serial data can be received through the AUX port header, AUX_HDR (Figure 8), which provides access to the AUX port of the CS4226. The four clock and data lines on AUX_HDR are defined in Table 2. The CS4226 will accept serial data through the AUX port by setting the CS2/1/0 bits in the Clock Mode Byte to 0, 1, 2, or 3 (hex), and by moving the RX_SEL jumper to the RX_AUXB position.

Notice that the LRCLKAUX and SCLKAUX lines on the AUX port are bidirectional. The AMS1/0 bits in the Auxiliary Port Mode Byte determine the direction of the LRCLKAUX and SCLKAUX lines. The PC software generates a control line called AUX_BUF, which controls the direction of the bidirectional transceiver, U23 (Figure 8). Care must be taken to ensure that the AMS bits correspond to the direction set by the software control line. Details on the software are given in the last section of this datasheet.

A buffered version of CLKOUT, called CLKOUT1, is available on AUX_HDR. CLKOUT frequencies of 1 Fs, 256 Fs, 384 Fs, and 512 Fs can be selected using the CO1/0 bits in the Clock Mode

CONNECTOR NAME	CONNECTOR TYPE	INPUT / OUTPUT	SIGNAL PRESENT
+5 VA	binding post	input	+5 Volts for analog section
+5 VD	binding post	input	+5 Volts for digital section
+/- 12 V	binding post	input	+/- 12 Volts for analog input and output buffers
AGND	binding post	input	analog ground connection from power source
GND	binding post	input	digital ground connection from power source
AIN1L, AIN1R	RCA	inputs	left and right channel analog inputs, 1st stereo pair
AIN2L, AIN2R	RCA	inputs	left and right channel analog inputs, 2nd stereo pair
AIN3L, AIN3R	RCA	inputs	left and right channel analog inputs, 3rd stereo pair
AINAUX	RCA	input	auxiliary analog input
OUT1 - OUT6	RCA	outputs	six buffered and filtered DAC output channels
RX_DIG	RCA	input	coaxial input to RX1 of CS4226 S/PDIF receiver
RX_OPT	Toslink	input	optical input to RX2, 3, or 4 of CS4226 S/PDIF receiver
8402_DIG	RCA	output	CS8402A digital output via transformer
8402_OPT	Toslink	output	CS8402A digital output via optical transmitter
DATAUX	header (AUX_HDR)	input	AUX port serial data input
LRCLKAUX, SCLKAUX	header (AUX_HDR)	inputs/outputs	I/O for AUX port serial and left/right clocks
CLKOUT1	header (AUX_HDR)	output	buffered CLKOUT from CS4226
SCL/CCLK1	header (DSP_HDR)	input	serial control clock for I^2C interface
SDA/CDOUT1	header (DSP_HDR)	bidirectional	control data I/O line for I^2C interface
SDIN1, SDIN2, SDIN3	header (DSP_HDR)	inputs	DSP port serial data inputs
XT	header (DSP_HDR)	input/output	DSP port XTI input access, or buffered XTO from CS4226
CLKOUT	header (DSP_HDR)	output	buffered CLKOUT from CS4226
LRCK, SCLK	header (DSP_HDR)	inputs/outputs	I/O for DSP port serial and left/right clocks
SDOUT1, SDOUT2	header (DSP_HDR)	outputs	DSP port serial data outputs
PC CONN	DB-25	inputs/outputs	DB-25 connector to PC for SPI/I^2C control port signals

Table 2. System Connections

Byte. This clock line is useful for synchronizing external A/D converters or other peripheral components. CLKOUT1 can be tristated by selecting the position of the CLK_SEL jumper, defined in Table 1. This feature may be useful in interfacing other Crystal evaluation boards (CDB5330A and CDB5334/35 for example) to the CDB4226, as it prevents a drive contention on the MCLK output of these boards.

S/PDIF Input Interface

The optical and coaxial digital inputs labeled RX_OPT and RX_DIG (Figure 8) allow access to the on-chip S/PDIF receiver, which can receive and decode one of four S/PDIF input sources. Setting the CS2/1/0 bits in the Clock Mode Byte to 4, 5, 6, or 7 (hex) will configure the CS4226 to choose RX1, RX2, RX3, or RX4, respectively, as the S/PDIF input source. The coaxial input, RX_DIG, is dedicated to the RX1 input on the CS4226. The optical input, RX_OPT, can be routed to one of the three other S/PDIF receiver input pins by using the RX_SEL jumper. Setting RX_SEL to the RX2, RX3, or RX4 position will route the S/PDIF data from the optical input to the RX2, RX3, or RX4 pin of the codec.

DSP PORT

The DSP port header, DSP_HDR, provides access to the DSP port of the CS4226. The eleven clock, control, and data lines are defined in Table 2. The XT, SCLK, and LRCK lines can be inputs or outputs, and their I/O configuration is defined in the "Clock Configuration" section above. CLKOUT, SDOUT1, and SDOUT2 are buffered outputs from the CS4226. The serial data input lines, SDIN1, 2, and 3, provide external access to the SDIN1, 2, and 3 pins of the CS4226. The I^2C interface lines, labeled SDA/CDOUT1 and SCL/CCLK1, allow configuration of the CS4226 registers without having to use the PC connector, PC CONN.

The Altera EPM7032 programmable logic device (PLD), shown in Figure 11, is used to route serial audio data in several ways on the board. The switches on S2 labeled SDIN_M2/M1/M0 (Figure 11) select the input to the SDIN1, 2 and 3 pins of the CS4226. The various routing schemes are defined in Table 3. There are seven loopback configurations which are selected by setting SDIN_M2/M1/M0 to 0-6 (hex). To access the SDIN pins on the codec from the DSP port header, SDIN_M2/M1/M0 should be set to 7 (hex).

S/PDIF OUTPUT

A CS8402A digital audio transmitter, shown in Figure 9, allows serial data from either SDOUT1 or SDOUT2 to be transmitted in S/PDIF form through an optical transmitter (8402_OPT) and through an RCA connector (8402_DIG). The transmitter provides a convenient way to evaluate the performance of the A/D converters on the CS4226.

The DIP switches SW1 and S2 (Figure 9) configure the PLD to adjust the clock and data outputs of the CS4226 to the format requirements of the CS8402A. The functionality of each switch is described below.

CS8402A MCLK Generation

The CLKOUT signal of the CS4226 can be 1 Fs, 256 Fs, 384 Fs, or 512 Fs. The CS8402A requires a master clock frequency of 128 Fs to operate. When CLKOUT is 1 Fs, the CS8402A will be inoperable. However, to accomodate the other possible frequencies of CLKOUT, the evaluation board can be configured to divide CLKOUT by 2, 3, or 4 to generate a 128 Fs master clock for the transmitter. The switches on SW1 labeled MCLK_S1 and MCLK_S0 select the degree of clock division as defined in Table 3.

CS8402A Format Selection

The five switches on SW1 and S2 labeled SP_RISING, SP_L_RB, BITS1, BITS0, and I2S are used to select the correct digital interface format for the CS8402A. These switches are defined in Table 3. Their settings must correspond with the DSCK and DDF2/1/0 bits in the DSP Port Mode Byte register. Table 4 shows which DSP Port Mode Byte settings the CS8402A can support for S/PDIF transmission. All other settings not listed in the table are not valid.

SDOUTx Output Selection

The switch on S2 labeled SDOUT_M0 selects the source of data to the CS8402A. A logic low selects SDOUT1 for transmission, and a logic high selects SDOUT2.

SW1 SWITCH #	0 = closed, 1 = open	Comment
6, 5	MCLK_S1, MCLK_S0	Divides CLKOUT to generate MCLK_8402 for CS8402A transmitter.
	0 0	Generates a 128 Fs clock when CLKOUT = 256 Fs (CO = 0).
	0 1	RESERVED
	1 0	Generates a 128 Fs clock when CLKOUT = 384 Fs (CO = 1).
	1 1	Generates a 128 Fs clock when CLKOUT = 512 Fs (CO = 2).
4	SP_RISING	Selects SCLK valid data edge. This bit must agree with DSCK bit in DSP Port Mode Byte.
	0	Data is clocked into CS8402A on falling edge of SCLK (DSCK = 1).
	1	Data is clocked into CS8402A on rising edge of SCLK (DSCK = 0).
3	SP_L_RB	Selects left or right justified data. This bit must agree with DDF bits in DSP Port Mode Byte.
	0	Serial data lines are right justified (DDF = 0,1,2).
	1	Serial data lines are left justified (DDF ≠ 0,1,2).
2, 1	BITS1, BITS0	Selects bits of resolution. These bits must agree with DDF bits in DSP Port Mode Byte.
	0 0	16 bits (DDF = 2)
	0 1	18 bits (DDF = 1)
	1 0	20 bits (DDF = 0, 3)
	1 1	RESERVED
S2 SWITCH #	**0 = closed, 1 = open**	**Comment**
5	I^2S	Selects I^2S compatible mode. This bit must agree with DDF bits in DSP Port Mode Byte.
	0	I^2S mode off (DDF ≠ 4).
	1	I^2S mode on (DDF = 4).
4	SDOUT_M0	Selects the source of data to the CS8402A.
	0	SDOUT1 from CS4226 is routed to SDATA pin of CS8402A.
	1	SDOUT2 from CS4226 is routed to SDATA pin of CS8402A.
3, 2, 1	SDIN_M2, SDIN_M1, SDIN_M0	Selects the source of data to SDIN1, 2, and 3 on the CS4226. Choices are SDOUT lines from the CS4226, SDIN lines from DSP_HDR, or zeros.
	0 0 0	SDOUT1 => SDIN1, 0 => SDIN2, 0 => SDIN3
	0 0 1	0 => SDIN1, SDOUT1 => SDIN2, 0 => SDIN3
	0 1 0	0 => SDIN1, 0 => SDIN2, SDOUT1 => SDIN3
	0 1 1	SDOUT1 => SDIN1, SDOUT1 => SDIN2, SDOUT1 => SDIN3
	1 0 0	SDOUT2 => SDIN1, SDOUT2 => SDIN2, SDOUT2 => SDIN3
	1 0 1	SDOUT1 => SDIN1, SDOUT1 => SDIN2, SDOUT2 => SDIN3
	1 1 0	SDOUT1 => SDIN1, SDOUT2 => SDIN2, SDOUT2 =>SDIN3
	1 1 1	SDIN1_HDR =>SDIN1, SDIN2_HDR =>SDIN2, SDIN3_HDR =>SDIN3

Table 3. DIP Switch Definitions

DSP Port Mode Byte	1 = open, 0 = closed, X = don't care, N/A = not available	SW1: #4	SW1: #3	SW1: #2, #1	S2: #5
(hex)	Descriptor	SP_RISING	SP_L_RB	BITS1/ BITS0	I^2S
	DCK1-DCK0 = 00, 01, or 11 => 128, 48, or 64 bit clocks per Fs period.				
01, 41, C1	CS4226 slave, valid data on SCLK rising edge, right-justified, 18 bit	1	0	01	0
02, 42, C2	CS4226 slave, valid data rising edge, right-justified, 16 bit	1	0	00	0
03, 43, C3	CS4226 slave, valid data rising edge, left-justified, 20 bit in, 24 bit out	1	1	10	0
04, 44, C4	CS4226 slave, valid data rising edge, I^2S, 20 bit in, 24 bit out	1	X	XX	1
09, 49, C9	CS4226 slave, valid data on SCLK falling edge, right-justified, 18 bit	0	0	01	0
0A, 4A, CA	CS4226 slave, valid data falling edge, right-justified, 16 bit	0	0	00	0
0B, 4B, CB	CS4226 slave, valid data falling edge, left-justified, 20 bit in, 24 bit out	0	1	10	0
0C, 4C, CC	CS4226 slave, valid data falling edge, I^2S, 20 bit in, 24 bit out	0	X	XX	1
11, 51, D1	CS4226 master burst, valid data on SCLK rising edge, right-justified, 18 bit	1	0	01	0
12, 52, D2	CS4226 master burst, valid data rising edge, right-justified, 16 bit	1	0	00	0
13, 53, D3	CS4226 master burst, valid data rising edge, left-justified, 20 bit in, 24 bit out	1	1	10	0
14, 54, D4	CS4226 master burst, valid data rising edge, I^2S, 20 bit in, 24 bit out	1	X	XX	1
19, 59, D9	CS4226 master burst, valid data on SCLK falling edge, right-justified, 18 bit	0	0	01	0
1A, 5A, DA	CS4226 master burst, valid data falling edge, right-justified, 16 bit	0	0	00	0
1B, 5B, DB	CS4226 master burst, valid data falling edge, left-justified, 20 bit in, 24 bit out	0	1	10	0
1C, 5C, DC	CS4226 master burst, valid data falling edge, I^2S, 20 bit in, 24 bit out	0	X	XX	1
21, E1	CS4226 master nonburst, valid data on SCLK rising edge, right-justified, 18 bit	1	0	01	0
22, E2	CS4226 master nonburst, valid data rising edge, right-justified, 16 bit	1	0	00	0
23, E3	CS4226 master nonburst, valid data rising edge, left-justified, 20 bit in, 24 bit out	1	1	10	0
24, E4	CS4226 master nonburst, valid data rising edge, I^2S, 20 bit in, 24 bit out	1	X	XX	1
29, E9	CS4226 master nonburst, valid data on SCLK falling edge, right-justified, 18 bit	0	0	01	0
2A, EA	CS4226 master nonburst, valid data falling edge, right-justified, 16 bit	0	0	00	0
2B, EB	CS4226 master nonburst, valid data falling edge, left-justified, 20 bit in, 24 bit out	0	1	10	0
2C, EC	CS4226 master nonburst, valid data falling edge, I^2S, 20 bit in, 24 bit out	0	X	XX	1
	DCK1-DCK0 = 10 =>32 bit blocks per Fs period (all formats default to 16 bits)				
80, 81, 82	CS4226 slave, valid data on SCLK rising edge, right-justified,16 bit	1	0	00	0
83	CS4226 slave, valid data rising edge, left-justified, 16 bit	1	1	XX	0
84	CS4226 slave, valid data rising edge, I^2S, 16 bit	1	X	XX	1
88, 89, 8A	CS4226 slave, valid data on SCLK falling edge, right-justified, 16 bit	0	0	00	0
8B	CS4226 slave, valid data falling edge, left-justified, 16 bit	0	1	00	0
8C	CS4226 slave, valid data falling edge, I^2S, 16 bit	0	X	XX	1
90, 91, 92	CS4226 master burst, valid data on SCLK rising edge, right-justified, 16 bit	1	0	00	0
93	CS4226 master burst, valid data rising edge, left-justified, 16 bit	1	1	00	0
94	CS4226 master burst, valid data rising edge, I^2S, 16 bit	1	X	XX	1
98, 99, 9A	CS4226 master burst, valid data on SCLK falling edge, right-justified, 16 bit	0	0	00	0
9B	CS4226 master burst, valid data falling edge, left-justified, 16 bit	0	1	00	0
9C	CS4226 master burst, valid data falling edge, I^2S, 16 bit	0	X	XX	1
A0, A1, A2	CS4226 master nonburst, valid data on SCLK rising edge, right-justified, 16 bit	1	0	00	0
A3	CS4226 master nonburst, valid data rising edge, left-justified, 16 bit	1	1	00	0
A4	CS4226 master nonburst, valid data rising edge, I^2S, 16 bit	1	X	XX	1
A8, A9, AA	CS4226 master nonburst, valid data on SCLK falling edge, right-justified, 16 bit	0	0	00	0
AB	CS4226 master nonburst, valid data falling edge, left-justified, 16 bit	0	1	00	0
AC	CS4226 master nonburst, valid data falling edge, I^2S, 16 bit	0	X	XX	1

Table 4. DSP Port Formats Supported by CS8402A Transmitter

SPI CONTROL PORT SOFTWARE

The SPI/I^2C port can be accessed through the DB-25 connector, PC CONN. Software is provided which allows reading and writing of the CS4226 control port registers with a PC using the SPI format. The supplied cable should be attached between PC CONN and the PC parallel port.

Software Description

Four C programs have been compiled to operate under MS-DOS. These programs can be run directly from the floppy disk provided. A brief description of the supplied routines is given. To see a full argument list for each routine, simply type the command with no arguments.

RSTSPI

Send a brief reset to the board. This is the same as depressing the /PDN switch.

RDSPI <map>

This routine returns the value located in the register pointed to by <map>. The <map> value is in hex and the value returned is in hex.

WRSPI <map> <data>

This routine writes the <data> into the register pointed to by <map>. Both values are in hex.

DUMPSPI <map>

This routine dumps the value of all the registers starting at <map> up to register 25.

RDPSI, WRSPI, and DUMPSPI have an optional argument "-pXX", defined in Table 5. This argument is used to set the direction of the bidirectional transceivers, U23 (Figure 8) and U16 (Figure 9). The "-pXX" argument must be sent at least once after powerup to configure the evaluation board to recognize whether the AUX port and DSP port are in master mode (clock lines are outputs) or in slave mode (clock lines are inputs). The "-pXX" argument should be set with consideration of setting the DMS bits in the DSP Port Mode Byte and the AMS bits in the Auxiliary Port Mode Byte.

Optional Argument	Description
-p00	CS4226 AUX port is master, DSP port is master (User must set AMS=2, DMS=2)
-p08	CS4226 AUX port is master, DSP port is slave (User must set AMS=2, DMS=0)
-p10	CS4226 AUX port is slave, DSP port is master (User must set AMS=0, DMS=2)
-p18	CS4226 AUX port is slave, DSP port is slave (User must set AMS=0, DMS=0)
-e <hex>	<hex> specifies an ending register on DUMPSPI

Table 5. Optional Software Switch Statements for RDSPI, WRSPI, and DUMPSPI commands

Pre-Configured Setups

For ease of implementation, batch files are provided along with the required jumper and dip switch settings for two modes of operation. Choice of operation mode is based primarily on the desired source of the data. All jumper settings not mentioned remain unchanged.

1: Receiver Mode

The clock source is a recovered clock from the S/PDIF coax input, RX_DIG. Recovered data is transmitted by the CS8402A. Additionally, SDOUT1 data is looped back to the DACs. Type "powuprx1" at the appropriate prompt to run the batch file for this mode of operation.

Signal Flow:

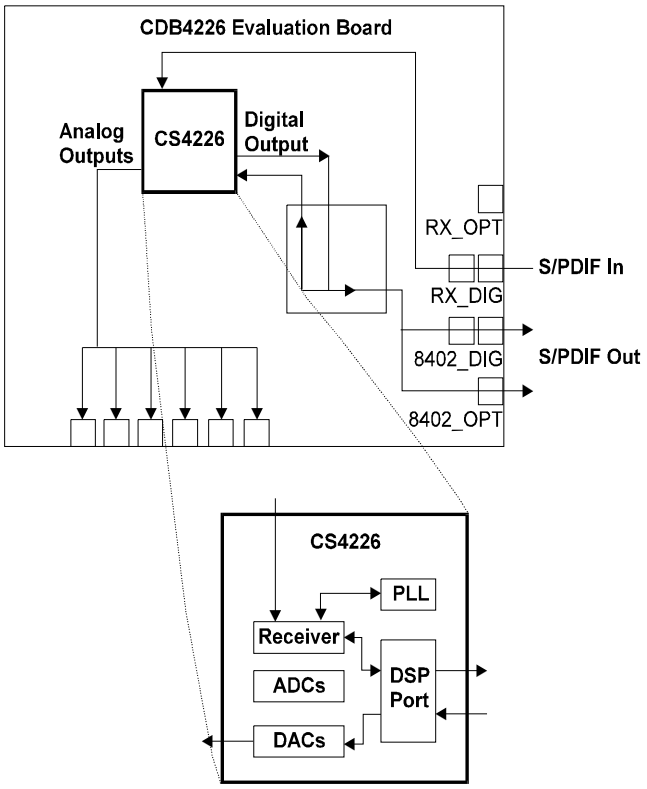


Figure 1. CDB4226 in Receiver Mode

DIP Switch Settings:

LOCATED ON S2

SDIN_M0 - 1 = >OPEN
SDIN_M1 - 1 = >OPEN
SDIN_M2 - 0 = >CLOSED
SDOUT_M0 -0 = >CLOSED
I^2S - 0 = >CLOSED

LOCATED ON SW1

BITS0 - 0 = >CLOSED
BITS1 -1 = > OPEN
SP_L_RB - 1 = >OPEN
SP_RISING - 0 = >CLOSED
MCLK_S0 - 0 = >CLOSED
MCLK_S1 - 0 = >CLOSED

Jumper Settings:

XT_SEL - XTAL
RX_SEL - RX2, RX3 or RX4
HRDR5,6,7,8 - CSOUT

Batch File:

POWUPRX1.BAT

2: Crystal mode

The clock source is a crystal (Y1). Stereo ADC output data is transmitted by the CS8402A. SDOUT1 data is looped back to the DACs. The stereo signal is applied to stereo pair 1 on the evaluation board (AIN1L/R). Type "powupxtl" at the appropriate prompt to run the batch file for this mode of operation.

Signal Flow:

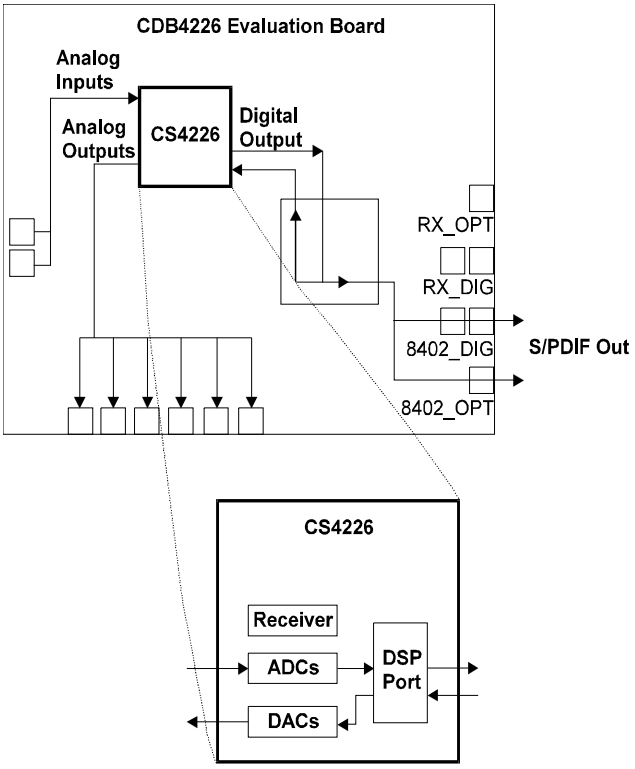


Figure 2. CDB4226 in Crystal Mode

DIP Switch Settings:

LOCATED ON S2

SDIN_M0 - 1 = >OPEN
SDIN_M1 - 1 = >OPEN
SDIN_M2 - 0 = >CLOSED
SDOUT_M0 - 0 = >CLOSED
I^2S - 0 = >CLOSED

LOCATED ON SWI

BITS0 - 0 = >CLOSED
BITS1 - 1 = >OPEN
SP_L_RB - 1 = >OPEN
SP_RISING - 0 = >CLOSED
MCLK_S0 - 0 = >CLOSED
MCLK_S1 - 0 = >CLOSED

JumperSettings:

HRDR5,6,7,8 - AIN
XT_SEL - XTAL

Batch File:

POWUPXTL.BAT

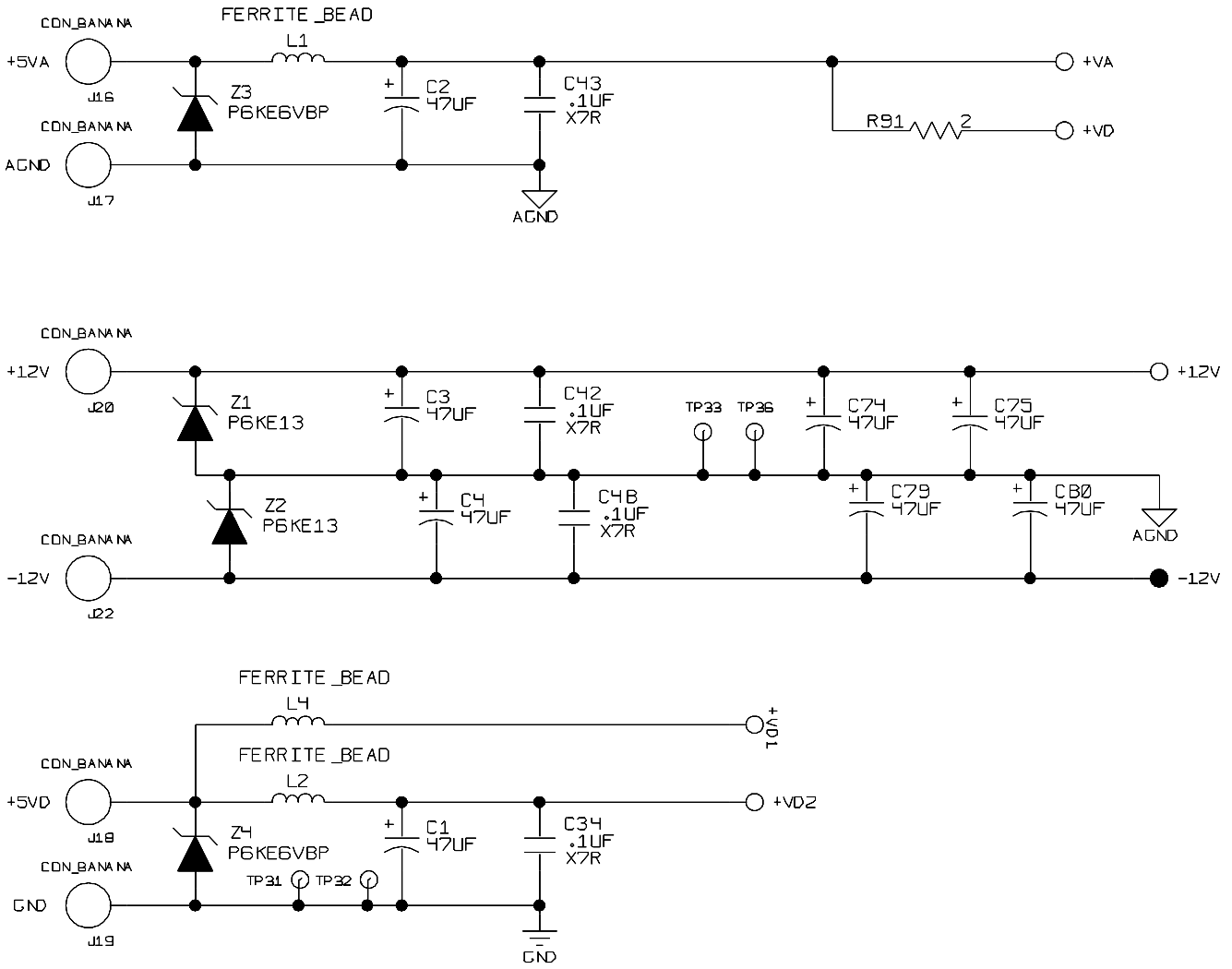


Figure 3. Power Supply and Bulk Filtering

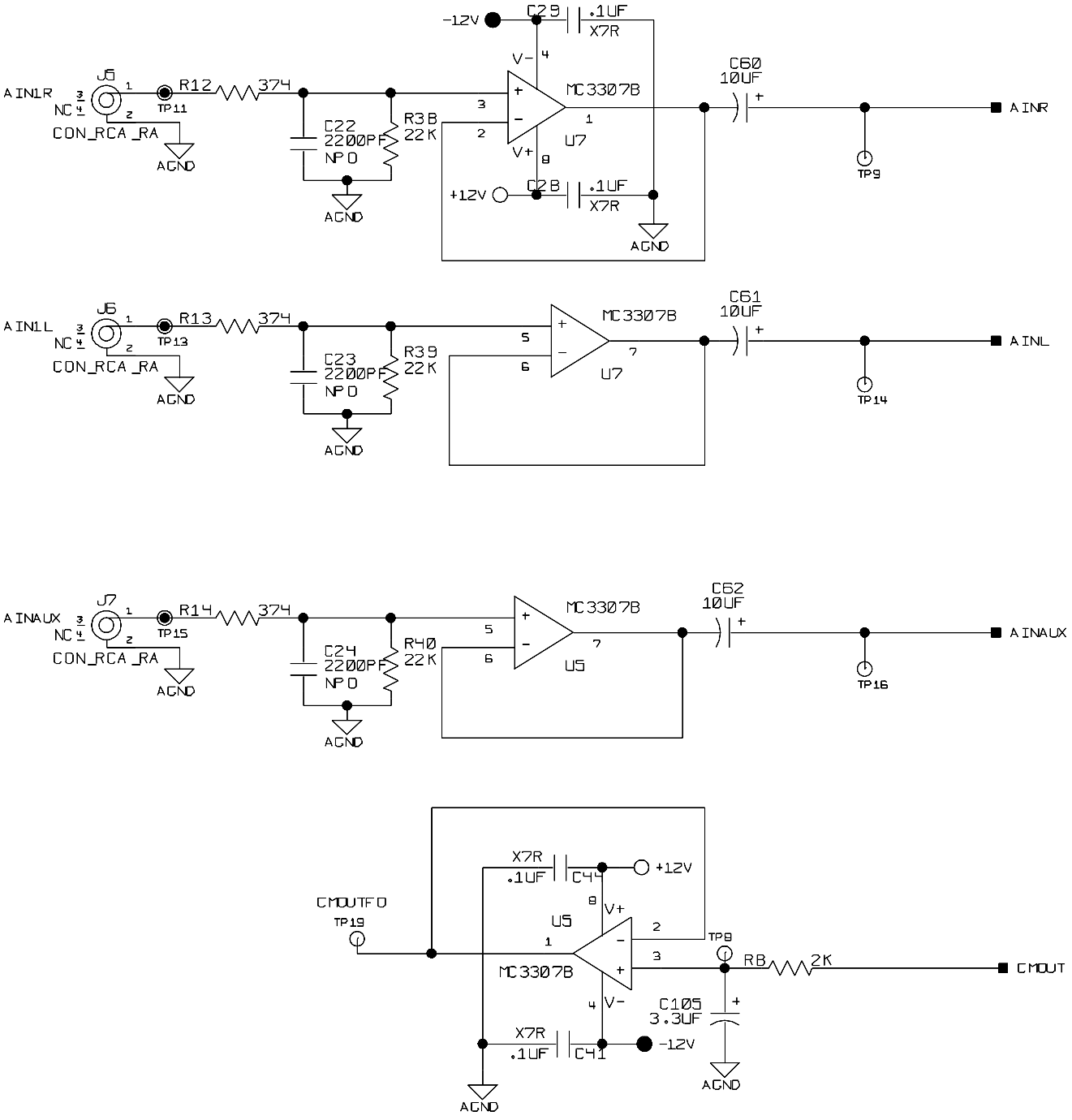


Figure 4. Dedicated Analog Inputs

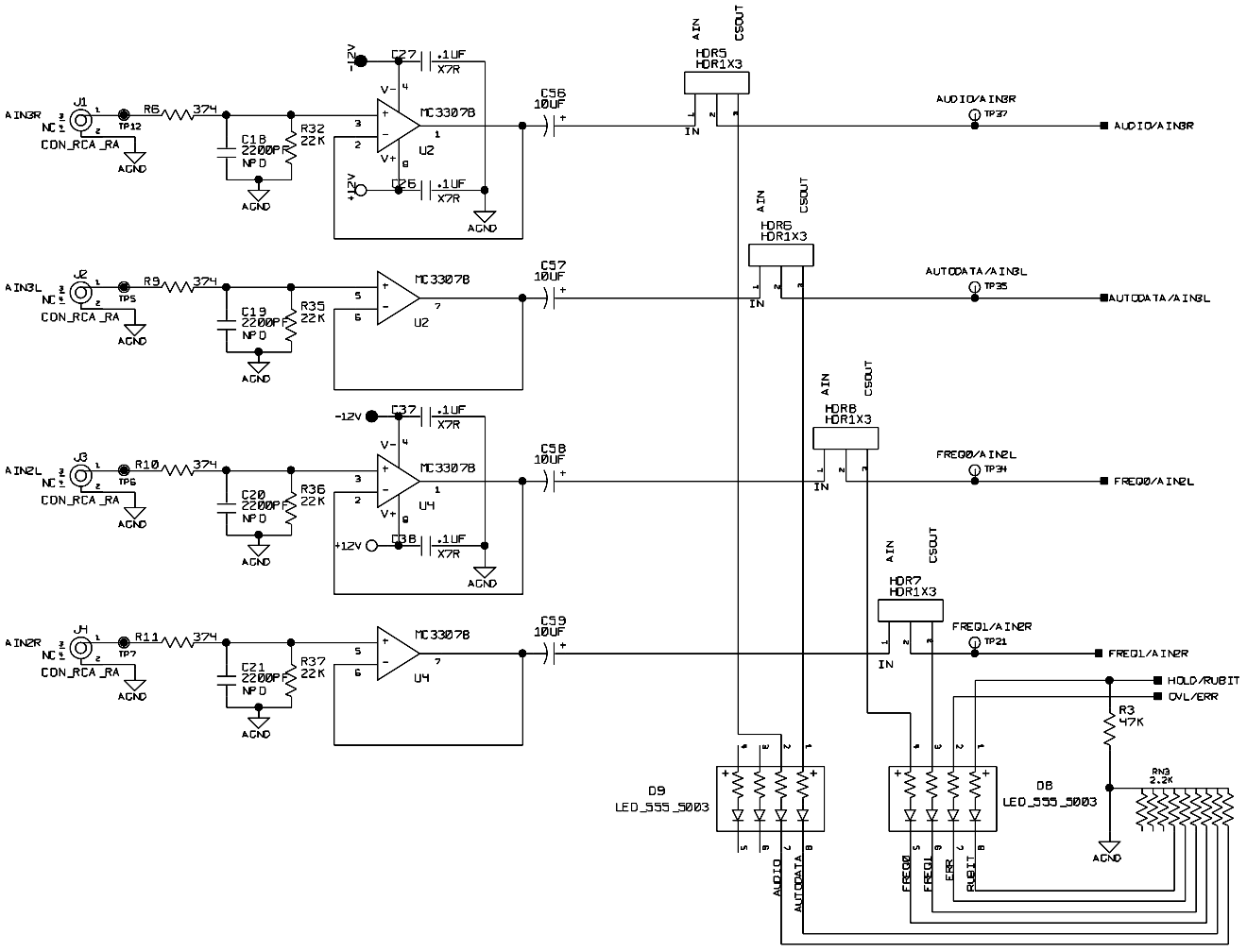


Figure 5. Analog Inputs/Channel Status Outputs with LED Indicators

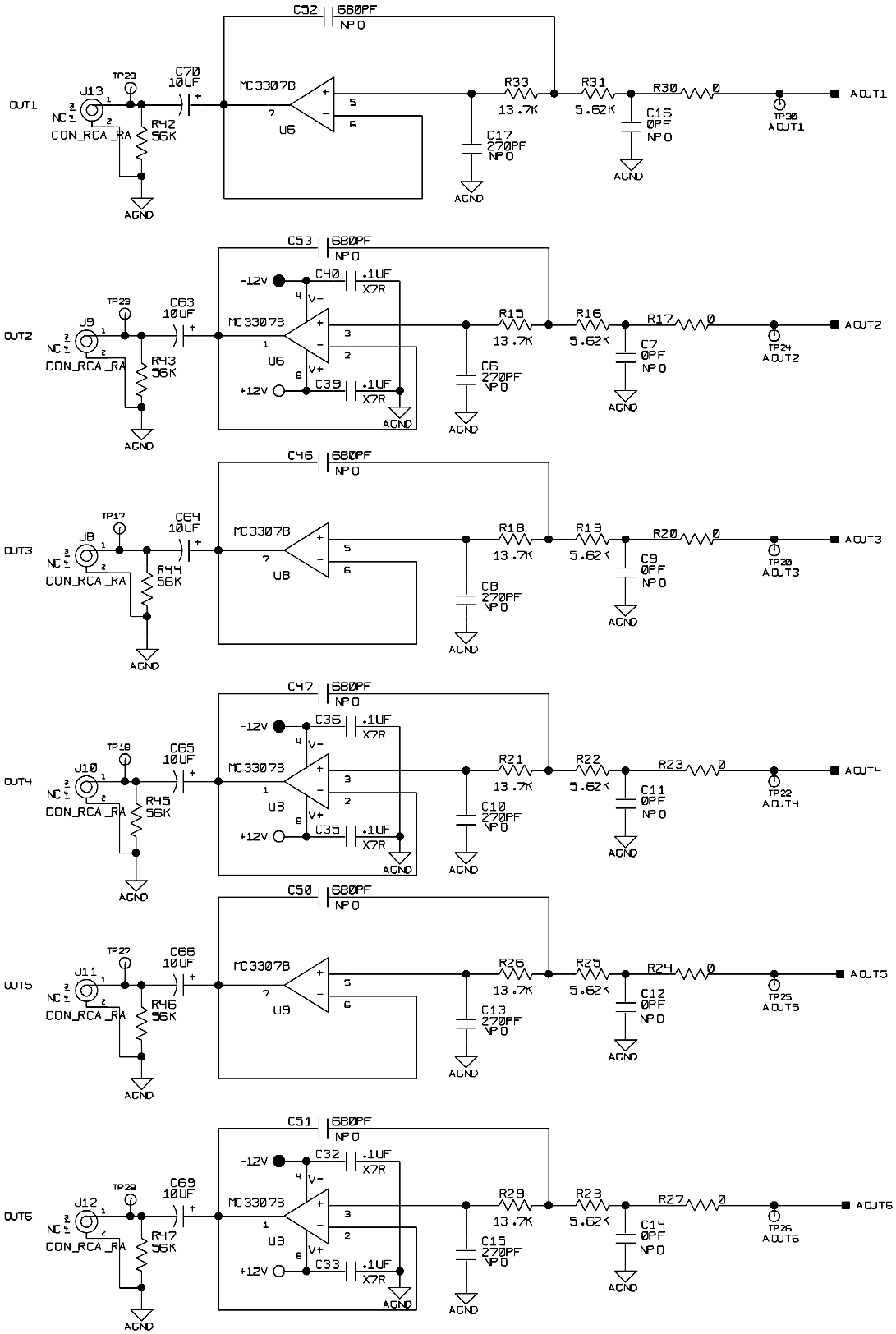


Figure 6. Analog Outputs

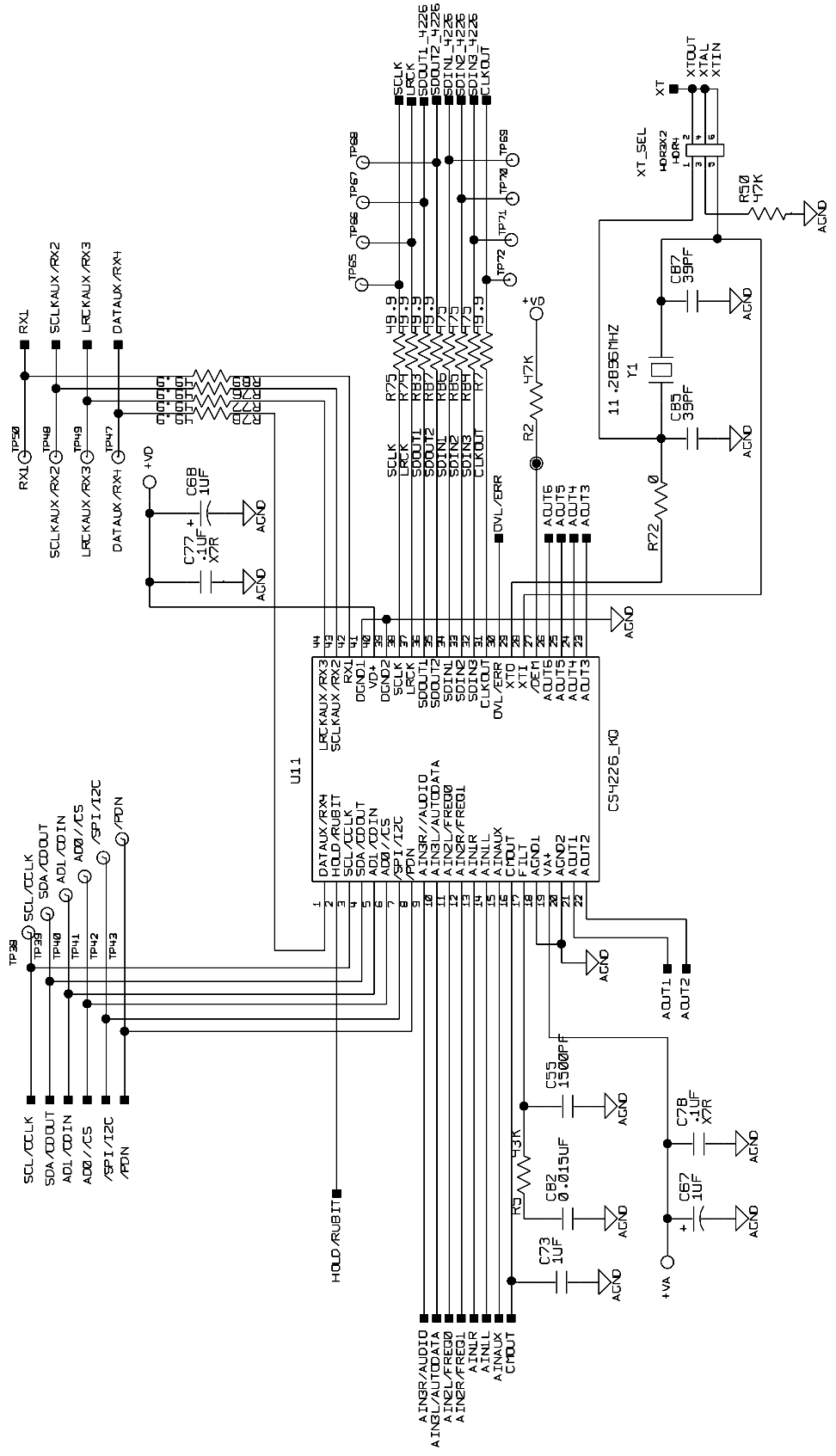


Figure 7. CS4226

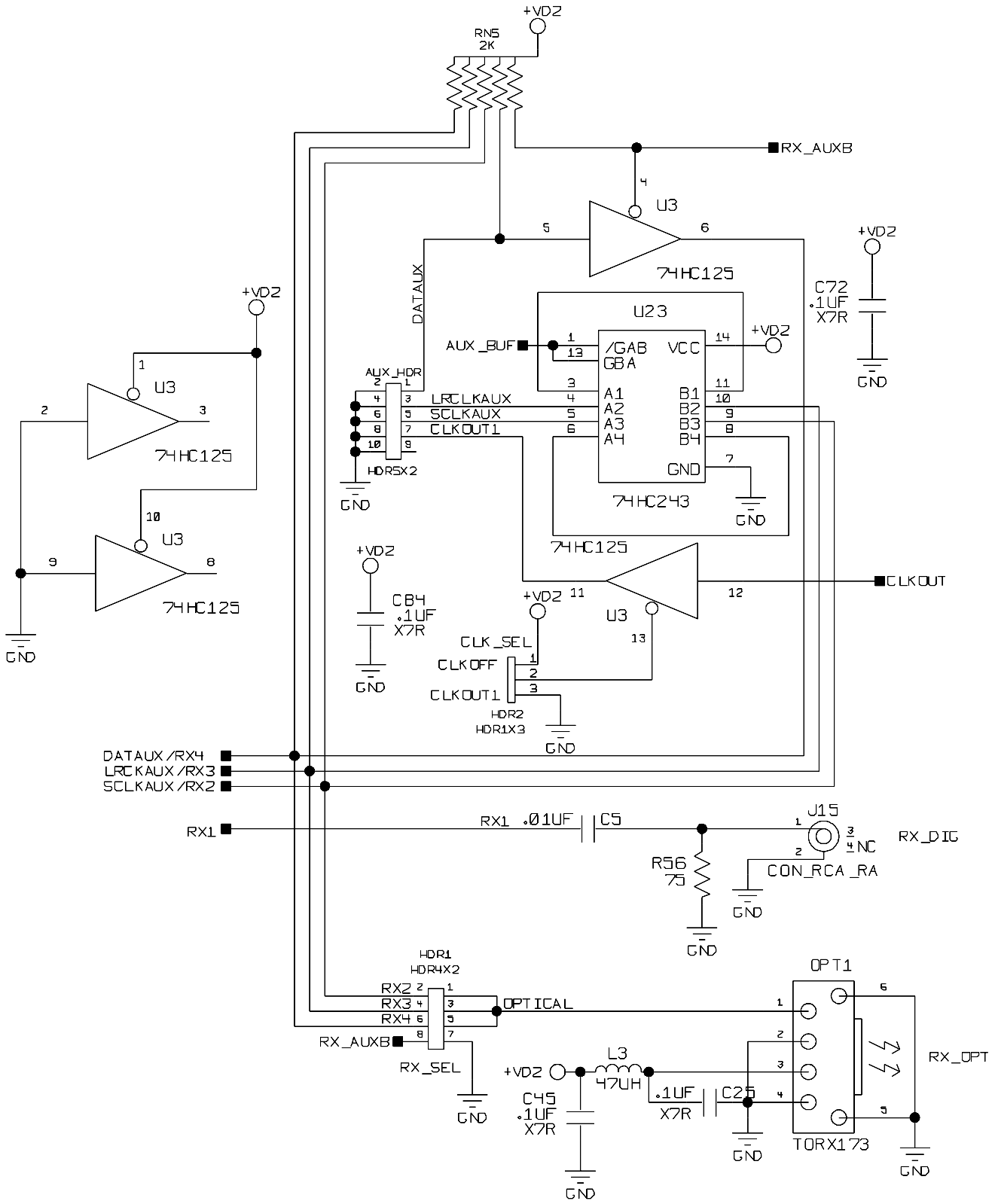


Figure 8. AUX Port and S/PDIF Inputs

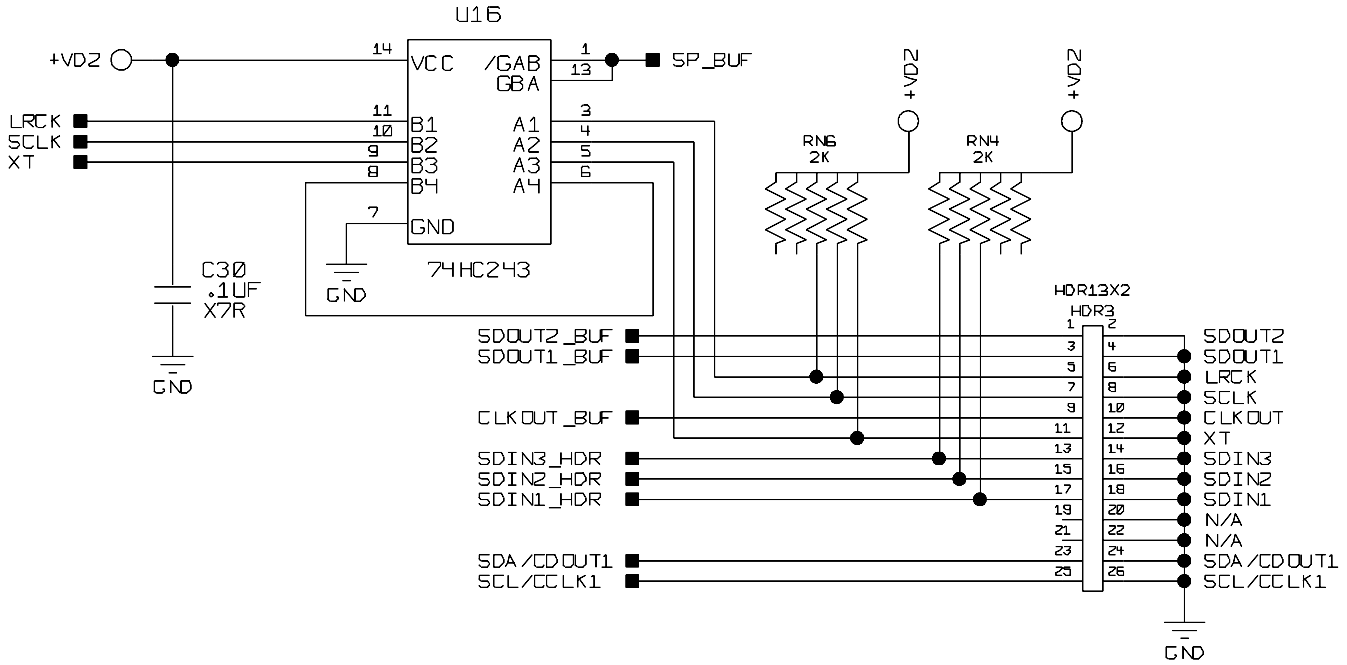


Figure 9. DSP Port

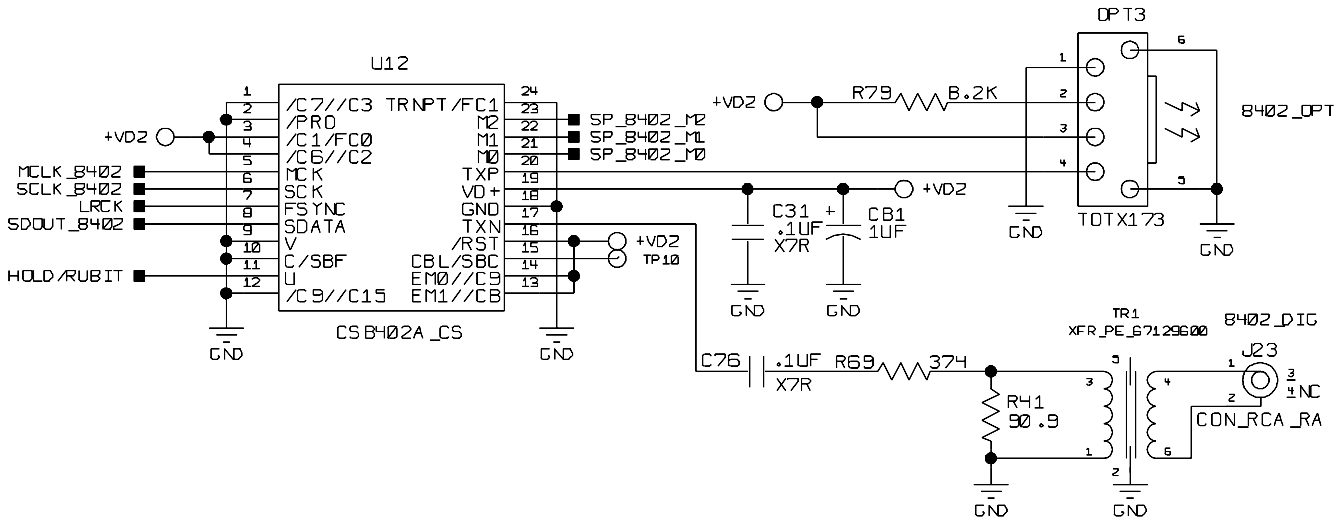


Figure 10. CS8402A Digital Audio Transmitter

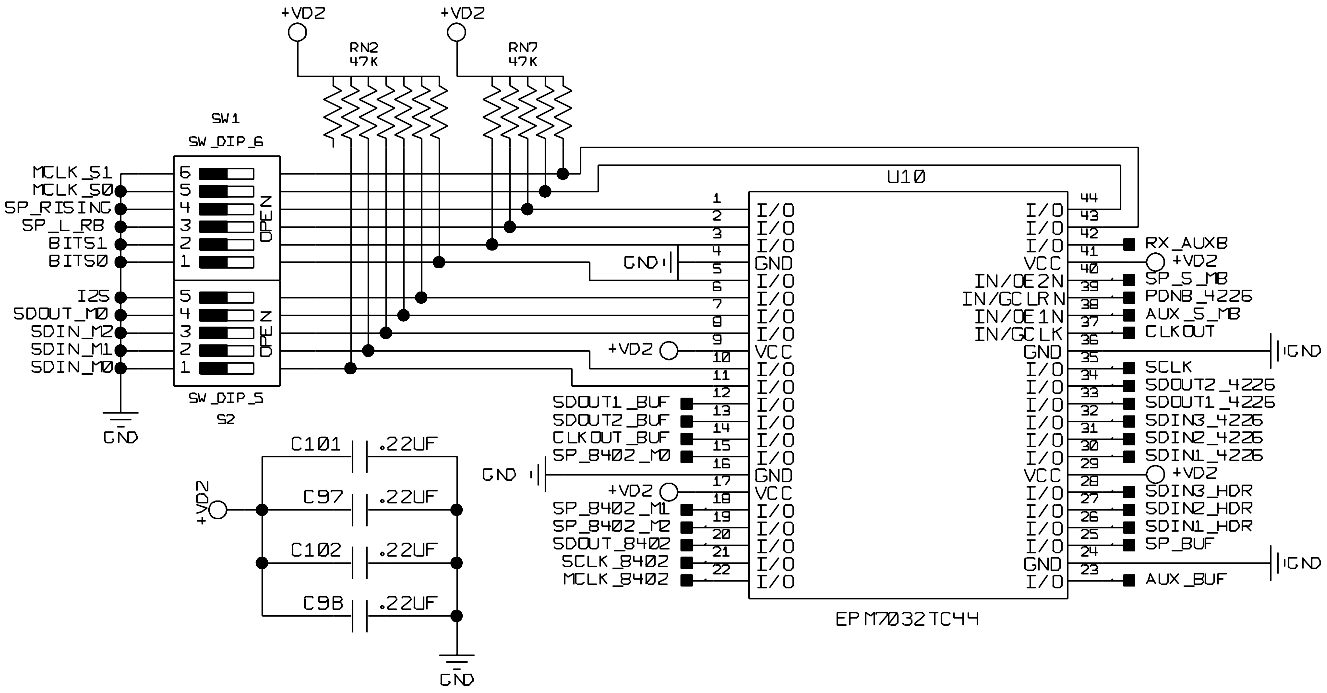


Figure 11. Altera PLD and DIP Switches

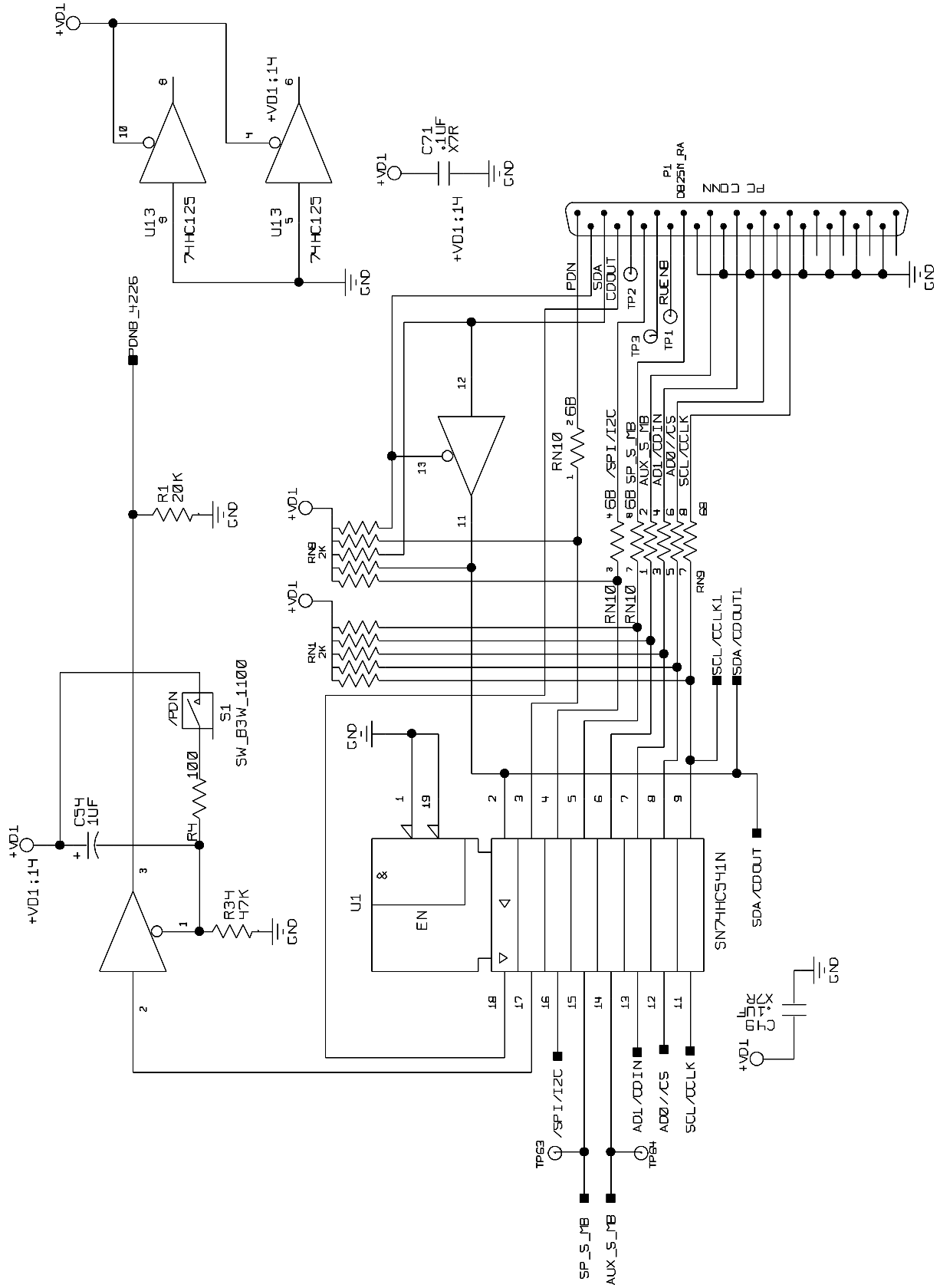


Figure 12. SPI/I²C Control Port Interface

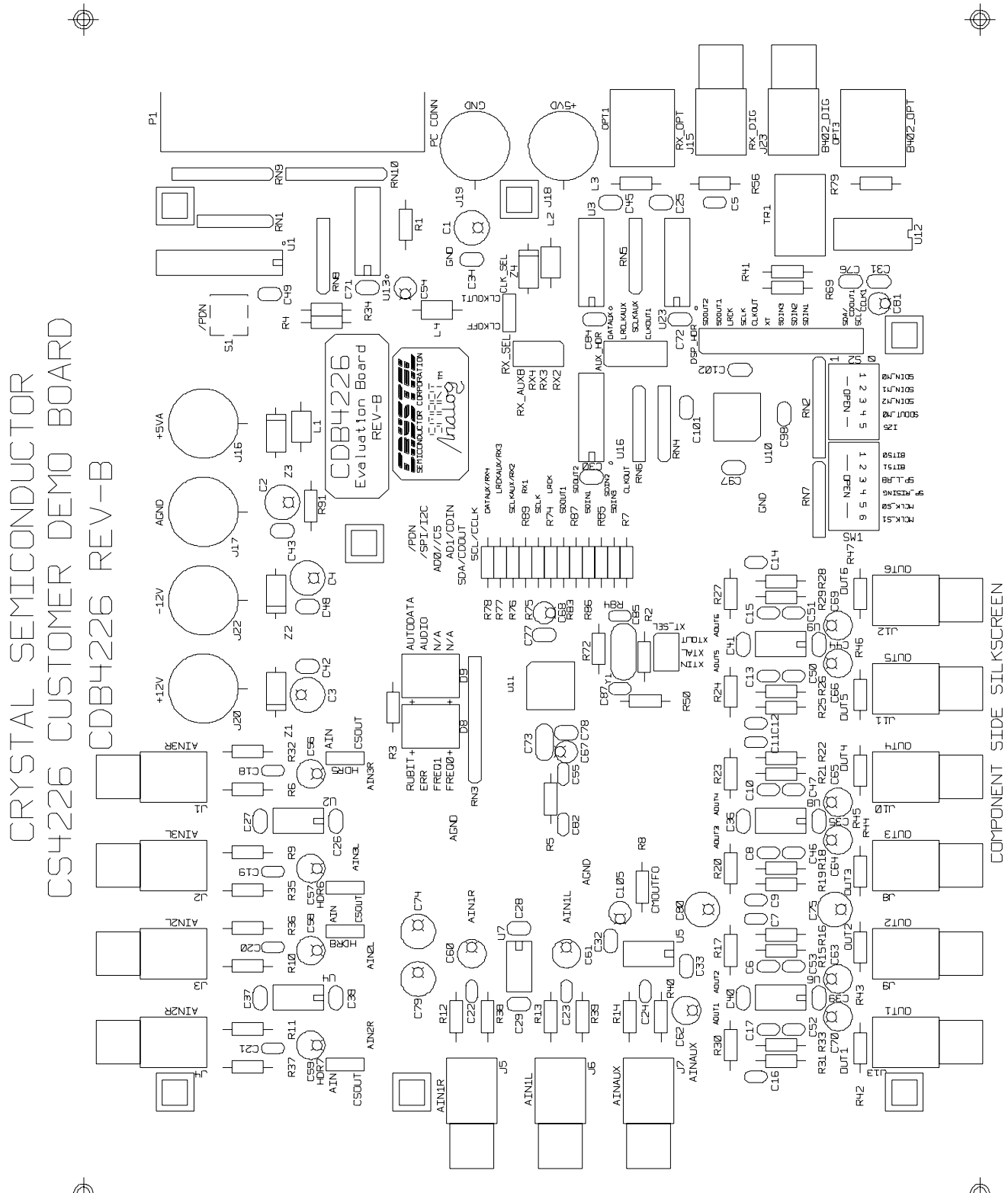


Figure 13. CDB4226 Rev. B Silkscreen (not to scale)

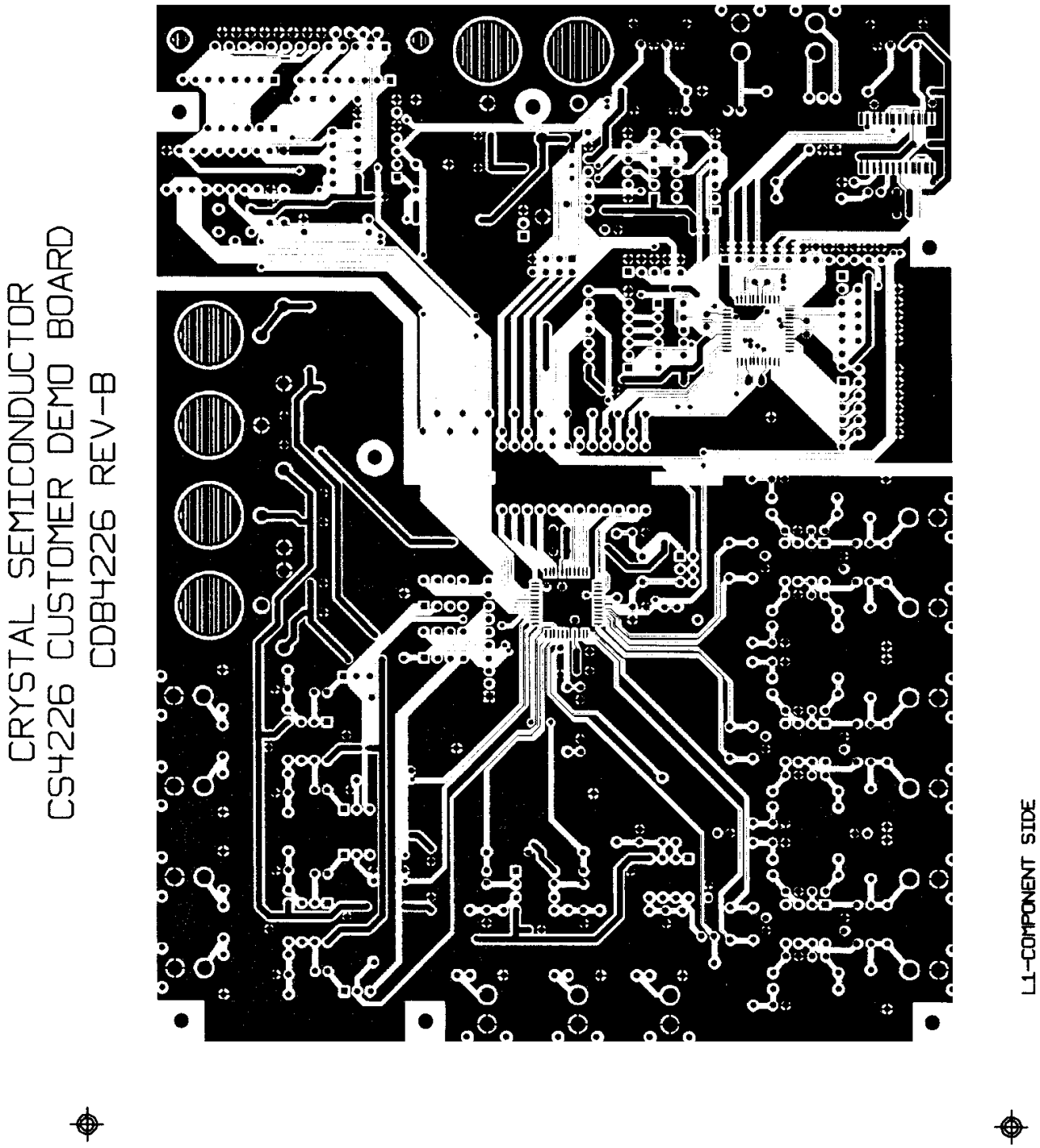


Figure 14. CDB4226 Rev. B Component Side (not to scale)

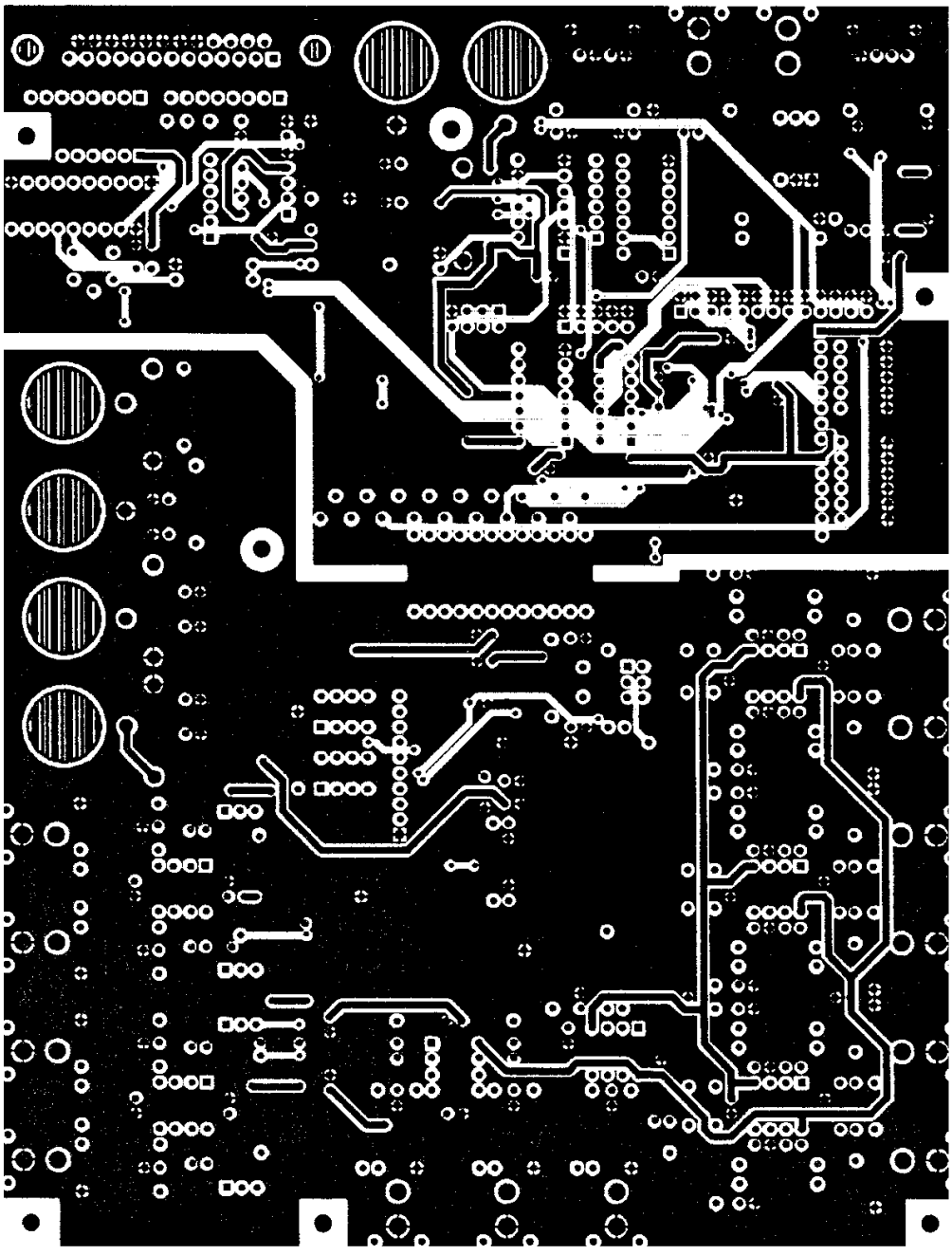


Figure 15. CDB4226 Rev. B Solder Side (not to scale)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