CS4228A

24-Bit, 96 kHz Surround Sound Codec

Features

- Six 24-bit D/A Converters
  - 100 dB dynamic range
  - -90 dB THD+N
- Two 24-bit A/D Converters
  - 97 dB dynamic range
  - -95 dB THD+N
- Sample rates up to 100 kHz
- Pop-free Digital Output Volume Controls
  - 90.5 dB range, 0.5 dB resolution (182 levels)
  - Variable smooth ramp rate, 0.125 dB steps
- Mute Control pin for off-chip muting circuits
- On-chip Anti-alias and Output Filters
- De-emphasis filters for 32, 44.1 and 48 kHz

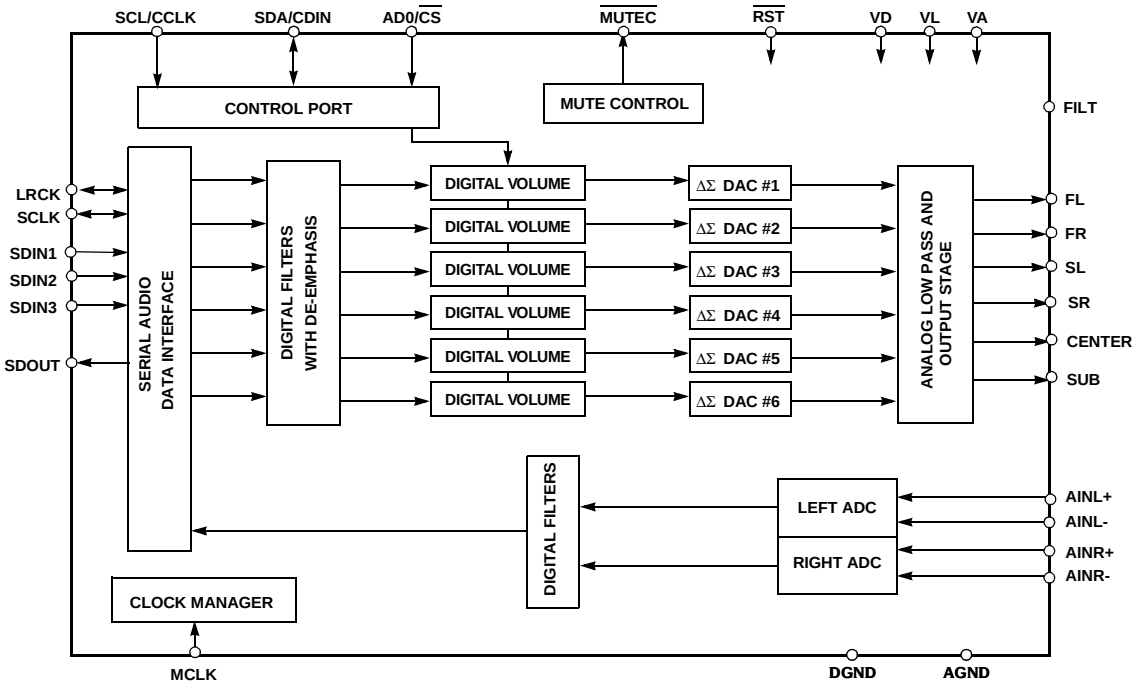
Description

The CS4228A codec provides two analog-to-digital and six digital-to-analog delta-sigma converters, along with volume controls, in a compact 28-pin SSOP device. Combined with an IEC958 (SPDIF) receiver (like the CS8414) and surround sound decoder (such as one of the CS492x or CS493xx families), it is ideal for use in DVD player, A/V receiver and car audio systems supporting multiple standards such as Dolby Digital AC-3, AAC, DTS, Dolby ProLogic, THX, and MPEG.

A flexible serial audio interface allows operation in Left Justified, Right Justified, I^2S, or One Line Data modes.

ORDERING INFORMATION

CS4228A-KS	-10° to +70° C	28-pin SSOP
CDB4228A		Evaluation Board



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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1. CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS

(Unless otherwise specified T_A = 25° C; VA = VD = VL = +5 V; Full Scale Input Sine wave, 984.375 Hz; Fs = 48 kHz BRM, 96 kHz HRM; Measurement Bandwidth is 20 Hz to 20 kHz; Local components as shown in Figure 5; SPI control mode, Left Justified serial format, MCLK = 256 x Fs for BRM, 128 x Fs for HRM, SCLK = 64 x Fs)

Parameter	Symbol	Base Rate Mode			High Rate Mode			Units
		Min	Typ	Max	Min	Typ	Max	
Analog Input Characteristics - Minimum gain setting (0 dB) Differential Input; unless otherwise specified.								
Dynamic Range, -60 dBFS input (A weighted) (unweighted)		90	97 94	-	90	97 94	-	dB dB
Total Harmonic Distortion + Noise (Note 1)	THD+N	-	-95	-88	-	-95	-88	dB
Interchannel Isolation		-	100	-	-	100	-	dB
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Offset Error (with high pass filter)		-	-	0	-	-	0	LSB
Full Scale Input Voltage (Differential):		5.24	5.66	6.09	5.24	5.66	6.09	Vp-p
Gain Drift		-	100	-	-	100	-	ppm/°C
Input Resistance		10	-	-	10	-	-	kΩ
Input Capacitance		-	-	15	-	-	15	pF
A/D Decimation Filter Characteristics (Note 2)								
Passband (Note 3)		0.022	-	21.77	0.022	-	43.54	kHz
Passband Ripple		-	-	0.01	-	-	0.05	dB
Stopband (Note 3)		30.0	-	6114	72.41	-	6071	kHz
Stopband Attenuation (Note 4)		80	-	-	45	-	-	dB
Group Delay	t_{gd}	-	TBD	-	-	TBD	-	s
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0	-	-	0	µs
High Pass Filter Characteristics (Note 2)								
Frequency Response: -3 dB (Note 5) -0.13 dB		- -	3.4 20	- -	- -	3.4 20	- -	Hz Hz
Phase Deviation @ 20 Hz (Note 5)		-	10	-	-	10	-	Degree
Passband Ripple		-	-	0	-	-	0	dB

Notes:
1. Referenced to typical full-scale differential input voltage (2 Vrms), Tested with -1 dBFS input.
2. Filter response is not tested but is guaranteed by design.
3. Filter characteristics scale with output sample rate.
4. The analog modulator samples the input at 128 times Fs. For example, input the sample rate is 6.144 MHz for an output sample rate of 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency (n × 6.144 MHz ±20.0 kHz where n = 0,1,2,3...).
5. High Pass Filter characteristics are specified for Fs=44.1 KHz.

Specifications are subject to change without notice

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	Base Rate Mode Min	Base Rate Mode Typ	Base Rate Mode Max	High Rate Mode Min	High Rate Mode Typ	High Rate Mode Max	Units
Analog Output Characteristics - Minimum Attenuation, 10 kΩ, 10 pF load; unless otherwise specified.								
Dynamic Range, -60 dBFS input (A weighted)		93	100	-	93	100	-	dB
(unweighted)		-	97	-	-	97	-	dB
Total Harmonic Distortion + Noise	THD+N	-	-90	-83	-	-90	-83	dB
Interchannel Isolation		-	95	-	-	95	-	dB
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Offset Voltage		-	10	-	-	10	-	mV
Full Scale Output Voltage		3.42	3.7	3.98	3.42	3.7	3.98	Vp-p
Gain Drift		-	100	-	-	100	-	ppm/°C
Analog Output Load								
Minimum Load Resistance:		-	10	-	-	10	-	kΩ
Maximum Load Capacitance:		-	100	-	-	100	-	pF
Combined Digital and Analog Filter Characteristics (Note 2)								
Frequency Response 10 Hz to 20 kHz			±0.1			±0.1		dB
Deviation from Linear Phase		-	±0.5	-	-	±0.5	-	Degrees
Passband: to 0.01 dB corner (Notes 6, 7)		0	-	21.77	0	-	43.54	kHz
Passband Ripple (Note 7)		-	-	±0.01	-	-	±0.01	dB
Stopband (Notes 6, 7)		26.2	-	-	62.5	-	-	kHz
Stopband Attenuation (Notes 5, 8)		70	-	-	65	-	-	dB
Group Delay (Fs = Input Word Rate)	tgd	-	27/Fs	-	-	TBD	-	s
Analog Loopback Performance								
Signal-to-noise Ratio (CCIR-2K weighted, -20 dB FS input)	CCIR-2K	-	90	-	-	90	-	dB

Notes: 6. The passband and stopband edges scale with frequency. For input word rates, Fs, other than 44.1 kHz, the 0.01 dB passband edge is 0.4535×Fs and the stopband edge is 0.5465×Fs.

7. Digital filter characteristics.

8. Measurement bandwidth is 10 Hz to 3 Fs.

Specifications are subject to change without notice

ANALOG CHARACTERISTICS (Continued)

Power Supply	Symbol	Base Rate Mode Min	Base Rate Mode Typ	Base Rate Mode Max	High Rate Mode Min	High Rate Mode Typ	High Rate Mode Max	Units
Power Supply Current Operating								
VA = VD = VL = 5 V VA		-	37	42	-	37	42	mA
VL		-	0.5	2	-	0.5	2	mA
VD		-	85	99	-	85	99	mA
Power Down: $\overline{RST}$ low, Clocks running								
VA		-	0.5	1	-	0.5	1	mA
VL		-	0.2	0.5	-	0.2	0.5	mA
VD		-	0.5	1	-	0.5	1	mA
Power Supply Rejection (1 kHz, 10 mV_{rms})		-	50	-		50		dB

DIGITAL CHARACTERISTICS Unless otherwise specified (T_A = 25 °C; VA = VD + 5V,VL = 2.375 to 5.25V)

Parameter	Symbol	Min	Max	Units
High-level Input Voltage	V_{IH}	0.7xVL	-	V
Low-level Input Voltage	V_{IL}		0.3xVL	V
High-level Output Voltage at VL = 5 V				
I_0 = -2.0 mA	V_{OH}	VL - 1.0	-	V
I_0 = -100 uA		VL - 0.7	-	V
VL = 2.5 V				
I_0 = -2.0 mA		0.9 X VL	-	V
Low-level Output Voltage at VL = 5 V				
I_0 = 2.0 mA	V_{OL}	-	0.4	V
I_0 = 100 uA		-	0.2	V
VL = 2.5 V				
I_0 = -2.0 mA		-	0.4	V
Input Leakage Current (Digital Inputs)		-	10	µA
Output Leakage Current (High-Impedance Digital Outputs)		-	10	µA

SWITCHING CHARACTERISTICS (T_A = 25°C; VA = VD + 5V,VL = 2.375 to 5.25V, C_L 30 pF)

Parameter	Symbol	Min	Typ	Max	Units
Audio ADC's and DAC's Sample Rate BRM	Fs	30	-	50	kHz
HRM		60	-	100	kHz
MCLK Frequency		3.84	-	25.6	MHz
MCLK Duty Cycle BRM					
MCLK =128, 384 Fs		TBD	50	TBD	%
MCLK = 256, 512 Fs		40	50	60	%
HRM					
MCLK = 64, 192 Fs		TBD	50	TBD	%
MCLK = 128, 256 Fs		40	50	60	%

SWITCHING CHARACTERISTICS (Continued)

Parameter		Symbol	Min	Typ	Max	Units
$\overline{\text{RST}}$ Low Time	(Note 9)		1	-	-	ms
SCLK Falling Edge to SDOUT Output Valid	(DSCK=0)	t_{dpd}		-	50	ns
LRCK Edge to MSB Valid		t_{lrpd}		-	20	ns
SDIN Setup Time Before SCLK Rising Edge		t_{ds}		-	10	ns
SDIN Hold Time After SCLK Rising Edge		t_{dh}		-	30	ns
Master Mode						
SCLK Falling to LRCK Edge		t_{mslr}		$\pm$10	-	ns
SCLK Duty Cycle				50	-	%
Slave Mode						
SCLK Period		t_{sckw}		-	-	ns
SCLK High Time		t_{sckh}	50	-	-	ns
SCLK Low Time		t_{sckl}	50	-	-	ns
SCLK rising to LRCK Edge	(DSCK=0)	t_{lrckd}	25	-	-	ns
LRCK Edge to SCLK Rising	(DSCK=0)	t_{lrcks}	25	-	-	ns

Notes: 9. After powering up the CS4228A, $\overline{\text{RST}}$ should be held low until the power supplies and clocks are settled.

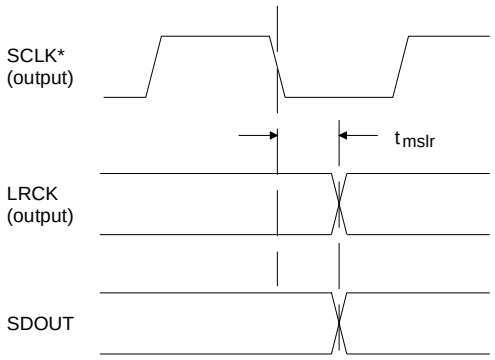
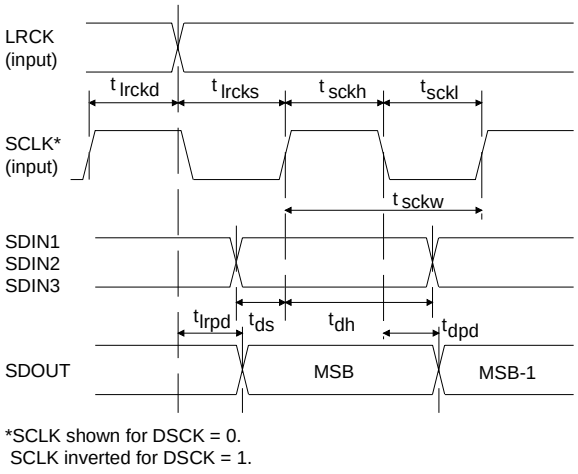


Figure 1. Serial Audio Port Master Mode Timing



*SCLK shown for DSCK = 0.
SCLK inverted for DSCK = 1.

Figure 2. Serial Audio Port Slave Mode Timing

SWITCHING CHARACTERISTICS - CONTROL PORT (TA = 25° C, VA = VD = +5 V, VL =2.375 to 5.25 V; Inputs: logic 0 = DGND, logic 1 = VL, C_L = 30 pF)

Parameter		Symbol	Min	Max	Units
SPI Mode (SDOUT > 47 kΩ to GND)					
CCLK Clock Frequency		f_{sck}	-	6	MHz
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0		µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20		ns
CCLK Low Time		t_{scl}	66		ns
CCLK High Time		t_{sch}	66		ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40		ns
CCLK Rising to DATA Hold Time	(Note 10)	t_{dh}	15		ns
Rise Time of CCLK and CDIN	(Note 11)	t_{r2}		100	ns
Fall Time of CCLK and CDIN	(Note 11)	t_{f2}		100	ns

Notes: 10. Data must be held for sufficient time to bridge the transition time of CCLK.

11. For F_{SCK} < 1 MHz

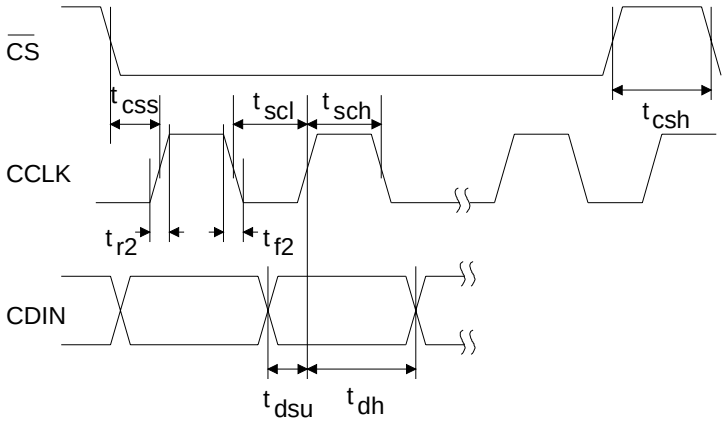


Figure 3. SPI Control Port Timing

SWITCHING CHARACTERISTICS - CONTROL PORT (T_A = 25° C; VA = VD = +5 V, VL=2.375 to 5.25 V; Inputs: logic 0 = DGND, logic 1 = VL, C_L = 30 pF)

Parameter	Symbol	Min	Max	Units
Two Wire Mode (SDOUT < 47 kΩ to ground)				
SCL Clock Frequency	f_{scl}	-	100	kHz
Bus Free Time Between Transmissions	t_{buf}	4.7		µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0		µs
Clock Low Time	t_{low}	4.7		µs
Clock High Time	t_{high}	4.0		µs
Setup Time for Repeated Start Condition	t_{sust}	4.7		µs
SDA Hold Time from SCL Falling (Note 12)	t_{hdd}	0		µs
SDA Setup Time to SCL Rising	t_{sud}	250		ns
Rise Time of Both SDA and SCL Lines	t_r		1	µs
Fall Time of Both SDA and SCL Lines	t_f		300	ns
Setup Time for Stop Condition	t_{susp}	4.7		µs

Notes: 12. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

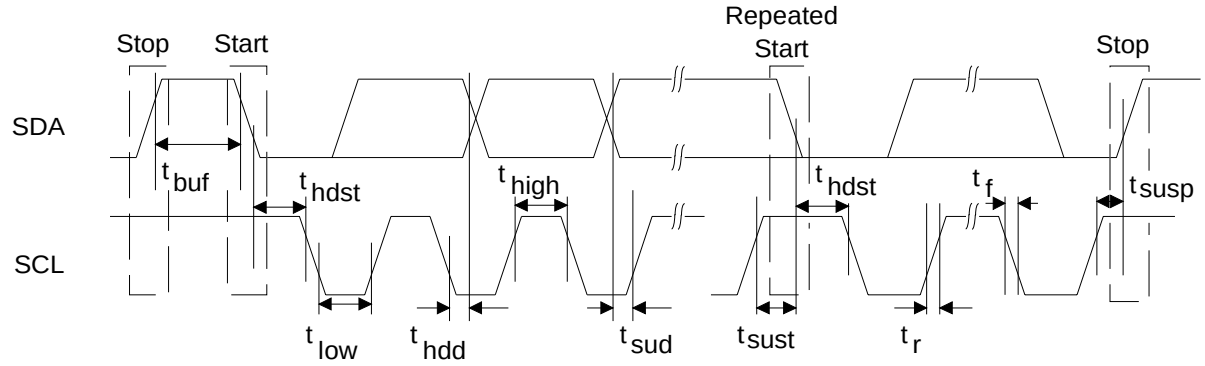


Figure 4. Two Wire Control Port Timing

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies	Digital	VD	-0.3	-	6.0	V
	Analog	VA	-0.3	-	6.0	V
	Interface	VL	-0.3	-	6.0	V
Input Current	(Note 13)		-	-	±10	mA
Analog Input Voltage	(Note 14)		-0.7	-	VA + 0.7	V
Digital Input Voltage	Input Pins		-0.7	-	VL + 2.5	V
	Bidirectional Pins		-0.7	-	VL + 0.7	V
	(Notes 14 and 15)					V
Ambient Temperature	(Power Applied)		-55	-	+125	°C
Storage Temperature			-65	-	+150	°C

Notes: 13. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

14. The maximum over or under voltage is limited by the input current.

15. Bidirectional pins configured as inputs.

Warning: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies	Digital	VD	4.75	5.0	5.25	V
	Analog	VA	4.75	5.0	5.25	V
	Interface	VL	2.375	-	5.25	V
Operating Ambient Temperature		T_A	-10	25	70	°C

2. TYPICAL CONNECTION DIAGRAM

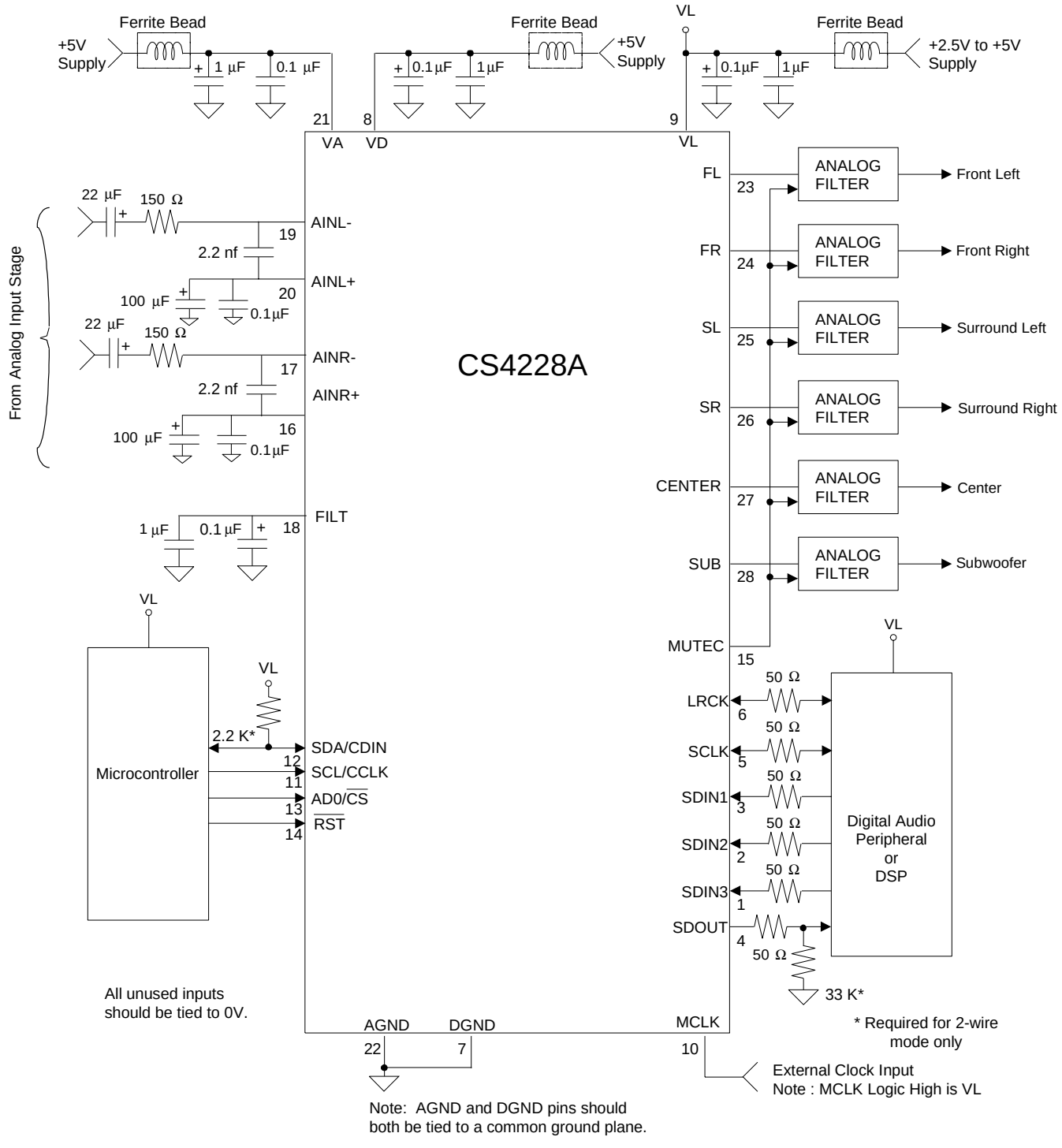


Figure 5. Recommended Connection Diagram

3. FUNCTIONAL DESCRIPTION

3.1 Overview

The CS4228A is a 24-bit audio codec comprised of 2 analog-to-digital converters (ADC) and 6 digital-to-analog converters (DAC), all implemented using single-bit delta-sigma techniques. Other functions integrated with the codec include independent digital volume controls for each DAC, digital DAC de-emphasis filters, ADC high-pass filters, an on-chip voltage reference, and a flexible serial audio interface. All functions are configured through a serial control port operable in SPI mode and in two wire mode. Figure 5 shows the recommended connections for the CS4228A.

3.2 Analog Inputs

3.2.1 Line Level Inputs

AINR+, AINR-, AINL+, and AINL- are the line level analog inputs (See Figure 5). These pins are internally biased to a DC operating voltage of approximately 2.3 VDC. AC coupling the inputs preserves this bias and minimizes signal distortion. Figure 5 shows operation with a single-ended input source. This source may be supplied to either the positive or negative input as long as the unused input is connected to ground through capacitors as shown. When operated with single-ended inputs, distortion will increase at input levels higher than -1 dBFS. Figure 6 shows an example of a differential input circuit.

Muting of the stereo ADC is possible through the ADC Control Byte.

The ADC output data is in 2's complement binary format. For inputs above positive full scale or below negative full scale, the ADC will output 7FFFFFH or 800000H, respectively.

3.2.2 High Pass Filter

Digital high pass filters in the signal path after the ADCs remove any DC offsts present on the analog inputs. The high pass filter helps prevent audible "clicks" when switching between audio sources downstream from the ADCs. The high pass filter response, given in "High Pass Filter Characteristics (Note 2)", scales linearly with sample rate. Thus, for High Rate Mode, the -3 dB frequency at a 96 kHz sample rate will be equal to 96/44.1 times that at a sample rate of 44.1 kHz.

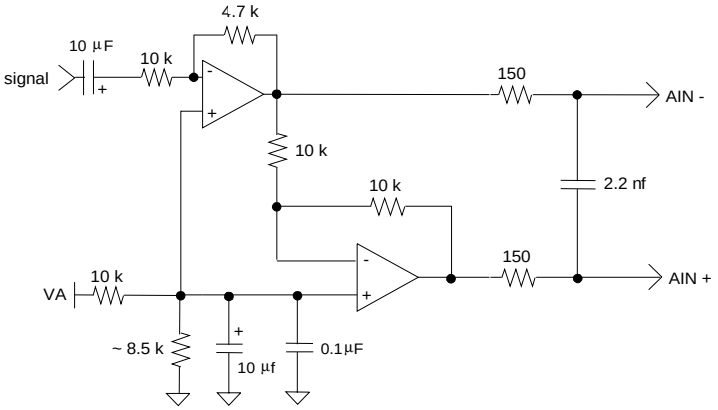


Figure 6. Optional Line Input Buffer

The high pass filters can be disabled by setting the HPF bit in the ADC Control register. When asserted, any DC present at the analog inputs will be represented in the ADC outputs. The high pass filter may also be "frozen" using the HPFZ bit in the ADC Control register. In this condition, it will remember the DC offset present at the ADC inputs at the moment the HPFZ bit was asserted, and will continue to remove this DC level from the ADC outputs. This is useful in cases where it is desirable to eliminate a fixed DC offset while still maintaining full frequency response down to DC.

3.3 Analog Outputs

3.3.1 Line Level Outputs

The CS4228A contains on-chip buffer amplifiers capable of producing line level outputs. These amplifiers are biased to a quiescent DC level of approximately 2.3 V. This bias, as well as variations in offset voltage, are removed using off-chip AC load coupling.

The delta-sigma conversion process produces high frequency noise beyond the audio passband, most of which is removed by the on-chip analog filters. The remaining out-of-band noise can be attenuated using an off-chip low pass filter. For most applications, a simple passive filter as show in Figure 7 can be used. Note that this circuit also serves to block the DC present at the outputs. Figure 8 gives an example of a filter which can be used in applications where greater out of band attenuation is desired. The 2-pole Butterworth filter has a -3 dB frequency of 50 kHz, a passband attenuation of 0.1 dB at 20 kHz providing optimal out-of-band filtering for sample rates from 44.1 kHz to 96 kHz. The filter has and a gain of 1.56 providing a 2 Vrms output signal.

3.3.2 Digital Volume Control

Each DAC's output level is controlled via the Digital Volume Control register operating over the range of 0 to 90.5 dB attenuation with 0.5 dB resolution. Volume control changes do not occur instantaneously. Instead they ramp in increments of 0.125 dB at a variable rate controlled by the RMP1:0 bits in the Digital Volume Control register.

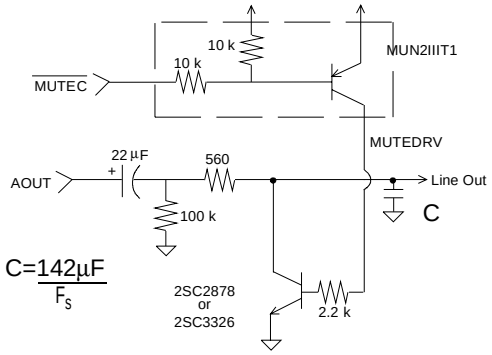


Figure 7. Passive Output Filter with Mute

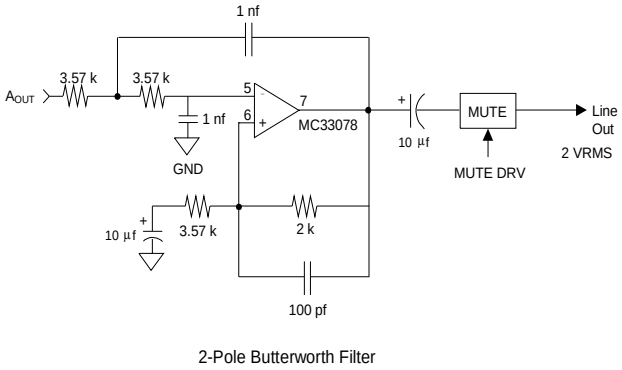


Figure 8. Butterworth Output Filter with Mute

Each output can be independently muted via mute control bits MUT6-1 in the DAC Mute1 Control register. When asserted, MUT attenuates the corresponding DAC to its maximum value (90.5 dB). When MUT is deasserted, the corresponding DAC returns to the attenuation level set in the Digital Volume Control register. The attenuation is ramped up and down at the rate specified by the RMP1:0 bits.

To achieve complete digital attenuation of an incoming signal, Hard Mute controls are provided. When asserted, Hard Mute will send zero data to a corresponding pair of DACs. Hard Mute is not ramped, so it should only be asserted after setting the two corresponding MUT bits to prevent high frequency transients from appearing on the DAC outputs. Hard Mute is controlled by the HMUTE56/34/12 bits in the DAC Mute2 Control register.

3.4 Mute Control

The Mute Control pin is typically connected to an external mute control circuit as shown in Figure 7 and Figure 8. The Mute Control pin is asserted during power up, power down, and when serial port clock errors are present. The pin can also be controlled by the user via the control port, or automatically asserted when zero data is present on all six DAC inputs. To prevent large transients on the output, it is desirable to mute the DAC outputs before the Mute Control pin is asserted. Please see the $\overline{\text{MUTEC}}$ pin in the Pin Descriptions section for more information.

3.5 Clock Generation

The master clock, MCLK, is supplied to the CS4228A from an external clock source. If MCLK stops for 10 µs, the CS4228A will enter Power Down Mode in which the supply current is reduced as specified under “Power Supply”. In all modes it is required that the number of MCLK periods per SCLK and LRCK period be constant.

3.5.1 Clock Source

The CS4228A internal logic requires an external master clock, MCLK, that operates at multiples of the sample rate frequency, Fs. The MCLK/Fs ratio is determined by the CI1:0 bits in the CODEC Clock Mode register.

3.5.2 Synchronization

The serial port is internally synchronized with MCLK. If from one LRCK cycle to the next, the number of MCLK cycles per LRCK cycle changes by more than 32, the CS4228A will undergo an internal reset of its data paths in an attempt to resynchronize. Consequently, it is advisable to mute the DACs and clear the $\overline{\text{DIGPDN}}$ bit when changing from one clock source to another to avoid the output of undesirable audio signals as the device resynchronizes. It is adviseable to ensure that MCLK complies with the Switching Characteristics at all times when switching clock sources without resetting the part.

3.6 Digital Interfaces

3.6.1 Serial Audio Interface Signals

The serial audio data is presented in 2's complement binary form with the MSB first in all formats. The serial interface clock, SCLK, is used for both transmitting and receiving audio data. SCLK can be generated by the CS4228A (master mode) or it can be input from an external source (slave mode). Mode selection is made with the DMS1:0 bits in the Serial Port Mode register. The number of SCLK cycles in one sample period can be set using the DCK1:0 bits as detailed in the Serial Port Mode register.

The Left/Right clock (LRCK) is used to indicate left and right data frames and the start of a new sample period. It may be an output of the CS4228A (master mode), or it may be generated by an external source (slave mode). The frequency of LRCK is the same as the system sample rate, Fs.

SDIN1, SDIN2, and SDIN3 are the data input pins. SDOUT, the data output pin, carries data from the two 24-bit ADC's. The serial audio port may also be operated in One Line Data Mode in which all 6 channels of DAC data is input on SDIN1 and the stereo ADC data is output on SDOUT. Table 1 outlines the serial port input to DAC channel allocations.

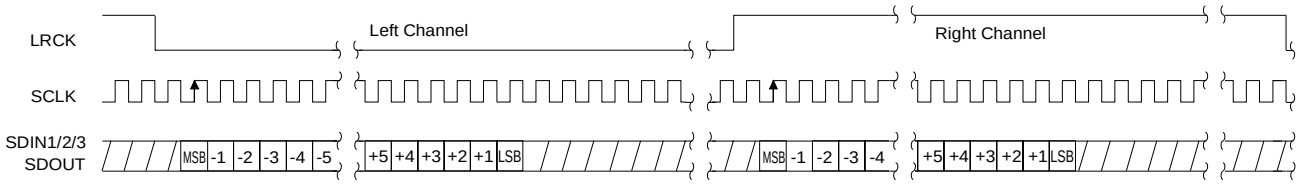
DAC Inputs		
SDIN1	left channel right channel single line	DAC #1 DAC #2 All 6 DAC channels (BRM)
SDIN2	left channel right channel	DAC #3 DAC #4
SDIN3	left channel right channel	DAC #5 DAC #6

Table 1. Serial Audio Port Input Channel Allocations

3.6.2 Serial Audio Interface Formats

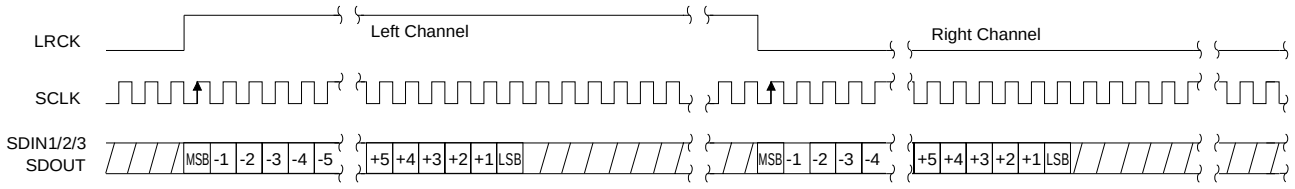
The digital audio port supports 6 formats, shown in Figures 9, 10, 11 and 12. These formats are selected using the DDF2:0 bits in the Serial Port Mode register.

In One Line Data Mode, all 6 DAC channels are input on SDIN1. One Line Data Mode is only available in BRM. See Figure 12 for channel allocations.



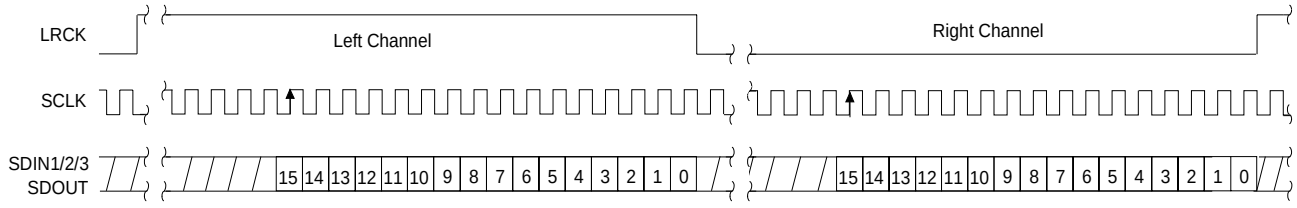
I2S Mode, Data Valid on Rising Edge of SCLK		
Bits/Sample	SCLK Rate(s)	Notes
16	32, 48, 64, 128 Fs 32, 64 Fs	BRM, 48 Fs available in slave mode only HRM
18 to 24	48, 64, 128 Fs 64 Fs	BRM, 48 Fs available in slave mode only HRM

Figure 9. I^2S Serial Audio Formats



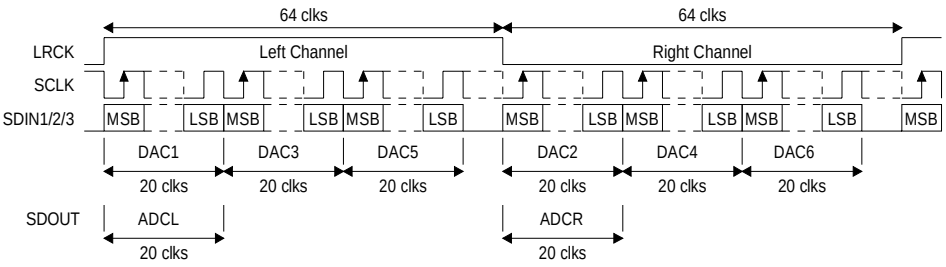
Left Justified Mode, Data Valid on Rising Edge of SCLK		
Bits/Sample	SCLK Rate(s)	Notes
16	32, 48, 64, 128 Fs 32, 64 Fs	BRM, 48 Fs available in slave mode only HRM
18 to 24	48, 64, 128 Fs 64 Fs	BRM, 48 Fs available in slave mode only HRM

Figure 10. Left Justified Serial Audio Formats



Right Justified Mode, Data Valid on Rising Edge of SCLK		
Bits/Sample	SCLK Rate(s)	Notes
16	32, 48, 64, 128 Fs 32, 64 Fs	BRM, 48 Fs available in slave mode only HRM
20	48, 64, 128 Fs 64 Fs	BRM, 48 Fs available in slave mode only HRM
24	48, 64, 128 Fs 64 Fs	BRM, 48 Fs available in slave mode only HRM

Figure 11. Right Justified Serial Audio Formats



One Line Data Mode, Data Valid on Rising Edge of SCLK		
Bits/Sample	SCLK Rate(s)	Notes
20	128 Fs	6 inputs, 2 outputs, BRM only

Figure 12. One Line Data Serial Audio Format

3.7 Control Port Signals

Internal registers are accessed through the control port. The control port may be operated asynchronously with respect to audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no register access is required.

The control port has 2 operating modes: SPI mode and two wire mode. In both modes the CS4228A operates as a slave device. Mode selection is determined by the state of the SDOUT pin when $\overline{RST}$ transitions from low to high: high for SPI, low for two wire mode. SDOUT is internally pulled high to VL. A resistive load from SDOUT to GND of less than 47 kΩ will enable two wire mode after a hardware reset.

3.7.1 SPI Mode

In SPI mode, $\overline{CS}$ is the CS4228A chip select signal, CCLK is the control port bit clock input, and CDIN is the input data line. There is no data output line, therefore all registers are write-only in SPI mode. Data is clocked in on the rising edge of CCLK.

Figure 13 shows the operation of the control port in SPI mode. The first 7 bits on CDIN, after $\overline{CS}$ goes low, form the chip address (0010000). The eighth bit is a read/write indicator (R/$\overline{W}$), which should always be low to write. The next 8 bits set the Memory Address Pointer (MAP) which is the address of the register that is to be written. The following bytes contain the data which will be placed into the registers designated by the MAP.

The CS4228A has a MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is zero, then the MAP will stay constant for successive writes. If INCR is 1, then the MAP will increment after each byte is written, allowing block reads or writes of successive registers.

3.7.2 Two Wire Mode

In two wire mode, SDA is a bidirectional data line. Data is clocked into and out of the port by the SCL clock. The signal timing is shown in Figures 14 and 15. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low.

The first byte sent to the CS4228A after a Start condition consists of a 7 bit chip address field and a R/$\overline{W}$ bit (high for a read, low for a write). The AD0 pin determines the LSB of the chip address field. The upper 6 bits of the address field must be 00100 and the seventh bit must match AD0. If the operation is to be a write, the second byte is the Memory Address Ponter (MAP), which selects the register to be written. The succeeding byte(s) are data. If the operation is to be a read, the second byte is sent from the chip to the controller and contains the contents of the register pointed to by the current value of the MAP.

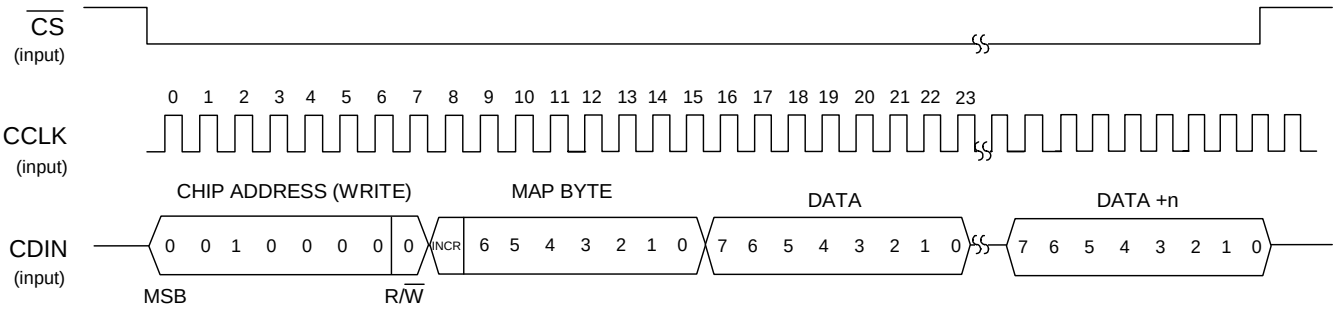


Figure 13. Control Port Timing, SPI Slave Mode Write

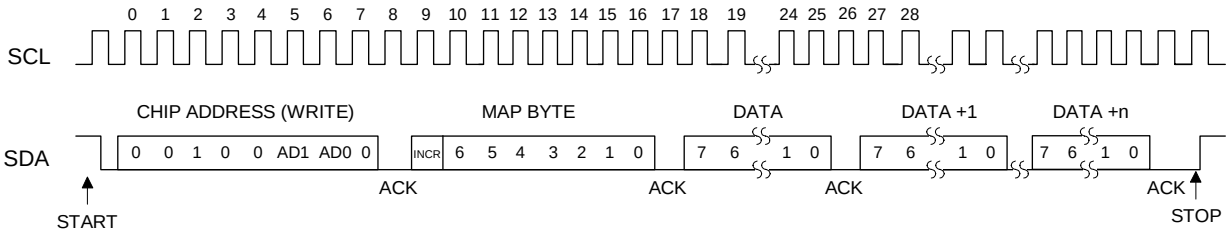


Figure 14. Control Port Timing, Two Wire Slave Mode Write

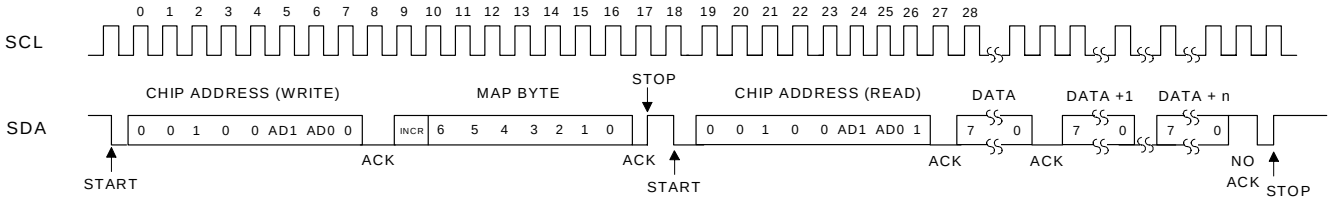


Figure 15. Control Port Timing, Two Wire Slave Mode Read

Since the read operation can not set the MAP, an aborted write operation is used as a preamble. As shown in Figure 15, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send start condition.

Send 001000x0 chip address & write operation.

Receive acknowledge bit.

Send MAP byte, auto increment off.

Receive acknowledge bit.

Send stop condition, aborting write.

Send start condition.

Send 001000x1 chip address & read operation.

Receive acknowledge bit.

Receive byte, contents of selected register.

Send acknowledge bit.

Send stop condition.

Setting the auto increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

3.8 Control Port Bit Definitions

All registers are read/write, except the Chip Status register which is read-only. For more detailed information, see the bit definition tables.

3.9 Power-up/Reset/Power Down Mode

Upon power up, the user should hold $\overline{RST}$ = 0 until the power supplies and clocks stabilize. In this state, the control registers are reset to their default settings, and the device remains in a low power mode in which the control port is inactive. The part may be held in a low power reset state by clearing the $\overline{DIGPDN}$ bit in the Chip Control register. In this state, the digital portions of the CODEC are in reset, but the control port is active and the desired register settings can be loaded. Normal operation is achieved by setting the $\overline{DIGPDN}$ bit to 1, at which time the CODEC powers up and normal operation begins.

The CS4228A will enter a stand-by mode if the master clock source stops for approximately 10 µs or if the number of MCLK cycles per LRCK period varies by more than 32. Should this occur, the control registers retain their settings.

The CS4228A will mute the analog outputs, assert the $\overline{\text{MUTEC}}$ pin and enter the Power Down Mode if the supply drops below approximately 4 volts.

3.10 Power Supply, Layout, and Grounding

The CS4228A requires careful attention to power supply and grounding details. VA is normally supplied from the system 5 VDC analog supply. VD is from a 5 VDC digital supply, or for optimum ADC performance, connect VD through a diode to a +5 V supply to lower the digital core voltage. VL should be from the supply used for the devices digitally interfacing with the CS4228A. The power up sequence of these three supply pins is not important.

AGND and DGND pins should both be tied to a solid ground plane surrounding the CS4228A. The system analog and digital ground planes should not be separated under normal circumstances. A solid ground plane underneath the part is recommended.

Decoupling capacitors should be mounted and routed in such a way as to minimize the circuit path length from the CS4228A supply pin or FILT pin, through the capacitor, and back to the applicable CS4228A AGND or DGND pin. The small value ceramic capacitors should be closest to the part. In some cases, ferrite beads in the VL, VD and VA supply lines, and low-value resistances (~ 50 Ω) in series with the LRCK, SCLK, SDIN and SDOUT lines can help reduce coupling of digital signals into the analog portions of the CS4228A.

The both capacitors on the FILT pin should be as close to the CS4228A as possible. Any noise that couples onto the FILT pin will couple directly onto all of the analog outputs. Please see the CDB4228 evaluation board data sheet for recommended layout of the decoupling components.

4. REGISTER QUICK REFERENCE

Addr	Function	7	6	5	4	3	2	1	0
MAP	Memory Address Pointer	INCR	Reserved	Reserved	MAP4	MAP3	MAP2	MAP1	MAP0
		1	0	0	0	0	0	0	1
0x01	CODEC Clock Mode	HRM	Reserved	Reserved	Reserved	CI1	CI0	Reserved	Reserved
	default=0x04	0	0	0	0	0	1	0	0
0x02	Chip Control	$\overline{\text{DIGPDN}}$	Reserved	Reserved	ADCPDN	DACPDN56	DACPDN34	DACPDN12	Reserved
	default=0x00	1	0	0	0	0	0	0	0
0x03	ADC Control	MUTL	MUTR	HPF	HPFZ	Reserved	Reserved	Reserved	Reserved
	default=0x00	0	0	0	0	0	0	0	0
0x04	DAC Mute1 Control	MUT6	MUT5	MUT4	MUT3	MUT2	MUT1	RMP1	RMP0
	default=0xFC	1	1	1	1	1	1	0	0
0x05	DAC Mute2 Control	MUTEC	MUTCZ	Reserved	Reserved	HMUTE56	HMUTE34	HMUTE12	Reserved
	default=0x80	1	0	0	0	0	0	0	0
0x06	DAC De-emphasis Control	DEMS1	DEMS0	DEM6	DEM5	DEM4	DEM3	DEM2	DEM1
	default=0x80	1	0	0	0	0	0	0	0
0x07	DAC 1 Volume Cntrl	Vol7	Vol6	Vol5	Vol4	Vol3	Vol2	Vol1	Vol0
	default=0x00	0	0	0	0	0	0	0	0
0x08	DAC 2 Volume Cntrl	Vol7	Vol6	Vol5	Vol4	Vol3	Vol2	Vol1	Vol0
	default=0x00	0	0	0	0	0	0	0	0
0x09	DAC 3 Volume Cntrl	Vol7	Vol6	Vol5	Vol4	Vol3	Vol2	Vol1	Vol0
	default=0x00	0	0	0	0	0	0	0	0
0x0A	DAC 4 Volume Cntrl	Vol7	Vol6	Vol5	Vol4	Vol3	Vol2	Vol1	Vol0
	default=0x00	0	0	0	0	0	0	0	0
0x0B	DAC 5 Volume Cntrl	Vol7	Vol6	Vol5	Vol4	Vol3	Vol2	Vol1	Vol0
	default=0x00	0	0	0	0	0	0	0	0
0x0C	DAC 6 Volume Cntrl	Vol7	Vol6	Vol5	Vol4	Vol3	Vol2	Vol1	Vol0
	default=0x00	0	0	0	0	0	0	0	0
0x0D	Serial Port Mode	DCK1	DCK0	DMS1	DMS0	Reserved	DDF2	DDF1	DDF0
	default=0x84	1	0	0	0	0	1	0	0
0x0E	Chip Status	CLKERR	ADCOVL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	read only	X	X	0	0	0	0	0	0
		7	**6**	**5**	**4**	**3**	**2**	**1**	**0**

5. REGISTER DESCRIPTIONS

All registers are read/write except for Chip Status, which is read only. See the following bit definition tables for bit assignment information. The default state of each bit after a power-up sequence or reset is listed in the tables underneath each bit's label. Default values are also marked in the text with an asterisk.

5.1 Memory Address Pointer (MAP)

Not a register

7	6	5	4	3	2	1	0
INCR	RESERVED		MAP4	MAP3	MAP2	MAP1	MAP0
1	0	0	0	0	0	0	1

INCR — memory address pointer auto increment control
- 0 - MAP is not incremented automatically.
- *1 - internal MAP is automatically incremented after each read or write.

MAP4:0 — Memory address pointer (MAP). Sets the register address that will be read or written by the control port.

5.2 CODEC Clock Mode

Address 0x01

7	6	5	4	3	2	1	0
HRM	RESERVED			CI1	CI0	RESERVED	
0	0	0	0	0	1	0	0

HRM — Sets the sample rate mode for the ADCs and DACs
- *0 - Base Rate Mode (BRM) supports sample rates up to 50 kHz
- 1 - High Rate Mode (HRM) supports sample rates up to 100 kHz. Typically used for 96 kHz sample rate.

CI1:0 — Specifies the ratio of MCLK to the sample rate of the ADCs and DACs (Fs)

CI1:0	BRM (Fs)	HRM (Fs)
0	128	64
*1	256	128
2	384	192
3	512	256

5.3 Chip Control

Address 0x02

7	6	5	4	3	2	1	0
$\overline{\text{DIGPDN}}$	RESERVED		ADCPDN	DACPDN56	DACPDN34	DACPDN12	RESERVED
1	0	0	0	0	0	0	0

$\overline{\text{DIGPDN}}$ Power down the digital portions of the CODEC
- 0 - Digital power down.
- *1 - Normal operation

ADCPDN Power down the analog section of the ADC
- *0 - Normal
- 1 - ADC power down.

DACPDN12 Power down the analog section of DAC 1 and 2
- *0 - Normal
- 1 - Power down DAC 1 and 2.

DACPDN34 Power down the analog section of DAC 3 and 4
- *0 - Normal
- 1 - Power down DAC 3 and 4.

DACPDN56 Power down the analog section of DAC 5 and 6
- *0 - Normal
- 1 - Power down DAC 5 and 6.

5.4 ADC Control

Address 0x03

7	6	5	4	3	2	1	0
MUTL	MUTR	HPF	HPFZ	RESERVED			
0	0	0	0	0	0	0	0

MUTL, MUTR ADC left and right channel mute control
- *0 - Normal
- 1 - Selected ADC output muted

HPF ADC DC offset removal. See “High Pass Filter” for more information
- *0 - Enabled
- 1 - Disabled

HPFZ ADC DC offset averaging freeze. See “High Pass Filter” for more information
- *0 - Normal. The DC offset average is dynamically calculated and subtracted from incoming ADC data.
- 1 - Freeze. The DC offset average is frozen at the current value and subtracted from incoming ADC data. Allows passthru of DC information.

5.5 DAC Mute1 Control

Address 0x04

7	6	5	4	3	2	1	0
MUT6	MUT5	MUT4	MUT3	MUT2	MUT1	RMP1	RMP0
1	1	1	1	1	1	0	0

MUT6 - MUT1 Mute control for DAC6 - DAC1 respectively. When asserted, the corresponding DAC is digitally attenuated to its maximum value (90.5 dB). When deasserted, the corresponding DAC attenuation value returns to the value stored in the corresponding Digital Volume Control register. The attenuation value is ramped up and down at the rate specified by RMP1:0.

0 - Normal output level

*1 - Selected DAC output fully attenuated.

RMP1:0 Attenuation ramp rate.

*0 - 0.5 dB change per 4 LRCKs

1 - 0.5 dB change per 8 LRCKs

2 - 0.5 dB change per 16 LRCKs

3 - 0.5 dB change per 32 LRCKs

5.6 DAC Mute2 Control

Address 0x05

7	6	5	4	3	2	1	0
MUTEC	MUTCZ	RESERVED		HMUTE56	HMUTE34	HMUTE12	RESERVED
1	0	0	0	0	0	0	0

MUTEC Controls the $\overline{\text{MUTEC}}$ pin

0 - Normal operation

*1 - $\overline{\text{MUTEC}}$ pin asserted low

MUTCZ Automatically asserts the $\overline{\text{MUTEC}}$ pin on consecutive zeros. When enabled, 512 consecutive zeros on all six DAC inputs will cause the $\overline{\text{MUTEC}}$ pin to be asserted low. A single non-zero value on any DAC input will cause the $\overline{\text{MUTEC}}$ pin to deassert.

*0 - Disabled

1 - Enabled

HMUTE56/34/12 Hard mute the corresponding DAC pair. When asserted, zero data is sent to the corresponding DAC pair causing an instantaneous mute. To prevent high frequency transients on the outputs, a DAC pair should be fully attenuated by asserting the corresponding MUT6-MUT1 bits in the DAC Mute Control register or by writing 0xFF to the corresponding Digital Volume Control registers before asserting HMUTE.

*0 - Normal operation

1 - DAC pair is muted

5.7 DAC De-emphasis Control

Address 0x06

7	6	5	4	3	2	1	0
DEMS1	DEMS0	DEM6	DEM5	DEM4	DEM3	DEM2	DEM1
1	0	0	0	0	0	0	0

DEMS1:0 Selects the DAC de-emphasis response curve.
- 0 - Reserved
- 1 - De-emphasis for 48 kHz
- *2 - De-emphasis for 44.1 kHz
- 3 - De-emphasis for 32 kHz

DEM6 - DEM1 De-emphasis control for DAC6 - DAC1 respectively
- *0 - De-emphasis off
- 1 - De-emphasis on

5.8 Digital Volume Control

Addresses 0x07, 0x08, 0x09, 0x0A, 0x0B, 0x0C

7	6	5	4	3	2	1	0
VOLn							
0	0	0	0	0	0	0	0

VOL6 - VOL1 Address 0x0C - 0x07 sets the attenuation level for DAC 6 - DAC1 respectively. The attenutation level is ramped up and down at the rate specified by RMP1:0 in the DAC Volume Control Setup register.
0 - 181 represents 0 to 90.5 dB of attenuation in 0.5 dB steps.

5.9 Serial Port Mode

Address 0x0D

7	6	5	4	3	2	1	0
DCK1	DCK0	DMS1	DMS0	RESERVED	DDF2	DDF1	DFF0
1	0	0	0	0	1	0	0

DCK1:0 Sets the number of Serial Clocks (SCLK) per Fs period (LRCLK)

DCK1:0	BRM (Fs)	HRM (Fs)
0	32 (1)	(3)
1	48 (2)	(3)
2	*64	32 (1)
3	128	64

Notes: 1. All formats will default to 16 bits
2. External Slave mode only
3. Invalid mode

DMS1:0 Sets the master/slave mode of the serial audio port
*0 - Slave (External LRCLK, SCLK)
1 - Reserved
2 - Reserved
3 - Master (No 48 Fs SCLK in BRM

DDF2:0 Serial Port Data Format
0 - Right Justified, 24-bit
1 - Right Justified, 20-bit
2 - Right Justified, 16-bit
3 - Left Justified, maximum 24-bit
*4 - I^2S compatible, maximum 24-bit
5 - One-line Data Mode, available in BRM only
6 - Reserved
7 - Reserved

5.10 Chip Status

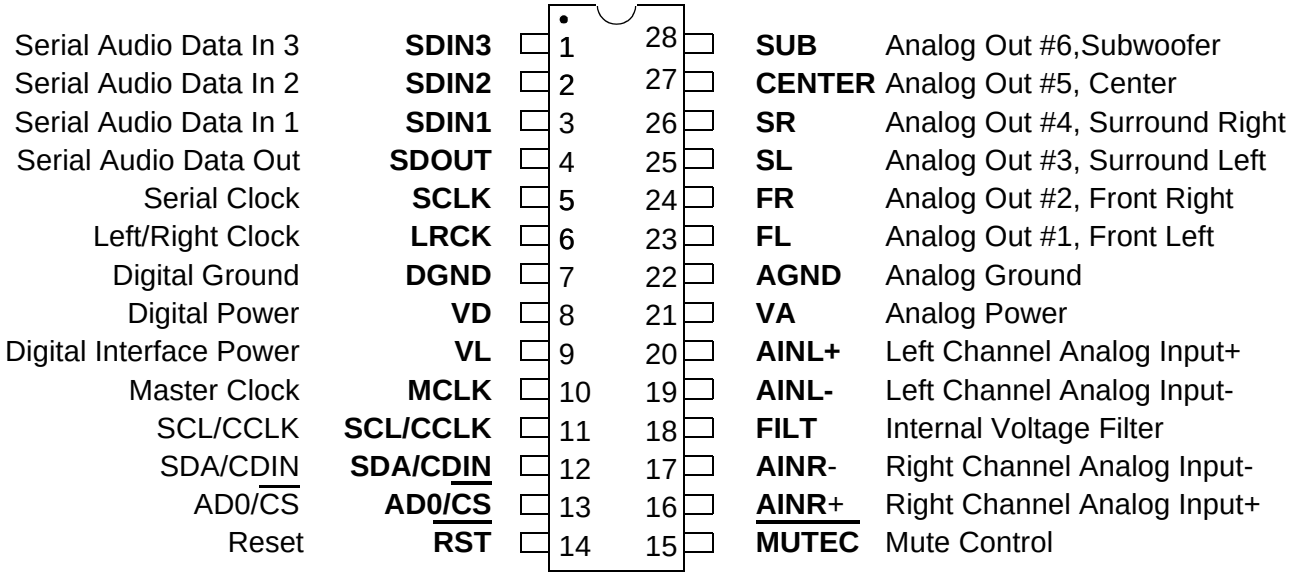
Address 0x0E

7	6	5	4	3	2	1	0
CLKERR	ADCOVL	RESERVED					
X	X	0	0	0	0	0	0

CLKERR Clocking system status, read only
0 - No Error
1 - No MCLK is present, or a request for clock change is in progress

ADCOVL ADC overflow bit, read only
0 - No overflow
1 - ADC overflow has occurred

6. PIN DESCRIPTION



SDIN1, SDIN2, SDIN3	1, 2, 3	**Serial Audio Data In** (*Input*) - Two's complement MSB-first serial audio data is input on this pin. The data is clocked into SDIN1, SDIN2, SDIN3 via the serial clock and the channel is determined by the Left/Right clock. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Serial Mode Register. The options are detailed in Figures 9, 10, 11, and 12.
SDOUT	4	**Serial Audio Data Out** (*Output*) - Two's complement MSB-first serial data is output on this pin. The data is clocked out of SDOUT via the serial clock and the channel is determined by the Left/Right clock. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Serial Mode Register. The options are detailed in Figures 9, 10, 11 and 12. The state of the SDOUT pin during reset is used to set the Control Port Mode (two wire or SPI). When $\overline{RST}$ is low, SDOUT is configured as an input, and the rising edge of $\overline{RST}$ latches the state of the pin. A weak internal pull up is present such that a resistive load less than 47 kΩ will pull the pin low, and the control port mode is two wire. When the resistive load on SDOUT is greater than 47 kΩ during reset, the control port mode is SPI.
SCLK	5	**Serial Clock** (*Bidirectional*) - Clocks serial data into the SDIN1, SDIN2, and SDIN3 pins, and out of the SDOUT pin. The pin is an output in master mode, and an input in slave mode. In master mode, SCLK is configured as an output. MCLK is divided internally to generate SCLK at the desired multiple of the sample rate. In slave mode, SCLK is configured as an input. The serial clock can be provided externally, or the pin can be grounded and the serial clock derived internally from MCLK. The required relationship between the Left/Right clock, serial clock and serial audio data is defined by the Serial Port Mode register. The options are detailed in Figures 9, 10, 11, and 12.

LRCK	6	**Left/Right Clock** (*Bidirectional*) - The Left/Right clock determines which channel is currently being input or output on the serial audio data output, SDOUT. The frequency of the Left/Right clock must be at the output sample rate, Fs. In Master mode, LRCK is an output, in Slave Mode, LRCK is an input whose frequency must be equal to Fs and synchronous to the Master clock. Audio samples in Left/Right pairs represent simultaneously sampled analog inputs whereas Right/Left pairs will exhibit a one sample period difference. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Serial Port Mode register. The options are detailed in Figures 9, 10, 11 and 12.
DGND	7	**Digital Ground** (*Input*) - Digital Ground Reference.
VD	8	**Digital Power** (*Input*) - Digital Power Supply. Typically 5.0 VDC.
VL	9	**Digital Interface Power** (*Input*) - Digital interface power supply. Typically 2.5, 3.3 or 5.0 VDC. All digital output voltages and input threshholds scale with VL.
MCLK	10	**Master Clock** (*Input*) - The master clock frequency must be either 128x, 256x, 384x or 512x the input sample rate in Base Rate Mode (BRM) and either 64x, 128x, 192x, or 256x the input sample rate in High Rate Mode (HRM). Table 2 illustrates several standard audio sample rates and the required master clock frequencies. The MCLK/Fs ratio is set by the CI1:0 bits in the CODEC Clock Mode register.

Sample Rate (kHz)	MCLK (MHz)							
	HRM				BRM			
	64x	128x	192x	256x	128x	256x	384x	512x
32	-	-	-	-	4.0960	8.1920	12.2880	16.3840
44.1	-	-	-	-	5.6448	11.2896	16.9344	22.5792
48	-	-	-	-	6.1440	12.2880	18.4320	24.5760
64	4.0960	8.1920	12.2880	16.3840	-	-	-	-
88.2	5.6448	11.2896	16.9344	22.5792	-	-	-	-
96	6.1440	12.2880	18.4320	24.5760	-	-	-	-

Table 2. Common Master Clock Frequencies

SCL/CCLK	11	**Serial Control Interface Clock (***Input*) - Clocks the serial control data into or out of SDA/CDIN.
SDA/CDIN	12	**Serial Control Data I/O** (*Bidirectional/Input*) - In two wire mode, SDA is a bidirectional control port data line. A pull up resistor must be provided for proper open drain output operation. In SPI mode, CDIN is the control port data input line. The state of the SDOUT pin during reset is used to set the control port mode.
ADO/$\overline{\text{CS}}$	13	**Address Bit 0 / Chip Select** (Input) - In two wire mode, AD0 is the LSB of the chip address. In SPI mode, $\overline{\text{CS}}$ is used as a enable for the control port interface.
$\overline{\text{RST}}$	14	**Reset** (Input) - When low, the device enters a low power mode and all internal registers are reset to the default settings, including the control port. The control port can not be accessed when reset is low. When high, the control port and the CODEC become operational.
MUTEC	15	**Mute Control** (*Output*) - The Mute Control pin goes low during the following conditions: power-up initialization, power-down, reset, no master clock present, or if the master clock to left/right clock frequency ratio is incorrect. The Mute Control pin can also be user controlled by the MUTEC bit in the DAC Mute2 Control register. Mute Control can be automatically asserted when 512 consecutive zeros are detected on all six DAC inputs, and automatically deasserted when a single non-zero value is sent to any of the six DACs. The mute on zero function is controlled by the MUTCZ bit in the DAC Mute2 Control register. The $\overline{\text{MUTEC}}$ pin is intended to be used as a control for an external mute circuit to achieve a very low noise floor during periods when no audio is present on the DAC outputs, and to prevent the clicks and pops that can occur in any single supply system. Use of the Mute Control pin is not mandatory but recommended.

AINR+, AINR-, AINL+, AINL-	16, 17, 19, 20	**Differential Analog Inputs** (*Input*) - The analog signal inputs are presented deferentially to the modulators via the AINR+/- and AINL+/- pins. The + and - input signals are 180° out of phase resulting in a nominal differential input voltage of twice the input pin voltage. These pins are biased to the internal reference voltage of approximately 2.3 V. A passive anti-aliasing filter is required for best performance, as shown in Figure 5. The inputs can be driven at -1 dB FS single-ended if the unused input is connected to ground through a large value capacitor. A single ended to differential converter circuit can also be used for slightly better performance.
FILT	18	**Internal Voltage Filter** (*Output*) - Filter for internal circuits. An external capacitor is required from FILT to analog ground, as shown in Figure 5. FILT is not intended to supply external current. FILT+ has a typical source impedance of 250 kΩ and any current drawn from this pin will alter device performance. Care should be taken during board layout to keep dynamic signal traces away from this pin.
VA	21	**Analog Power** (*Input*) **-** Power for the analog and reference circuits. Typically 5.0 VDC.
AGND	22	**Analog Ground** (*Input*) **-** Analog ground reference.
FR, FL, SR, SL SUB, CENTER	23, 24, 25, 26, 27, 28	**Analog Outputs** (*Output*) **-** Analog outputs from the DACs. The full scale analog output level is specified in the Analog Characteristics specifications table. The amplitude of the outputs is controlled by the Digital Volume Control registers 0x07 - 0x0C..

7. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the full scale RMS value of the signal to the RMS sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dbFs signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Total Harmonic Distortion + Noise

The ratio of the RMS value of the signal to the RMS sum of all other spectral components over the specified bandwidth (typically 20 Hz to 20 kHz), including distortion components. Expressed in decibels. ADCs are measured at -1dBFs as suggested in AES 17-1991 Annex A.

Idle Channel Noise / Signal-to-Noise-Ratio

The ratio of the RMS analog output level with 1 kHz full scale digital input to the RMS analog output level with all zeros into the digital input. Measured A-weighted over a 10 Hz to 20 kHz bandwidth. Units in decibels. This specification has been standardized by the Audio Engineering Society, AES17-1991, and referred to as Idle Channel Noise. This specification has also been standardized by the Electronic Industries Association of Japan, EIAJ CP-307, and referred to as Signal-to-Noise-Ratio.

Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the RMS sum of all the in-band harmonics of the test signal. Units in decibels.

Interchannel Isolation

A measure of crosstalk between channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Frequency Response

A measure of the amplitude response variation from 20 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units are in decibels.

Gain Error

The deviation from the nominal full scale output for a full scale input.

Gain Drift

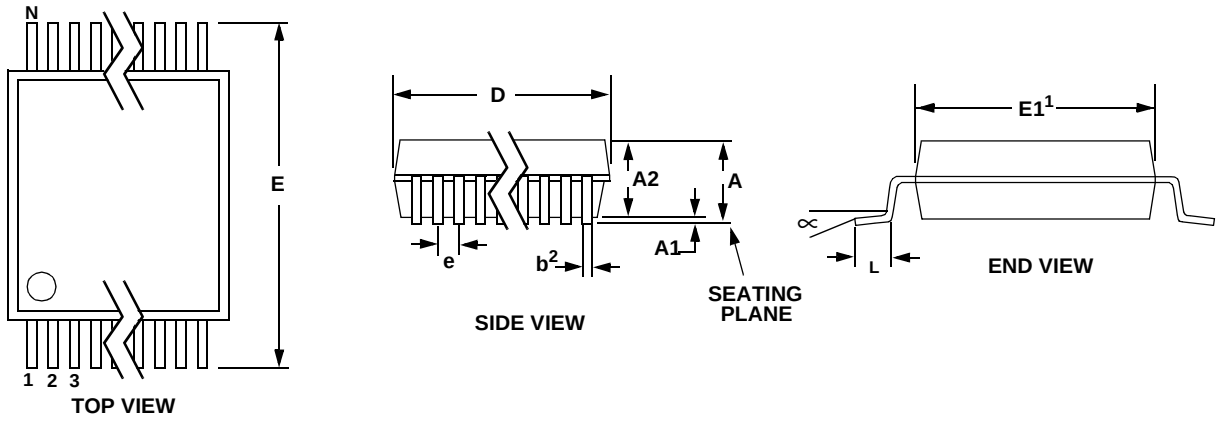
The change in gain value with temperature. Units in ppm/°C.

Offset Error

For the ADCs, the deviation in LSBs of the output from mid-scale with the selected input grounded. For the DACs, the deviation of the output from zero (relative to CMOUT) with mid-scale input code. Units are in volts.

8. PACKAGE DIMENSIONS

28L SSOP PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.006	0.010	0.05	0.15	0.25	
A2	0.064	0.069	0.074	1.62	1.75	1.88	
b	0.009	--	0.015	0.22	--	0.38	2,3
D	0.390	0.4015	0.413	9.90	10.20	10.50	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.0354	0.041	0.63	0.90	1.03	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-150

Controlling Dimension is Millimeters

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.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