



CS4396

24-Bit, 192 kHz D/A Converter for Digital Audio

Features

- 24 Bit Conversion
- Up to 192 kHz Sample Rates
- 120 dB Dynamic Range
- -100 dB THD+N
- Advanced Dynamic-Element Matching
- Low Clock Jitter Sensitivity
- Digital De-emphasis for 32 kHz, 44.1 kHz and 48 kHz
- External Reference Input

Description

The CS4396 is a complete high performance 24-bit 48/96/192 kHz stereo digital-to-analog conversion system. The device includes a digital interpolation filter followed by a oversampled multi-bit delta-sigma modulator which drives dynamic-element-matching (DEM) selection logic. The output from the DEM block controls the input to a multi-element switched capacitor DAC/low-pass filter, with fully-differential outputs. This multi-bit architecture features significantly lower out-of-band noise and jitter sensitivity than traditional 1-bit designs, and the advanced DEM guarantees low noise and distortion at all signal levels.

ORDERING INFORMATION

CS4396-KS -10° to 70° C 28-pin Plastic SOIC
CDB4397 Evaluation Board

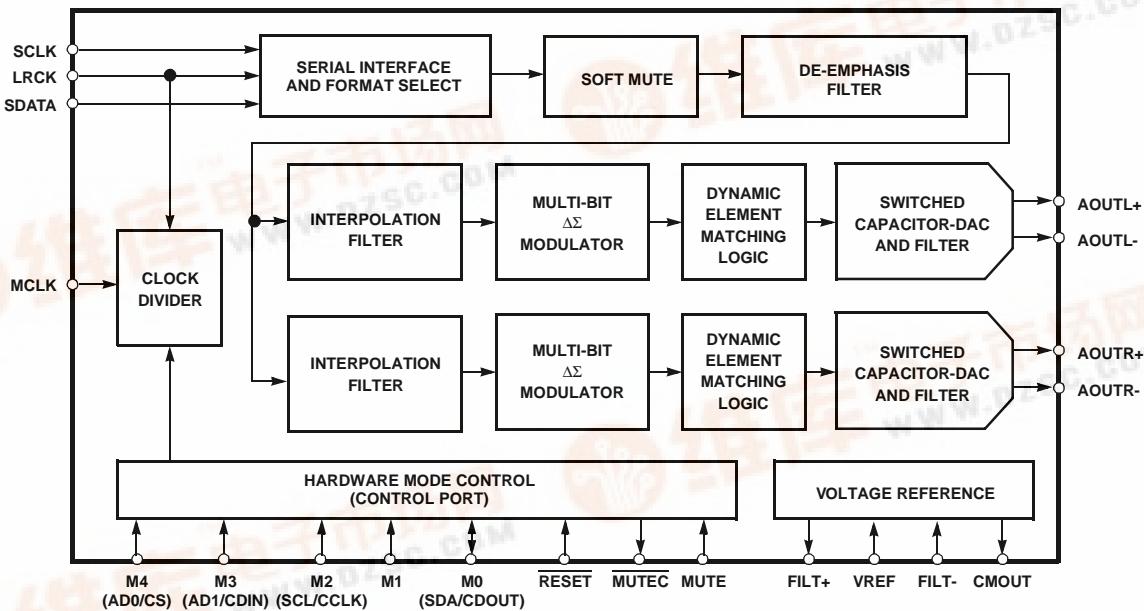


TABLE OF CONTENTS

1.0 CHARACTERISTICS/SPECIFICATIONS	4
ANALOG CHARACTERISTICS.....	4
Dynamic Performance - Single Speed Mode - Fs equal to 48 kHz	4
Dynamic Performance - Double Speed Mode - Fs equal to 96 kHz	4
Dynamic Performance - Quad-Speed Mode - Fs equal to 192 kHz	4
ANALOG CHARACTERISTICS.....	5
Power Supplies	5
Analog Output	5
Combined Digital and On-chip Analog Filter Response - Single Speed Mode	6
Combined Digital and On-chip Analog Filter Response - Double Speed Mode	6
Combined Digital and On-chip Analog Filter Response - Quad-Speed Mode	6
DIGITAL CHARACTERISTICS.....	7
ABSOLUTE MAXIMUM RATINGS	7
RECOMMENDED OPERATING CONDITIONS	7
SWITCHING CHARACTERISTICS	8
SWITCHING CHARACTERISTICS - CONTROL PORT	9
I ² C [®] Mode	9
SPI Mode	10
2.0 TYPICAL CONNECTION DIAGRAM	11
3.0 REGISTER DESCRIPTION	12
3.1 Differential DC offset calibration	12
3.2 Soft Mute	12
3.3 Mode Select	13
3.4 Power DowN	13
4.0 PIN DESCRIPTION	14
5.0 APPLICATIONS	19
5.1 Recommended Power-up Sequence	19
6.0 CONTROL PORT INTERFACE	20
6.1 SPI Mode	20
6.2 I ² C Mode	20
6.2 Memory Address Pointer (MAP)	20
7.0 PARAMETER DEFINITIONS	26
8.0 REFERENCES	26
9.0 PACKAGE DIMENSIONS	27

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"The I²C-Bus Specification: Version 2.0" Philips Semiconductors, December 1998.
<http://www.semiconductors.philips.com>

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TABLE OF FIGURES

Figure 1. Serial Audio Input Timing	8
Figure 2. I ² C Control Port Timing	9
Figure 3. SPI Control Port Timing	10
Figure 4. Typical Connection Diagram - Hardware Mode (Control Port Mode)	11
Figure 5. Control Port Timing, I ² C Mode	21
Figure 6. Control Port Timing, SPI mode	21
Figure 7. Single-speed Transition Band	23
Figure 8. Single-speed Stopband Rejection	23
Figure 9. Single-speed Transition Band	23
Figure 10. Single-speed Frequency Response	23
Figure 11. Double-speed Stopband	23
Figure 12. Double-speed Transition Band	23
Figure 13. Double-speed Transition Band	23
Figure 14. Double-speed Frequency Response	23
Figure 15. Quad-speed Stopband Rejection	24
Figure 16. Quad-speed Transition Band	24
Figure 17. Quad-speed Transition Band	24
Figure 18. Quad-speed Frequency Response	24
Figure 19. De-Emphasis Curve	24
Figure 20. Format 0, Left Justified	25
Figure 21. Format 1, I ² S	25
Figure 22. Format 2, Right Justified, 16-Bit Data	25
Figure 23. Format 3, Right Justified, 24-Bit Data	25

1.0 CHARACTERISTICS/SPECIFICATIONS

ANALOG CHARACTERISTICS

($T_A = 25^\circ\text{C}$; Logic "1" = $VD = 5\text{ V}$; $VA = 5\text{V}$; Logic "0" = $DGND$; Full-Scale Output Sine Wave, 997 Hz; $MCLK = 12.288\text{ MHz}$; $SCLK = 3.072\text{ MHz}$, Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified. Test load $R_L = 1\text{ k}\Omega$, $C_L = 10\text{ pF}$)

Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Performance - Single Speed Mode - F_s equal to 48 kHz					
Dynamic Range (Note 1)					
24-Bit unweighted		TBD	117	-	dB
24-Bit A-Weighted		TBD	120	-	dB
16-Bit unweighted		-	95	-	dB
(Note 2) A-Weighted		-	98	-	dB
Total Harmonic Distortion + Noise (Note 1)	THD+N				
24-Bit 0 dB		-	-100	TBD	dB
24-Bit -20 dB		-	-97	TBD	dB
24-Bit -60 dB		-	-57	TBD	dB
16-Bit 0 dB		-	-95	-	dB
(Note 2) -20 dB		-	-75	-	dB
(Note 2) -60 dB		-	-35	-	dB
Dynamic Performance - Double Speed Mode - F_s equal to 96 kHz					
Dynamic Range (Note 1)					
24-Bit unweighted		TBD	117	-	dB
24-Bit A-Weighted		TBD	120	-	dB
40 kHz bandwidth unweighted		TBD	114	-	dB
16-Bit unweighted		-	92	-	dB
(Note 2) A-Weighted		-	98	-	dB
Total Harmonic Distortion + Noise (Note 1)	THD+N				
24-Bit 0 dB		-	-100	TBD	dB
24-Bit -20 dB		-	-97	TBD	dB
24-Bit -60 dB		-	-57	TBD	dB
16-Bit 0 dB		-	-95	-	dB
(Note 2) -20 dB		-	-75	-	dB
(Note 2) -60 dB		-	-35	-	dB
Dynamic Performance - Quad-Speed Mode - F_s equal to 192 kHz					
Dynamic Range (Note 1)					
24-Bit unweighted		TBD	117	-	dB
24-Bit A-Weighted		TBD	120	-	dB
40 kHz bandwidth unweighted		TBD	114	-	dB
16-Bit unweighted		-	92	-	dB
(Note 2) A-Weighted		-	98	-	dB
Total Harmonic Distortion + Noise (Note 1)	THD+N				
24-Bit 0 dB		-	-100	TBD	dB
24-Bit -20 dB		-	-97	TBD	dB
24-Bit -60 dB		-	-57	TBD	dB
16-Bit 0 dB		-	-95	-	dB
(Note 2) -20 dB		-	-75	-	dB
(Note 2) -60 dB		-	-35	-	dB

Notes: 1. Triangular PDF dithered data.
2. Performance limited by 16-bit quantization noise.

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	VD = 3 V			VD = 5 V			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Supplies								
Supply Current VA = 5 V	normal operation I _A	-	20	TBD	-	20	TBD	mA
	normal operation I _D	-	TBD	TBD	-	TBD	TBD	mA
	power-down state I _D + I _A	-	60	-	-	30	-	μA
Power Dissipation VA = 5 V	normal operation power-down		-	TBD	TBD	-	TBD	mW
			-	0.3	-	-	0.3	mW
Power Supply Rejection Ratio (1 kHz) (120 Hz)	PSRR	-	60	-	-	60	-	dB
		-	40	-	-	40	-	dB

Parameter	Symbol	Min	Typ	Max	Unit
Analog Output					
Full Scale Differential Output Voltage		TBD	1.4VREF	TBD	V _{pp}
Common Mode Voltage		-	0.5VREF	-	V _{DC}
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Drift		-	100	-	ppm/°C
Differential DC Offset		-	2.0	TBD	mV
AC-Load Resistance	R _L	1	-	-	kΩ
Load Capacitance	C _L	-	-	100	pF
Interchannel Isolation (1 kHz)		-	90	-	dB

Notes: 3. Valid with the recommended capacitor values on FILT+ and CMOUT as shown in Figure 1. Increasing the capacitance will also increase the PSRR.

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
Combined Digital and On-chip Analog Filter Response - Single Speed Mode					
Passband (Note 4) to -0.1 dB corner to -3 dB corner		- -	- -	0.470 0.492	Fs Fs
Frequency Response 10 Hz to 20 kHz		-0.020	-	+0.015	dB
Passband Ripple		-	-	± 0.0001	dB
StopBand		.5465	-	-	Fs
StopBand Attenuation (Note 5)		102	-	-	dB
Group Delay (Note 6)	tgd	-	37/Fs	-	s
De-emphasis Error (Note 7) Fs = 32 kHz (Relative to 1 kHz) Fs = 44.1 kHz Fs = 48 kHz		- - -	- - -	± 0.10 ± 0.10 ± 0.13	dB dB dB
Combined Digital and On-chip Analog Filter Response - Double Speed Mode					
Passband (Note 4) to -0.1 dB corner to -3 dB corner		0 0	- -	0.448 0.486	Fs Fs
Frequency Response 10 Hz to 20 kHz		-0.017	-	0.035	dB
Passband Ripple		-	-	± 0.0008	dB
StopBand		.570	-	-	Fs
StopBand Attenuation (Note 5)		82	-	-	dB
Group Delay	tgd	-	20/Fs	-	s
Combined Digital and On-chip Analog Filter Response - Quad-Speed Mode					
Passband (Note 4) to -0.1 dB corner to -3 dB corner		- -	- -	0.385 0.472	Fs Fs
Frequency Response 10 Hz to 20 kHz		0	-	+0.015	dB
Passband Ripple		-	-	± 0.00065	dB
StopBand		0.635	-	-	Fs
StopBand Attenuation (Note 5)		83	-	-	dB
Group Delay	tgd	-	11/Fs	-	s

Notes:

4. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 7-18) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
5. For Single-Speed Mode, the Measurement Bandwidth is 0.5465 Fs to 1.4 Fs.
For Double-Speed Mode, the Measurement Bandwidth is 0.570 Fs to 1.4 Fs.
For Quad-Speed Mode, the Measurement Bandwidth is 0.635 Fs to 1.3 Fs.
6. Group Delay for Fs=48 kHz 37/48 kHz=770 μ s
7. De-emphasis is available only in Single Speed Mode.

DIGITAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$; $VD = 3.0\text{V} - 5.25\text{V}$)

Parameters	Symbol	Min	Typ	Max	Units
High-Level Input Voltage $VD = 5\text{ V}$	V_{IH}	2.0	-	-	V
		2.0	-	-	V
Low-Level Input Voltage $VD = 5\text{ V}$	V_{IL}	-	-	0.8	V
		-	-	0.8	V
Input Leakage Current	I_{in}	-	-	± 10	μA
Input Capacitance		-	8	-	pF
Maximum MUTEC Drive Current		-	3	-	mA

ABSOLUTE MAXIMUM RATINGS (AGND = 0 V, all voltages with respect to ground.)

Parameter	Symbol	Min	Max	Unit
DC Power Supply: Positive Analog Positive Digital Reference Voltage	VA	-0.3	6.0	V
	VD	-0.3	6.0	V
	VREF	-0.3	VA	V
Input Current, Any Pin Except Supplies	I_{in}	-	± 10	mA
Digital Input Voltage	V_{IND}	-0.3	$(VD)+0.4$	V
Ambient Operating Temperature (power applied)	T_A	-55	125	$^\circ\text{C}$
Storage Temperature	T_{stg}	-65	150	$^\circ\text{C}$

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (DGND = 0V; all voltages with respect to ground)

Parameter	Symbol	Min	Typ	Max	Unit
DC Power Supply: Positive Digital Positive Analog Reference Voltage	VD	3.0	3.3	5.25	V
	VA	4.75	5.0	5.25	V
	VREF	TBD	5.0	VA	V
Specified Temperature Range	T_A	-10	-	70	$^\circ\text{C}$

SWITCHING CHARACTERISTICS (T_A = -10 to 70°C; Logic 0 = AGND = DGND; Logic 1 = VD = 5.25 to 3.0 Volts; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Input Sample Rate (Single-speed mode) (Double-speed mode) (Quad-speed mode)	Fs	16	-	50	kHz
	Fs	50	-	100	kHz
	Fs	100	-	200	kHz
LRCK Duty Cycle		45	50	55	%
MCLK Frequency (Single-speed 256 Fs, Double speed 128 Fs or Quad-speed 64 Fs)		4.096	-	12.8	MHz
MCLK Frequency (Single-speed 384 Fs, Double speed 192 Fs or Quad-speed, 96 Fs)		6.144	-	19.2	MHz
MCLK Frequency (Single-speed 512 Fs, Double speed 256 Fs or Quad-speed, 128 Fs)		8.192	-	25.6	MHz
MCLK Frequency (Single-speed 768 Fs, Double speed 384 Fs or Quad-speed, 192 Fs)		12.288	-	38.4	MHz
MCLK Duty Cycle		40	50	60	%
SCLK Frequency (Single-speed mode) (Double-speed mode) (Quad-speed mode)		-	-	256×Fs	Hz
		-	-	128×Fs	Hz
		-	-	64×Fs	Hz
SCLK rising to LRCK edge delay	t _{slrd}	20	-	-	ns
SCLK rising to LRCK edge setup time	t _{slrs}	20	-	-	ns
SDATA valid to SCLK rising setup time	t _{sdlrs}	20	-	-	ns
SCLK rising to SDATA hold time	t _{sdh}	20	-	-	ns

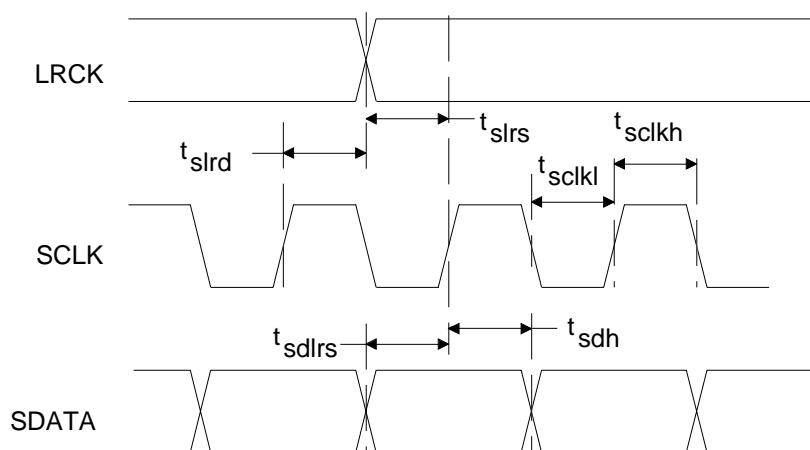


Figure 1. Serial Audio Input Timing

SWITCHING CHARACTERISTICS - CONTROL PORT

($T_A = 25^\circ\text{C}$; $VD = 5.25\text{ V}$ to 3.0 Volts ; Inputs: logic 0 = AGND, logic 1 = VD , $C_L = 30\text{ pF}$)

Parameter	Symbol	Min	Max	Unit
<i>I²C® Mode</i>				
SCL Clock Frequency	f_{scl}	-	100	KHz
RST Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	μs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	μs
Clock Low time	t_{low}	4.7	-	μs
Clock High Time	t_{high}	4.0	-	μs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	μs
SDA Hold Time from SCL Falling	t_{hdd}	0	-	μs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of Both SDA and SCL Lines	t_r	-	1	μs
Fall Time of Both SDA and SCL Lines	t_f	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	μs

Notes: 8. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

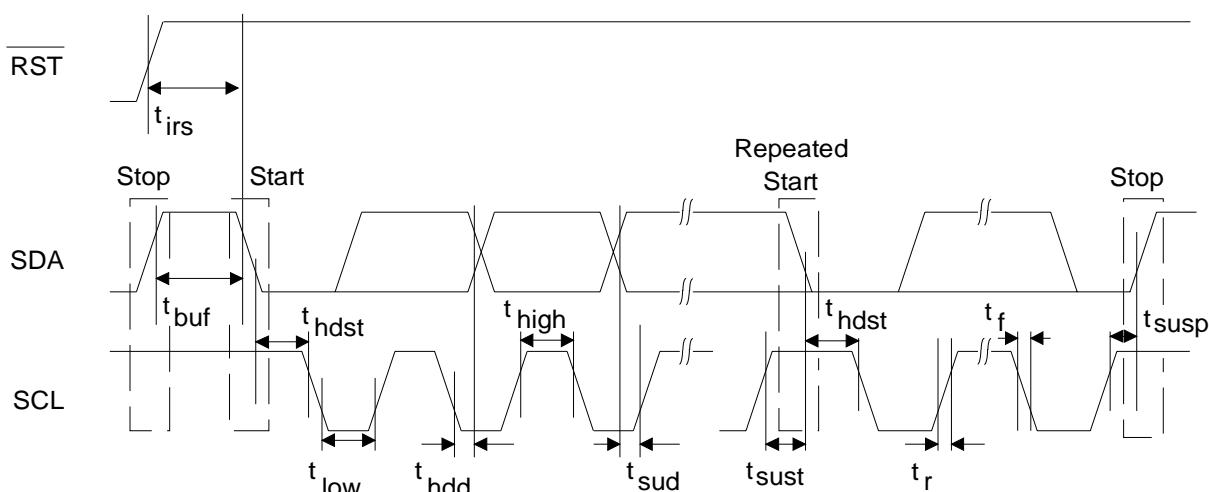


Figure 2. I²C Control Port Timing

SWITCHING CHARACTERISTICS - CONTROL PORT

($T_A = 25^\circ C$; $VD = 5.25 V$ to 3.0 Volts; Inputs: logic 0 = AGND, logic 1 = VD , $C_L = 30 pF$)

Parameter	Symbol	Min	Max	Unit
SPI Mode				
CCLK Clock Frequency	f_{sclk}	-	6	MHz
RST Rising Edge to CS Falling	t_{srs}	500	-	ns
CCLK Edge to CS Falling (Note 9)	t_{spi}	500	-	ns
CS High Time Between Transmissions	t_{csh}	1.0	-	μs
CS Falling to CCLK Edge	t_{css}	20	-	ns
CCLK Low Time	t_{scl}	66	-	ns
CCLK High Time	t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time	t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time (Note 10)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN (Note 11)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN (Note 11)	t_{f2}	-	100	ns
CCLK Falling to CDOUT valid	t_{ov}	45	-	ns

Notes: 9. t_{spi} only needed before first falling edge of \overline{CS} after \overline{RST} rising edge. $t_{spi} = 0$ at all other times.

10. Data must be held for sufficient time to bridge the transition time of CCLK.

11. For $F_{SCK} < 1$ MHz

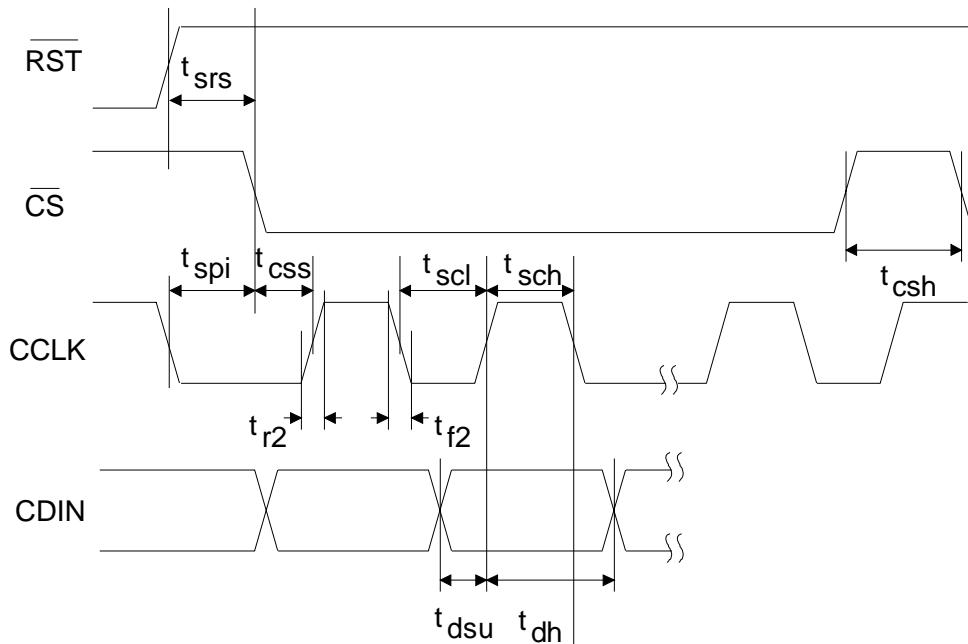


Figure 3. SPI Control Port Timing

2.0 TYPICAL CONNECTION DIAGRAM

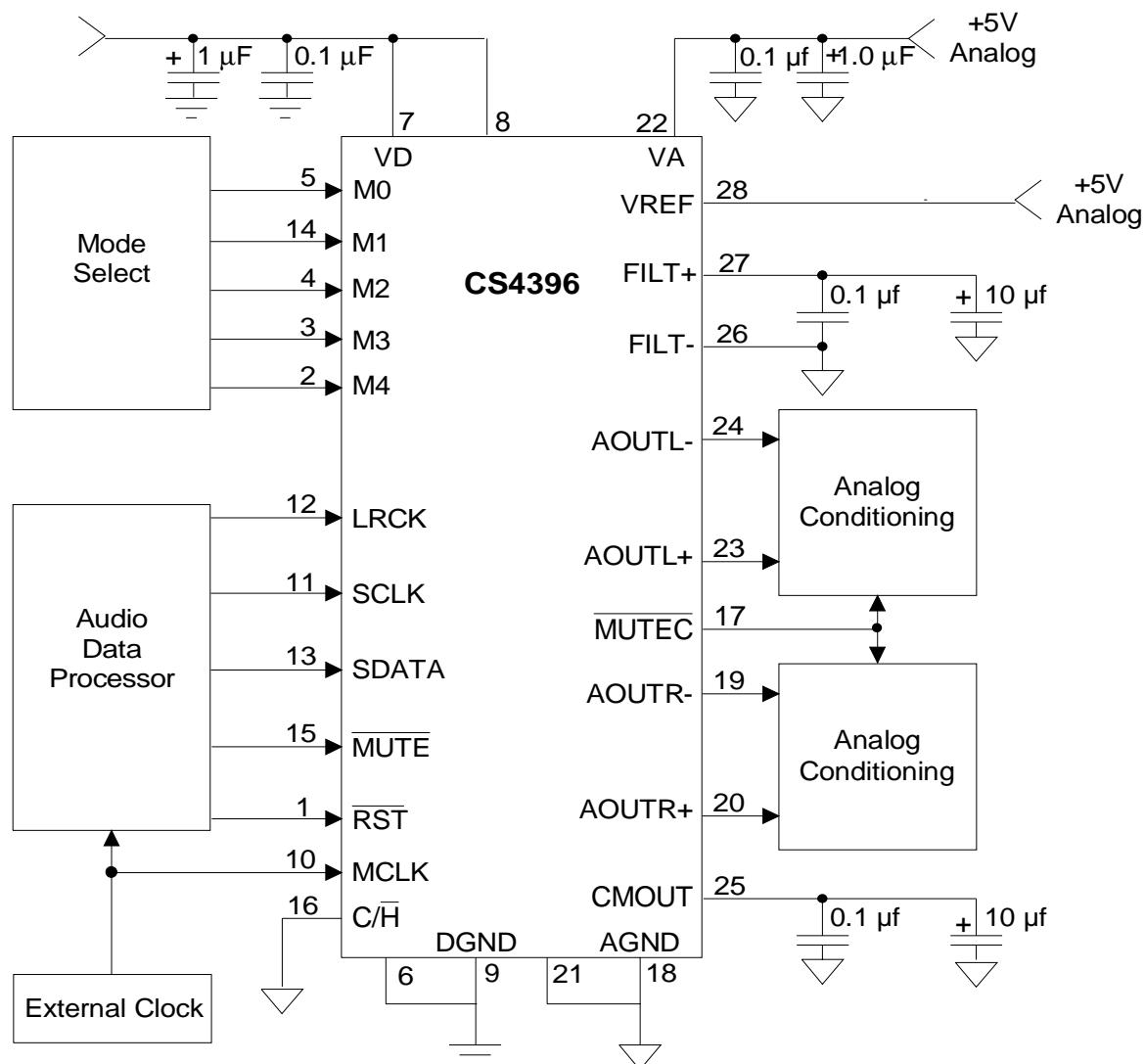


Figure 4. Typical Connection Diagram - Hardware Mode (Control Port Mode)

3.0 REGISTER DESCRIPTION

3.1 DIFFERENTIAL DC OFFSET CALIBRATION

Mode Control Register (address 01h)

7	6	5	4	3	2	1	0
CAL	MUTE	M4	M3	M2	M1	M0	PDN

Access:

R/W in I²C and SPI.

Default:

0 - Disabled

Function:

Enabling this function will initiate a calibration to minimize the differential DC offset. This function will be automatically reset following completion of the calibration sequence.

CAL	MODE
0	Disabled : CAL complete
1	Enabled : CAL initiated

Table 1.

3.2 SOFT MUTE

Mode Control Register (address 01h)

7	6	5	4	3	2	1	0
CAL	MUTE	M4	M3	M2	M1	M0	PDN

Access:

R/W in I²C and SPI.

Default:

0 - Enabled

Function:

The analog outputs will ramp to a muted state when enabled. The ramp requires 1152 left/right clock cycles in Single Speed, 2304 cycles in Double Speed and 4608 cycles in Quad Speed mode. The bias voltage on the outputs will be retained and MUTE_C will go low at the completion of the ramp period.

The analog outputs will ramp to a normal state when this function transitions from the enabled to disabled state. The ramp requires 1152 left/right clock cycles in Single Speed, 2304 cycles in Double Speed and 4608 cycles in Quad Speed mode. The MUTE_C will go high immediately on disabling of MUTE.

MUTE	MODE
0	Enabled
1	Disabled

Table 2.

3.3 MODE SELECT

Mode Control Register (address 01h)

7	6	5	4	3	2	1	0
CAL	<u>MUTE</u>	M4	M3	M2	M1	M0	PDN

Access:

R/W in I²C and SPI.

Default:

00000

Function:

The Mode Select pins determine the operational mode of the device as detailed in Tables 7-10. The options include:

Selection of the Digital Interface Format which determines the required relationship between the Left/Right clock, serial clock and serial data as detailed in Figures 20-23

Selection of the standard 15 µs/50 µs digital de-emphasis filter response, Figure 28, which requires re-configuration of the digital filter to maintain the proper filter response for 32, 44.1 or 48 kHz sample rates.

Selection of the appropriate clocking mode to match the input sample rates.

3.4 POWER DOWN

Mode Control Register (address 01h)

7	6	5	4	3	2	1	0
CAL	<u>MUTE</u>	M4	M3	M2	M1	M0	PDN

Access:

R/W in I²C and SPI.

Default:

1 - Powered Down

Function:

The analog and digital sections will be placed into a power-down mode when this function is enabled. This bit must be cleared to resume normal operation.

PDN	MODE
0	Disabled
1	Enabled

Table 3.

4.0 PIN DESCRIPTION

Reset	RST	1	28	VREF	Voltage Reference
See Description	M4(AD0/CS)	2	27	FILT+	Reference Filter
See Description	M3(AD1/CDIN)	3	26	FILT-	Reference Ground
See Description	M2(SCL/CCLK)	4	25	CMOUT	Common ModeS Voltage
See Description	M0(SDA/CDOUT)	5	24	AOUTL-	Differential Output
Digital Ground	DGND	6	23	AOUTL+	Differential Output
Digital Power	VD	7	22	VA	Analog Power
Digital Power	VD	8	21	AGND	Analog Ground
Digital Ground	DGND	9	20	AOUTR+	Differential Output
Master Clock	MCLK	10	19	AOUTR-	Differential Output
Serial Clock	SCLK	11	18	AGND	Analog Ground
Left/Right Clock	LRCK	12	17	<u>MUTEC</u>	Mute Control
Serial Data	SDATA	13	16	<u>C/H</u>	Control port/Hardware select
See Description	M1	14	15	<u>MUTE</u>	Soft Mute

Reset - RST

Pins 1, Input

Function:

The device enters a low power mode and all internal state machines registers are reset when low. When high, the device will be in a normal operation mode .

RST	DESCRIPTION
0	Enabled
1	Normal operation mode

Digital Ground - DGND

Pins 6 and 9, Inputs

Function:

Digital ground reference.

Digital Power - VD

Pins 7 and 8, Input

Function:

Digital power supply. Typically 5.0 to 3.0 VDC.

Master Clock - MCLK

Pin 10, Input

Function:

The master clock frequency must be either 256x, 384x, 512x or 768x the input sample rate in Single Speed Mode; either 128x, 192x 256x or 384x the input sample rate in Double Speed Mode; or 64x, 96x 128x or 192x the input sample rate in Quad Speed Mode. Tables 4-6 illustrate the standard audio sample rates and the required master clock frequencies.

Sample Rate (kHz)	MCLK (MHz)			
	256x	384x	512x	768x
32	8.1920	12.2880	16.3840	24.5760
44.1	11.2896	16.9344	22.5792	33.8688
48	12.2880	18.4320	24.5760	36.8640

Table 4. Single Speed (16 to 50 kHz sample rates) Common Clock Frequencies

Sample Rate (kHz)	MCLK (MHz)			
	128x	192x	256x	384x
64	8.1920	12.2880	16.3840	24.5760
88.2	11.2896	16.9344	22.5792	33.8688
96	12.2880	18.4320	24.5760	36.8640

Table 5. Double Speed (50 to 100 kHz sample rates) Common Clock Frequencies

Sample Rate (kHz)	MCLK (MHz)			
	64x	96x	128x	192x
176.4	11.2896	16.9344	22.5792	33.8688
192	12.2880	18.4320	24.5760	36.8640

Table 6. Quad Speed (100 to 200 kHz sample rates) Common Clock Frequencies**Serial Clock - SCLK***Pin 11, Input**Function:*

Clocks individual bits of serial data into the SDATA pin. The required relationship between the Left/Right clock, serial clock and serial data is defined by either the Mode Control Byte in Control Port Mode or the M0 - M4 pins in Hardware Mode. The options are detailed in Figures 20-23

Left/Right Clock - LRCK*Pin 12, Input**Function:*

The Left/Right clock determines which channel is currently being input on the serial audio data input, SDATA. The frequency of the Left/Right clock must be at the input sample rate. Audio samples in Left/Right sample pairs will be simultaneously output from the digital-to-analog converter whereas Right/Left pairs will exhibit a one sample period difference. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Mode Control Byte and the options are detailed in Figures 20-23

Serial Audio Data - SDATA*Pin 13, Input**Function:*

Two's complement MSB-first serial data is input on this pin. The data is clocked into SDATA via the serial clock and the channel is determined by the Left/Right clock. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Mode Control Byte and the options are detailed in Figures 20-23

Soft Mute - MUTE*Pin 15, Input**Function:*

The analog outputs will ramp to a muted state when enabled. The ramp requires 1152 left/right clock cy-

cles in Single Speed, 2304 cycles in Double Speed and 4608 cycles in Quad Speed mode. The bias voltage on the outputs will be retained and MUTEC will go active at the completion of the ramp period.

The analog outputs will ramp to a normal state when this function transitions from the enabled to disabled state. The ramp requires 1152 left/right clock cycles in Single Speed, 2304 cycles in Double Speed and 4608 cycles in Quad Speed mode. The MUTEC will release immediately on setting MUTE = 1.

The converter analog outputs will mute when enabled. The bias voltage on the outputs will be retained and MUTEC will go active during the mute period.

Mute	DESCRIPTION
0	Enabled
1	Normal operation mode

Control Port / Hardware Mode Select - C/H

Pin 16, Input

Function:

Determines if the device will operate in either the Hardware Mode or Control Port Mode.

C/H	DESCRIPTION
0	Hardware Mode Enabled
1	Control Port Mode Enabled

Mute Control - MUTEC

Pin 17, Output

Function:

The Mute Control pin goes low during power-up initialization, reset, muting, master clock to left/right clock frequency ratio is incorrect or power-down. This pin is intended to be used as a control for an external mute circuit to prevent the clicks and pops that can occur in any single supply system. Use of Mute Control is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops.

Analog Ground - AGND

Pins 18 and 21, Inputs

Function:

Analog ground reference.

Differential Analog Outputs - AOUTR- , AOUTR+ and AOUTL- , AOUTL+

Pins 19, 20, 23 and 24, Outputs

Function:

The full scale differential analog output level is specified in the Analog Characteristics specifications table.

Analog Power - VA

Pin 22, Input

Function:

Power for the analog and reference circuits. Typically 5VDC.

Common Mode Voltage - CMOUT*Pin 25, Output**Function:*

Filter connection for internal bias voltage, typically 50% of VREF. Capacitors must be connected from CMOUT to analog ground, as shown in Figure 4. CMOUT has a typical source impedance of 25 kΩ and any current drawn from this pin will alter device performance

Reference Ground - FILT-*Pin 26, Input**Function:*

Ground reference for the internal sampling circuits. Must be connected to analog ground.

Reference Filter - FILT+*Pin 27, Output**Function:*

Positive reference for internal sampling circuits. External capacitors are required from FILT+ to analog ground, as shown in Figure 4. The recommended values will typically provide 60 dB of PSRR at 1 kHz and 40 dB of PSRR at 120 Hz. FILT+ is not intended to supply external current.

Voltage Reference Input- VREF*Pin 28, Input**Function:*

Analog voltage reference. Typically 5VDC.

HARDWARE MODE**Mode Select - M0, M1, M2, M3, M4***Pins 2, 3, 4, 5 and 14, Inputs**Function:*

The Mode Select pins determine the operational mode of the device as detailed in Tables 7-10. The options include;

Selection of the Digital Interface Format which determines the required relationship between the Left/Right clock, serial clock and serial data as detailed in Figures 20-23

Selection of the standard 15 µs/50 µs digital de-emphasis filter response, Figure 28, which requires re-configuration of the digital filter to maintain the proper filter response for 32, 44.1 or 48 kHz sample rates.

Selection of the appropriate clocking mode to match the input sample rates.

CONTROL PORT MODE**Address Bit 0 / Chip Select - AD0 / \overline{CS}** *Pin 2, Input**Function:*

In I²C mode, AD0 is a chip address bit. \overline{CS} is used to enable the control port interface in SPI mode. The device will enter the SPI mode at anytime a high to low transition is detected on this pin. Once the device has entered the SPI mode, it will remain until either the part is reset or undergoes a power-down cycle.

Address Bit 1 / Control Data Input - AD1/CDIN

Pin 3, Input

Function:

In I²C mode, AD1 is a chip address bit. CDIN is the control data input line for the control port interface in SPI mode.

Serial Control Interface Clock - SCL/CCLK

Pin 4, Input

Function:

In I²C mode, SCL clocks the serial control data into or from SDA/CDOUT.

In SPI mode, CCLK clocks the serial data into AD1/CDIN and out of SDA/CDOUT.

Serial Control Data I/O - SDA/CDOUT

Pin 5, Input/Output

Function:

In I²C mode, SDA is a data input/output. CDOUT is the control data output for the control port interface in SPI mode.

M1 - Mode Select

Pin 14, Input

Function:

This pin is not used in Control Port Mode and must be terminated to ground.

5.0 APPLICATIONS

5.1 Recommended Power-up Sequence

1. Hold $\overline{\text{RST}}$ low until the power supplies, master, and left/right clocks are stable.
2. Bring $\overline{\text{RST}}$ high.

6.0 CONTROL PORT INTERFACE

The control port is used to load all the internal settings of the CS4396. The operation of the control port may be completely asynchronous to the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has 2 modes: SPI and I²C, with the CS4396 operating as a slave device in both modes. If I²C operation is desired, AD0/CS should be tied to VD or DGND. If the CS4396 ever detects a high to low transition on AD0/CS after power-up, SPI mode will be selected.

6.1 SPI Mode

In SPI mode, CS is the CS4396 chip select signal, CCLK is the control port bit clock, CDIN is the input data line from the microcontroller, CDOUT is the data output and the chip address is 0010000. The data is clocked on the rising edge of CCLK.

Figure 5 shows the operation of the control port in SPI mode. To write to a register, bring CS low. The first 7 bits on CDIN form the chip address, and must be 0010000. The eighth bit is a read/write indicator (R/W). The next 8 bits form the Memory Address Pointer (MAP), which is set to 01h. The next 8 bits are the data which will be placed into the register designated by the MAP.

6.2 I²C Mode

In I²C mode, SDA is a bi-directional data line. Data is clocked into and out of the part by the clock, SCL, with the clock to data relationship as shown in Figure 2. There is no CS pin. Pins AD0 and AD1 form the partial chip address and should be tied to VD or DGND as required. The 7-bit address field, which is the first byte sent to the CS4396, must be 00100(AD1)(AD0) where (AD1) and (AD0) match the setting of the AD0 and AD1 pins. The eighth bit of the address byte is the R/W bit (high for a read, low for a write). If the operation is a write, the next byte is the Memory Address Pointer, MAP, which selects the register to be read or written. The MAP is then followed by the data to be written. If the operation is a read, then the contents of the register pointed to by the MAP will be output after the chip address.

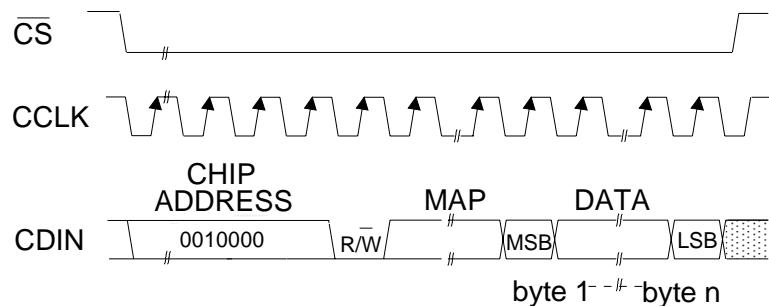
For more information on I²C, please see “The I²C-Bus Specification: Version 2.0”, listed in the References section.

Memory Address Pointer (MAP)

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	Reserved	MAP2	MAP1	MAP0

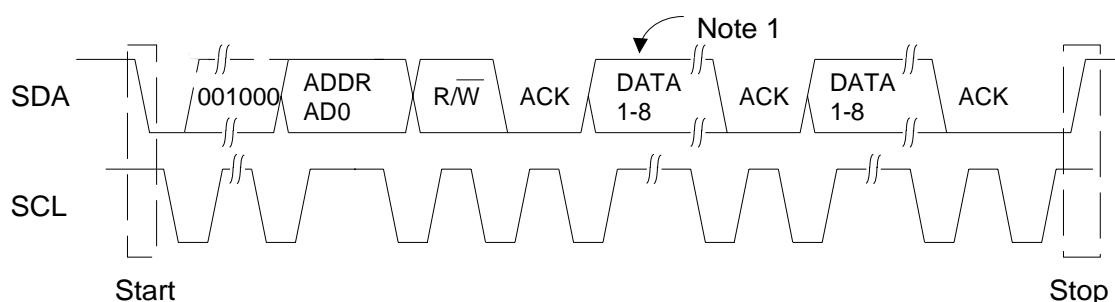
INCR (Auto MAP Increment Enable)
Default = '0'
0 - Disabled
1 - Enabled

MAP0-2 (Memory Address Pointer)
Default = '001'



MAP = Memory Address Pointer = 0

Figure 5. Control Port Timing, SPI mode



Note: If operation is a write, this byte contains the Memory Address Pointer, MAP.

Figure 6. Control Port Timing, I²C Mode

M4	M1 (DIF1)	M0 (DIF0)	DESCRIPTION	FORMAT	FIGURE
0	0	0	Left Justified, up to 24-bit data	0	20
0	0	1	I ² S, up to 24-bit data	1	21
0	1	0	Right Justified, 16-bit Data	2	22
0	1	1	Right Justified, 24-bit Data	3	23

Table 7. Single Speed (16 to 50 kHz) Digital Interface Format Options

M4	M3 (DEM1)	M2 (DEM0)	DESCRIPTION	FIGURE
0	0	0	32 kHz De-Emphasis	19
0	0	1	44.1 kHz De-Emphasis	19
0	1	0	48 kHz De-Emphasis	19
0	1	1	De-Emphasis Disabled	-

Table 8. Single Speed (16 to 50 kHz) De-Emphasis Options

M4	M3	M2	M1	M0	DESCRIPTION
1	1	1	0	0	Left Justified up to 24-bit data, Format 0
1	1	1	0	1	I ² S up to 24-bit data, Format 1
1	1	1	1	0	Right Justified 16-bit data, Format 2
1	1	1	1	1	Right Justified 24-bit data, Format 3

Table 9. Double Speed (50 to 100 kHz) Sample Rate Mode Options

M4	M3	M2	M1	M0	DESCRIPTION
1	1	0	0	0	Left Justified up to 24-bit data, Format 0
1	1	0	0	1	I ² S up to 24-bit data, Format 1
1	1	0	1	0	Right Justified 16-bit data, Format 2
1	1	0	1	1	Right Justified 24-bit data, Format 3

Table 10. Quad (100 to 200 kHz) Sample Rate Mode Options

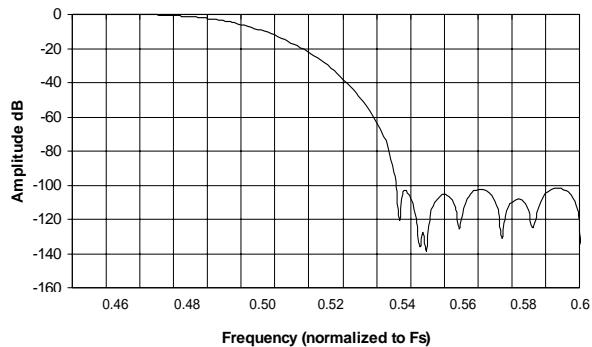


Figure 7. Single-speed Transition Band

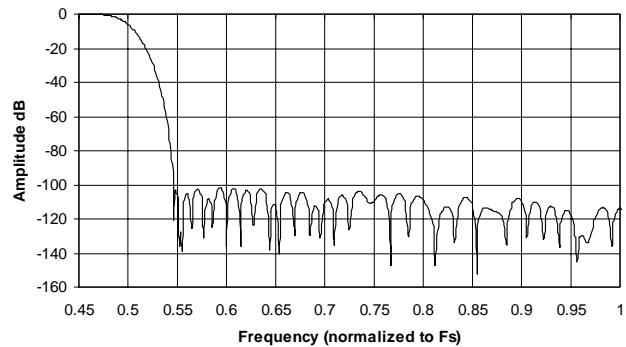


Figure 8. Single-speed Stopband Rejection

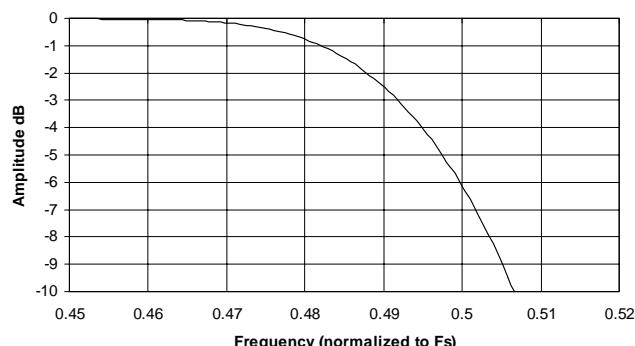


Figure 9. Single-speed Transition Band

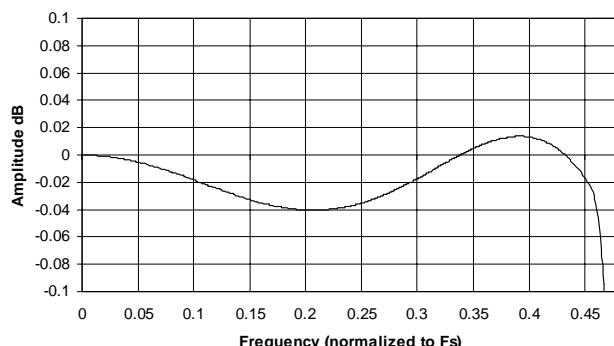


Figure 10. Single-speed Frequency Response

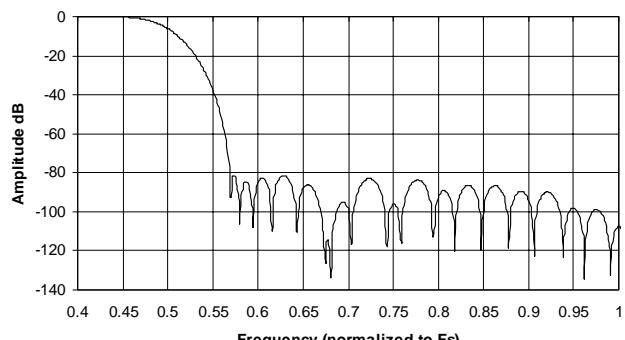


Figure 11. Double-speed Stopband

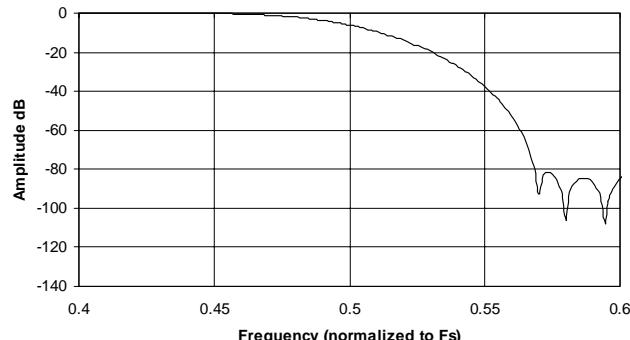


Figure 12. Double-speed Transition Band

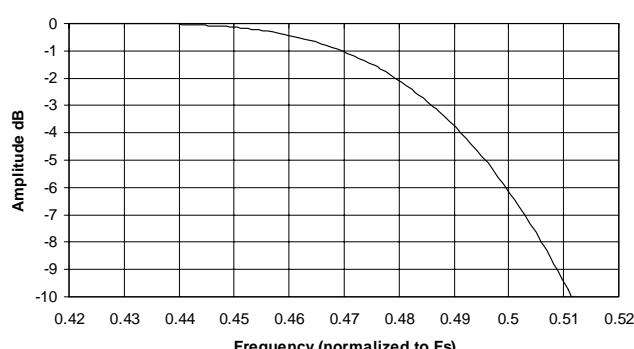


Figure 13. Double-speed Transition Band

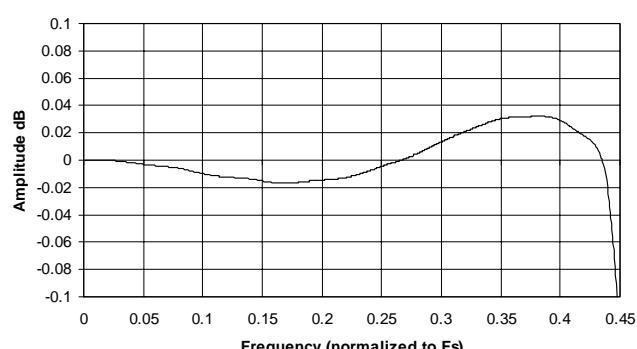


Figure 14. Double-speed Frequency Response

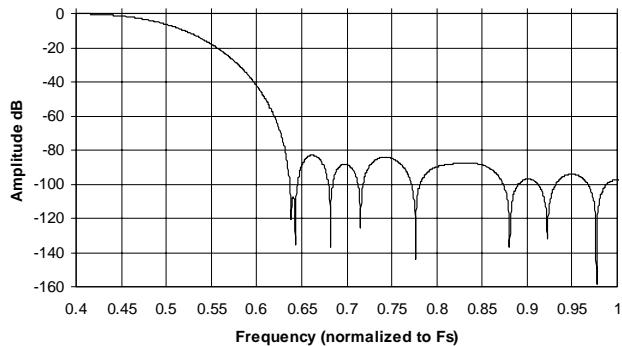


Figure 15. Quad-speed Stopband Rejection

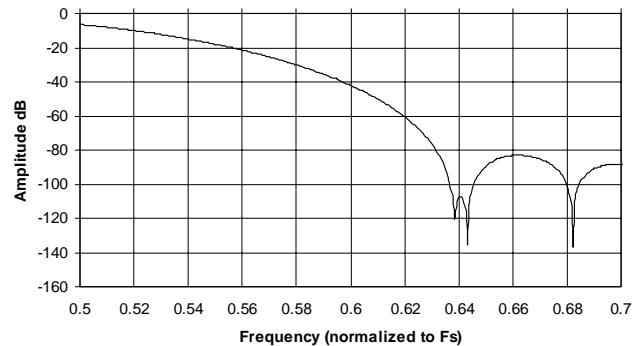


Figure 16. Quad-speed Transition Band

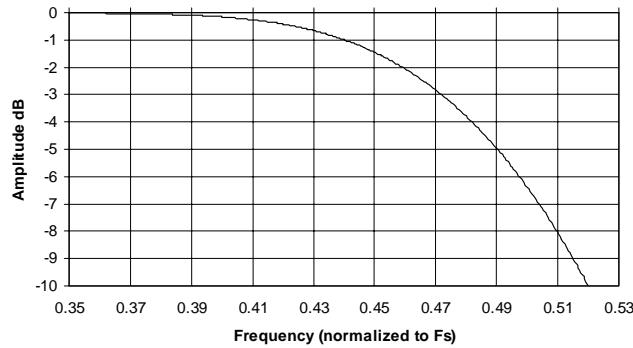


Figure 17. Quad-speed Transition Band

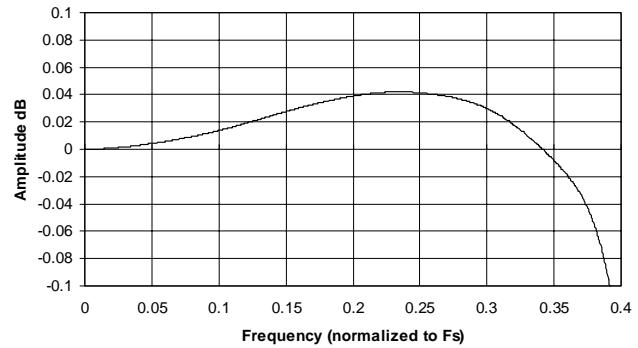


Figure 18. Quad-speed Frequency Response

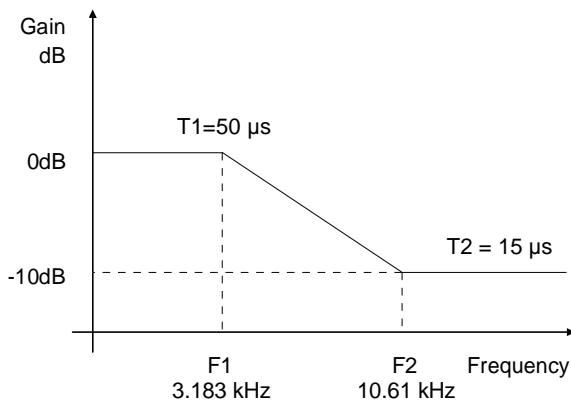


Figure 19. De-Emphasis Curve

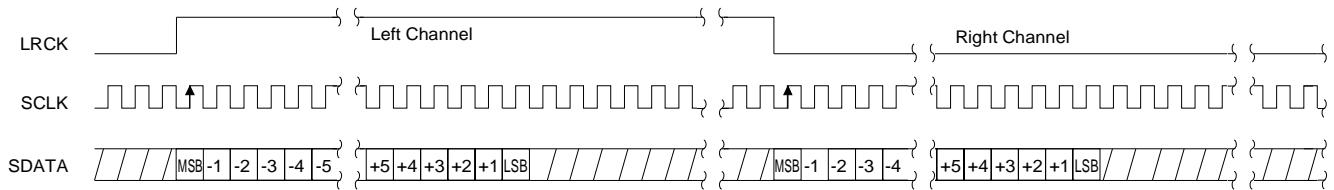


Figure 20. Format 0, Left Justified

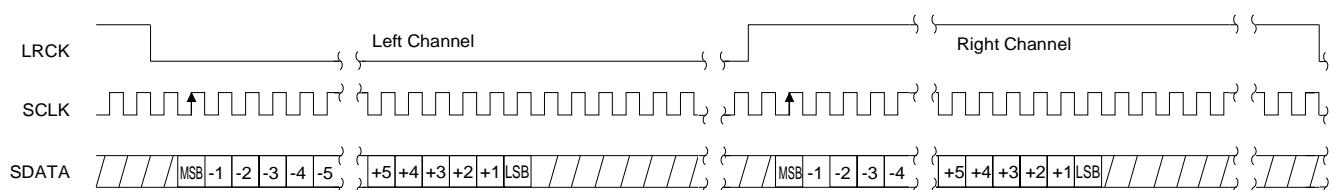


Figure 21. Format 1, I²S

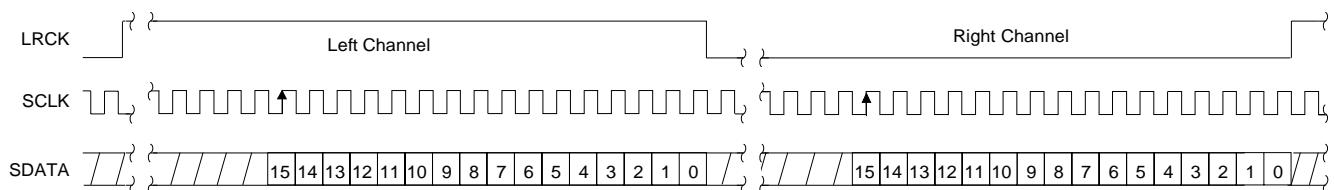


Figure 22. Format 2, Right Justified, 16-Bit Data

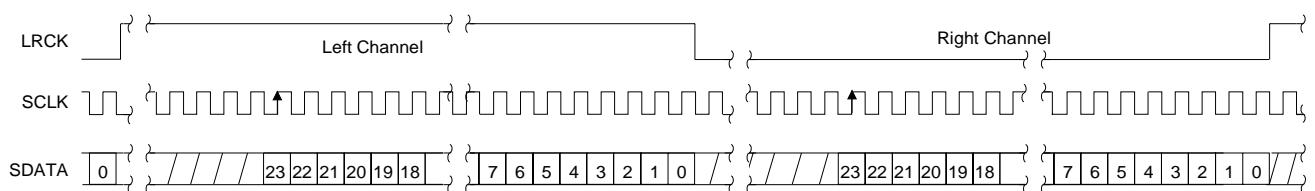


Figure 23. Format 3, Right Justified, 24-Bit Data

7.0 PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10Hz to 20kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full scale analog output for a full scale digital input.

Gain Drift

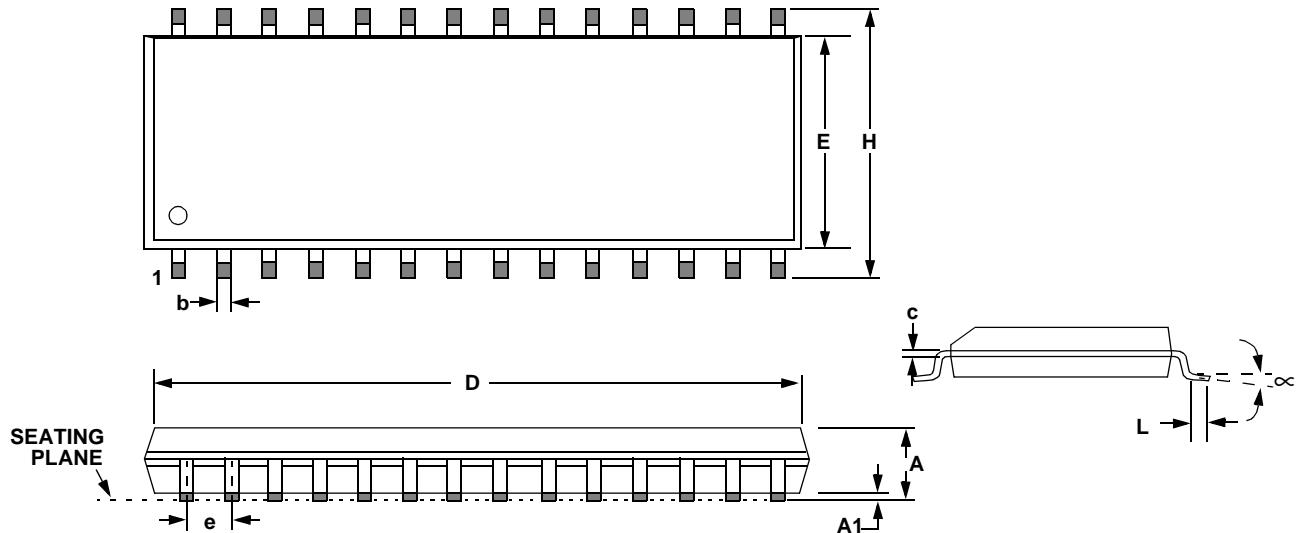
The change in gain value with temperature. Units in ppm/°C.

8.0 REFERENCES

- 1) "How to Achieve Optimum Performance from Delta-Sigma A/D & D/A Converters" by Steven Harris. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.
- 2) CDB4397 Evaluation Board Datasheet
- 3) "The I²C-Bus Specification: Version 2.0" Philips Semiconductors, December 1998.
<http://www.semiconductors.philips.com>

9.0 PACKAGE DIMENSIONS

28L SOIC (300 MIL BODY) PACKAGE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.697	0.713	17.70	18.10
E	0.29G10	0.299	7.40	7.60
	1			
e	0.040	0.060	1.02	1.52
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
∞	0°	8°	0°	8°

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