CIRRUS LOGIC®

CS8952

CrystalLAN™ 100BASE-X and 10BASE-T Transceiver

Features

- Single-Chip IEEE 802.3 Physical Interface IC for 100BASE-TX, 100BASE-FX and 10BASE-T
- Adaptive Equalizer provides Extended Length Operation (>160 m) with Superior Noise Immunity and NEXT Margin
- Extremely Low Transmit Jitter (<400 ps)
- Low Common Mode Noise on TX Driver for Reduced EMI Problems
- Integrated RX and TX Filters for 10BASE-T
- Compensation for Back-to-Back “Killer Packets”
- Digital Interfaces Supported
  - Media Independent Interface (MII) for 100BASE-X and 10BASE-T
  - Repeater 5-bit code-group interface (100BASE-X)
  - 10BASE-T Serial Interface
- Register Set Compatible with DP83840A
- IEEE 802.3 Auto-Negotiation with Next Page Support
- Six LED drivers (LNK, COL, FDX, TX, RX, and SPD)
- Low power (135 mA Typ) CMOS design operates on a single 5 V supply

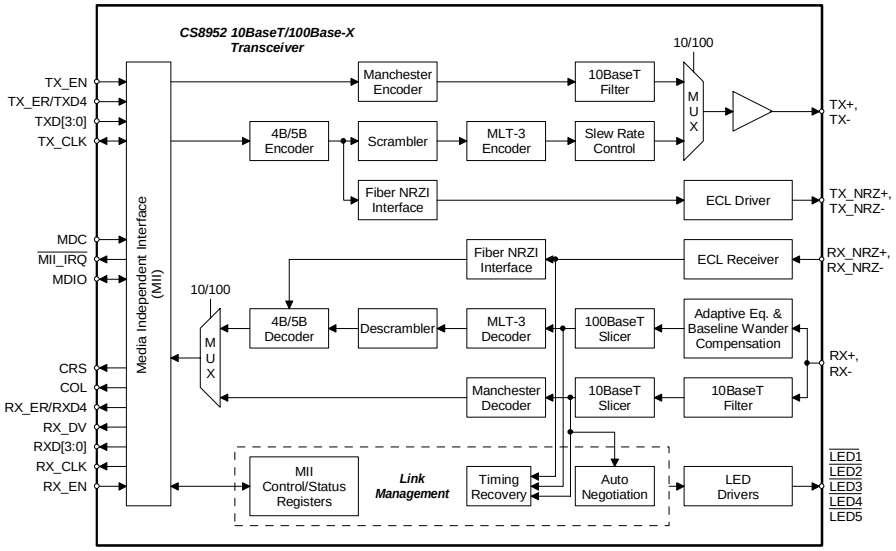
Description

The CS8952 uses CMOS technology to deliver a high-performance, low-cost 100BASE-X/10BASE-T Physical Layer (PHY) line interface. It makes use of an adaptive equalizer optimized for noise and near end crosstalk (NEXT) immunity to extend receiver operation to cable lengths exceeding 160 m. In addition, the transmit circuitry has been designed to provide extremely low transmit jitter (<400 ps) for improved link partner performance. Transmit driver common mode noise has been minimized to reduce EMI for simplified FCC certification.

The CS8952 incorporates a standard Media Independent Interface (MII) for easy connection to a variety of 10 and 100 Mb/s Media Access Controllers (MACs). The CS8952 also includes a pseudo-ECL interface for use with 100Base-FX fiber interconnect modules.

ORDERING INFORMATION

CS8952-CQ	0 to 70 °C	100-pin TQFP
CDB8952		Evaluation Board



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

CIRRUS LOGIC®
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.cirrus.com

TABLE OF CONTENTS

Contacting Cirrus Logic Support

For a complete listing of Direct Sales, Distributor, and Sales Representative contacts, visit the Cirrus Logic web site at:
http://www.cirrus.com/corporate/contacts/sales.cfm

1. SPECIFICATIONS AND CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (AVSS, DVSS = 0 V, all voltages with respect to 0 V.)

Parameter	Symbol	Min	Max	Unit
Power Supply	V_{DD} V_{DD_MII}	-0.3 -0.3	6.0 6.0	V
Input Current Except Supply Pins		-	+/-10.0	mA
Input Voltage		-0.3	V_{DD} + 0.3	V
Ambient Temperature Power Applied		-55	+125	°C
Storage Temperature		-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AVSS, DVSS = 0 V, all voltages with respect to 0 V.)

Parameter	Symbol	Min	Max	Unit
Power Supply Core MII	V_{DD} V_{DD_MII}	4.75 3.0	5.25 5.25	V V
Operating Ambient Temperature	T_A	0	70	°C

QUARTZ CRYSTAL REQUIREMENTS (If a 25 MHz quartz crystal is used, it must meet the following specifications.)

Parameter	Min	Typ	Max	Unit
Parallel Resonant Frequency	-	25.0	-	MHz
Resonant Frequency Error (CL = 15 pF)	-50	-	+50	ppm
Resonant Frequency Change Over Operating Temperature	-40	-	+40	ppm
Crystal Load Capacitance	-	15	-	pF
Motional Crystal Capacitance	-	0.021	-	pF
Series Resistance	-	-	18	Ω
Shunt Capacitance	-	-	7	pF

DC CHARACTERISTICS (Over recommended operating conditions)

Parameter	Symbol	Min	Typ	Max	Unit
External Oscillator					
XTAL_I Input Low Voltage	V_{IXH}	-0.3	-	0.5	V
XTAL_I Input High Voltage	V_{IXH}	3.5	-	VDD+0.5	V
XTAL_I Input Low Current	I_{IXL}	-40	-	-	µA
XTAL_I Input High Current	I_{IXH}	-	-	40	µA
XTAL_I Input Capacitance	C_L		-	35	pF
XTAL_I Input Cycle Time	t_{IXC}	39.996	-	40.004	ns
XTAL_I Input Low Time	t_{IXL}	18	-	22	ns
XTAL_I Input High Time	t_{XH}	18	-	22	ns
Power Supply					
Power Supply Current 100BASE-TX (Note **1**) 100BASE-FX (Note **1**) 10BASE-T (Note **1**)	I_{DD}	- - -	135 90 80	145 - -	mA
Hardware Power-Down (Note **1**)	I_{DDHPDN}	-	900	-	µA
Software Power-Down (Note **1**)	I_{DDSPDN}	-	20	-	mA
Low Power Power-Up (Note **1**)	$I_{DDSLPUP}$	-	900	-	µA
Digital I/O					
Output Low Voltage CLK25, $\overline{\text{MII\_IRQ}}$, SPD10, SPD100 I_{OL} = 4.0mA LED[4:0] I_{OL} = 10.0mA	V_{OL}	 - -	 - -	 0.4 0.4	V
Output Low Voltage (MII_DRV = 1) COL, CRS, MDIO, RXD[3:0], RX_CLK, RX_DV, RX_ER, TX_CLK I_{OL} = 4.0mA VDD_MII = 5V; I_{OL} = 43.0mA VDD_MII = 3.3V, I_{OL} = 26.0mA	V_{OL}	 - - -	 - - -	 0.4 3.05 2.1	V
Output Low Voltage (MII_DRV = 0) COL, CRS, MDIO, RXD[3:0], RX_CLK, RX_DV, RX_ER, TX_CLK I_{OL} = 4.0mA	V_{OL}	 -	 -	 0.4	V
Output High Voltage CLK25, SPD10, SPD100 I_{OH} = -4.0mA	V_{OH}	 2.4	 -	 -	V
Output High Voltage (MII_DRV = 1) COL, CRS, MDIO, RXD[3:0], RX_CLK, RX_DV, RX_ER, TX_CLK I_{OH}= -4.0mA VDD_MII = 5V; I_{OH} = -20.0mA VDD_MII = 3.3V, I_{OH} = -20.0mA	V_{OH}	 2.4 1.1 1.1	 - - -	 - - -	V

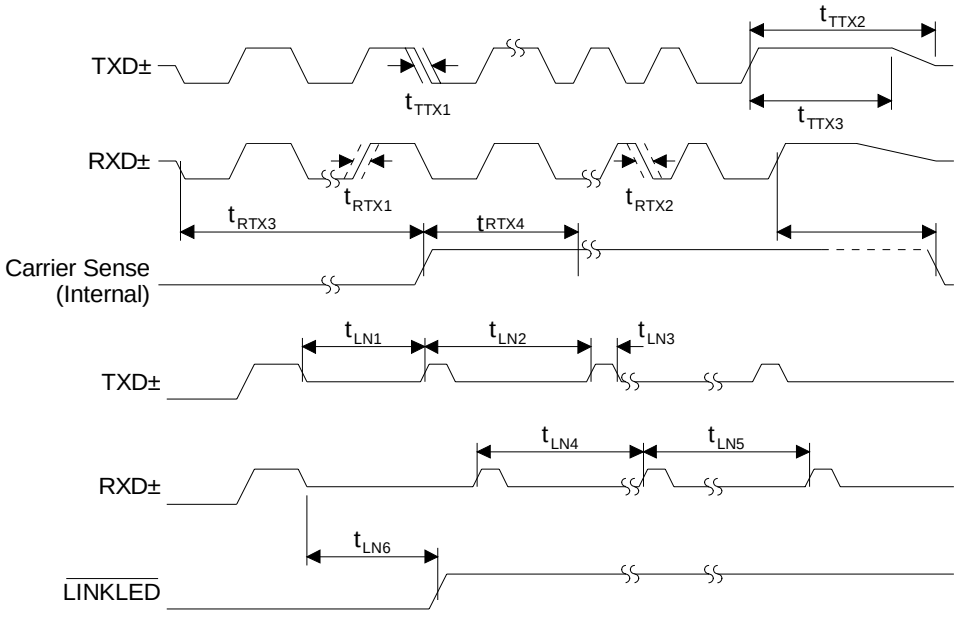
DC CHARACTERISTICS *(CONTINUED)* (Over recommended operating conditions)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (MII_DRV = 0) COL, CRS, MDIO, RXD[3:0], RX_CLK, RX_DV, RX_ER, TX_CLK I_{OH} = -4.0mA	V_{OH}	2.4	-	-	V
Input Low Voltage All Inputs Except AN[1:0], TCM, TXSLEW[1:0]	V_{IL}	-	-	0.8	V
Input High Voltage All Inputs Except AN[1:0], TCM, TXSLEW[1:0]	V_{IH}	2.0	-	-	V
Tri-Level Input Voltages AN[1:0], TCM, TXSLEW[1:0]	V_{IL}	-	-	1/3 V_{DD_MII} - 20%	V
	V_{IM}	1/3 V_{DD_MII} + 20%	-	2/3 V_{DD_MII} - 20%	
	V_{IH}	2/3 V_{DD_MII} + 20%	-	-	
Input Low Current MDC, TXD[3:0], TX_CLK, TX_EN, TX_ER V_I = 0.0V	I_{IL}	-20	-	-	µA
MDIO V_I = 0.0V		-3800	-	-	
Input High Current MDC, TXD[3:0], TX_CLK, TX_EN, TX_ER V_I = 5.0V	I_{IH}	-	-	200	µA
MDIO V_I = 5.0V		-	-	20	
Input Leakage Current All Other Inputs 0<=V<=V_{DD}	I_{LEAK}	-10	-	+10	µA

Notes: 1. With digital outputs connected to CMOS loads.

10BASE-T CHARACTERISTICS

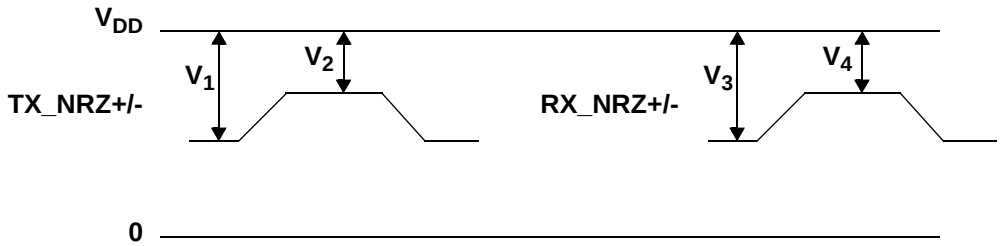
Parameter	Symbol	Min	Typ	Max	Unit
10BASE-T Interface					
Transmitter Differential Output Voltage (Peak)	V_{OD}	2.2	-	2.8	V
Receiver Normal Squelch Level (Peak)	V_{ISQ}	300	-	525	mV
Receiver Low Squelch Level (LoRxSquelch bit set)	V_{SQL}	125	-	290	mV
10BASE-T Transmitter					
TXD Pair Jitter into 100 Ω Load	t_{TTX1}	-	-	8	ns
TXD Pair Return to ≤50 mV after Last Positive Transition	t_{TTX2}	-	-	4.5	µs
TXD Pair Positive Hold Time at End of Packet	t_{TTX3}	250	-	-	ns
10BASE-T Receiver					
Allowable Received Jitter at Bit Cell Center	t_{TRX1}	-	-	+/-13.5	ns
Allowable Received Jitter at Bit Cell Boundary	t_{TRX2}	-	-	+/-13.5	ns
10BASE-T Link Integrity					
First Transmitted Link Pulse after Last Transmitted Packet	t_{LN1}	15	16	17	ms
Time Between Transmitted Link Pulses	t_{LN2}	15	16	17	ms
Width of Transmitted Link Pulses	t_{LN3}	60	-	200	ns
Minimum Received Link Pulses Separation	t_{LN4}	2	5	7	ms
Maximum Received Link Pulse Separation	t_{LN5}	25	52	150	ms
Last Receive Activity to Link Fail (Link Loss Timer)	t_{LN6}	50	52	150	ms
10Base-T Jabber/Unjabber Timing					
Maximum Transmit Time		-	105	-	ms
Unjabber Time		-	406	-	ms



100BASE-X CHARACTERISTICS

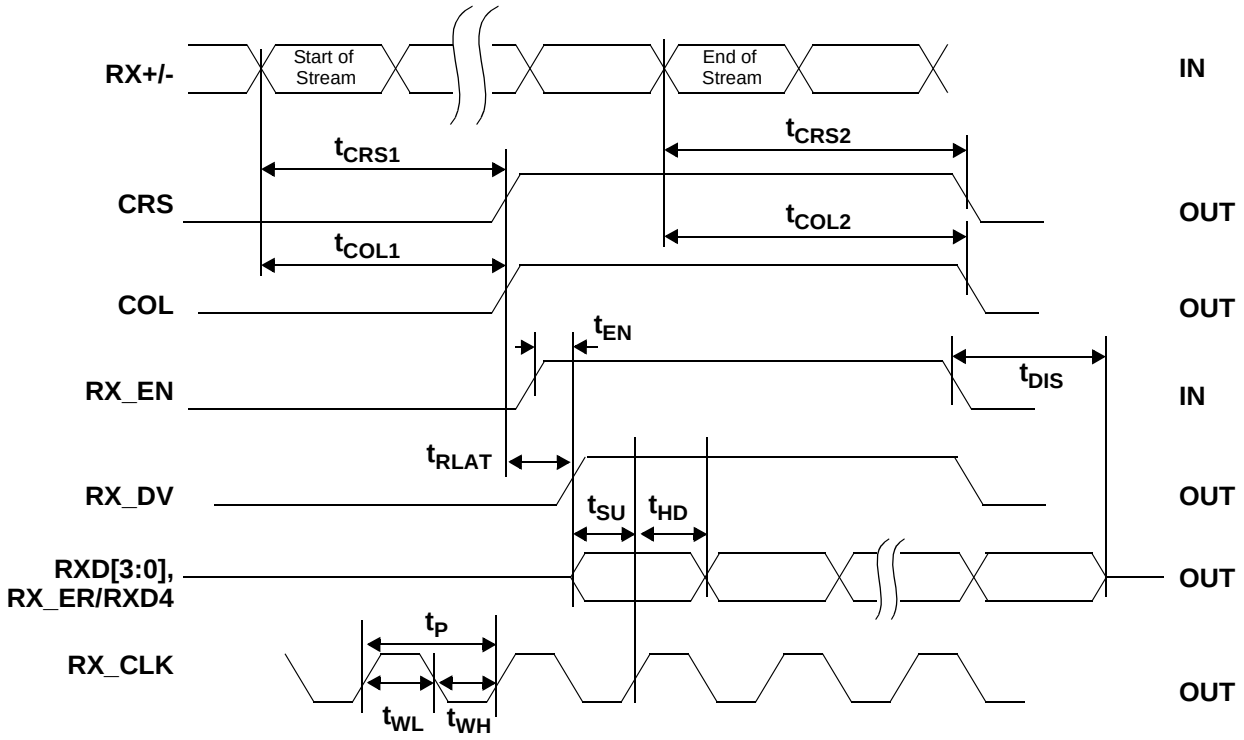
Parameter	Symbol	Min	Typ	Max	Unit
100BASE-TX Transmitter					
TX Differential Output Voltage (Peak)	V_{OP}	0.95	-	1.05	V
Signal Amplitude Symmetry	V_{SYM}	98	-	102	%
Signal Rise/Fall Time	t_{RF}	3.0	-	5.0	ns
Rise/Fall Symmetry	t_{RFS}	-	-	0.5	ns
Duty Cycle Distortion	t_{DCD}	-	-	+/-0.5	ns
Overshoot/Undershoot	t_{OS}	-	-	5	%
Transmit Jitter	t_{JT}	-	400	1400	ps
TX Differential Output Impedance	Z_{OUT}	-	100	-	ohms
100BASE-TX Receiver					
Receive Signal Detect Assert Threshold		-	-	1.0	V_{p-p}
Receive Signal Detect De-assert Threshold		0.2	-	-	V_{p-p}
Receive Signal Detect Assert Time		-	-	1000	µs
Receive Signal Detect De-assert Time		-	-	350	µs
100BASE-FX Transmitter					
TX_NRZ+/- Output Voltage - Low	V_1	-1.830	-	-1.605	V
TX_NRZ+/- Output Voltage - High	V_2	-1.035	-	-0.880	V
Signal Rise/Fall Time	T_{RF}	-	-	1.6	ns
100Base-FX Receiver					
RX_NRZ+/- Input Voltage - Low	V_3	-1.830	-	-1.605	V
RX_NRZ+/- Input Voltage - High	V_4	-1.035	-	-0.880	V
Common Mode Input Range	V_{CMIP}	-	3.56	-	V

RX/TX Signaling for 100Base-FX



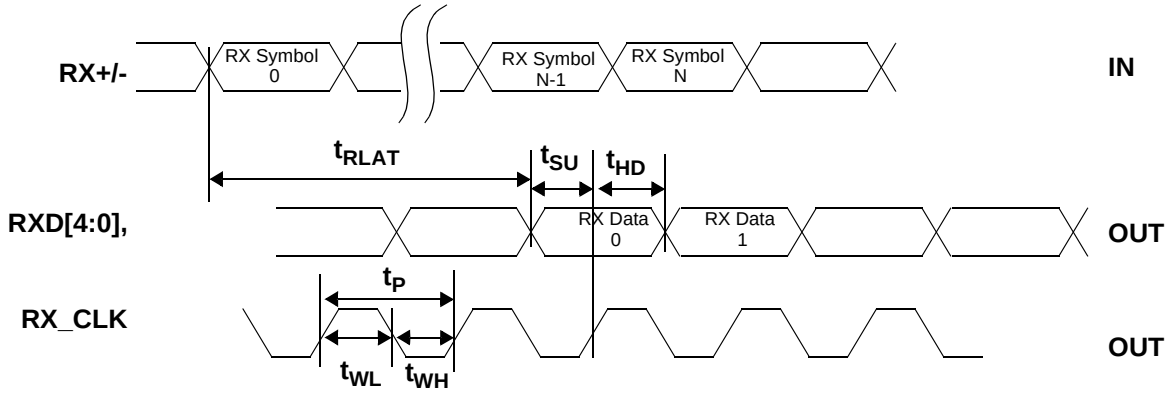
100BASE-TX MII RECEIVE TIMING - 4B/5B ALIGNED MODES

Parameter	Symbol	Min	Typ	Max	Unit
RX_CLK Period	t_P	-	40	-	ns
RX_CLK Pulse Width	t_{WL}, t_{WH}	-	20	-	ns
RXD[3:0],RX_ER/RXD4,RX_DV setup to rising edge of RX_CLK	t_{SU}	10	-	-	ns
RXD[3:0],RX_ER/RXD4,RX_DV hold from rising edge of RX_CLK	t_{HD}	10	-	-	ns
CRS to RXD latency 4B Aligned 5B Aligned	t_{DLAT}	2 2	3 - 6 3 - 6	8 8	BT
“Start of Stream” to CRS asserted	t_{CRS1}	-	10	11	BT
“End of Stream” to CRS de-asserted	t_{CRS2}	-	-	21	BT
“Start of Stream” to COL asserted	t_{COL1}	-	-	11	BT
“End of Stream” to COL de-asserted	t_{COL2}	-	-	21	BT
RX_EN asserted to RX_DV, RXD[3:0] valid	t_{EN}	-	TBD	-	ns
RX_EN de-asserted to RX_DV, RXD[3:0]. RX_ER/RXD4 in high impedance state	t_{DIS}	-	TBD	-	ns



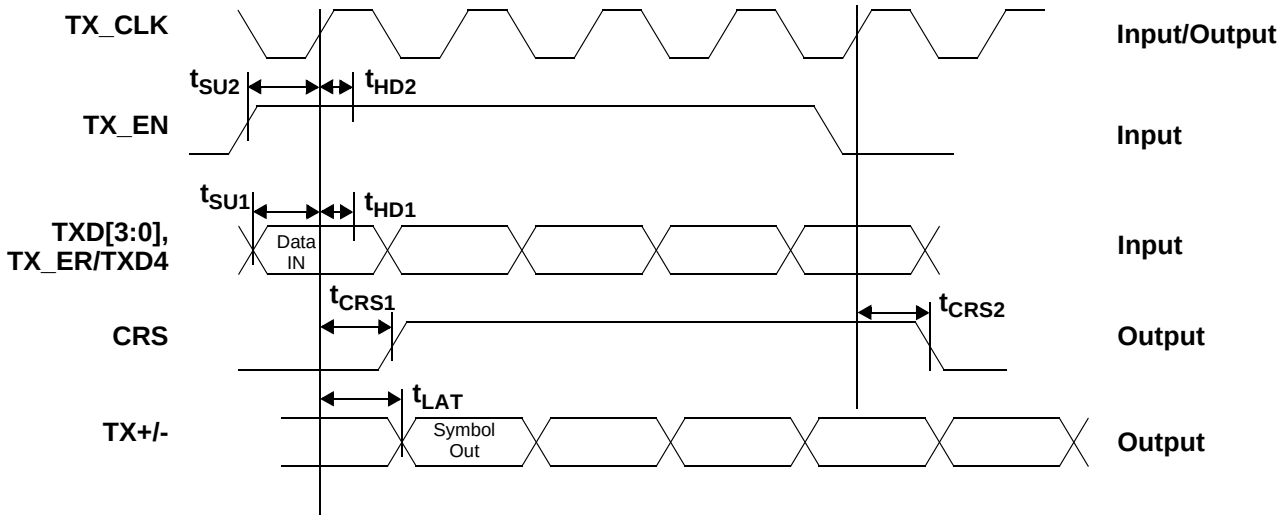
100BASE-TX MII RECEIVE TIMING - 5B BYPASS ALIGN MODE

Parameter	Symbol	Min	Typ	Max	Unit
RX_CLK Period	t_P	-	40	-	ns
RX_CLK Pulse Width	t_{WL}, t_{WH}	-	20	-	ns
RXD[4:0] setup to rising edge of RX_CLK	t_{SU}	10	-	-	ns
RXD[4:0] hold after rising edge of RX_CLK	t_{HD}	10	-	-	ns
Start of 5B symbol to symbol output on RX[4:0] 5B Mode	t_{RLAT}	5	-	9	BT



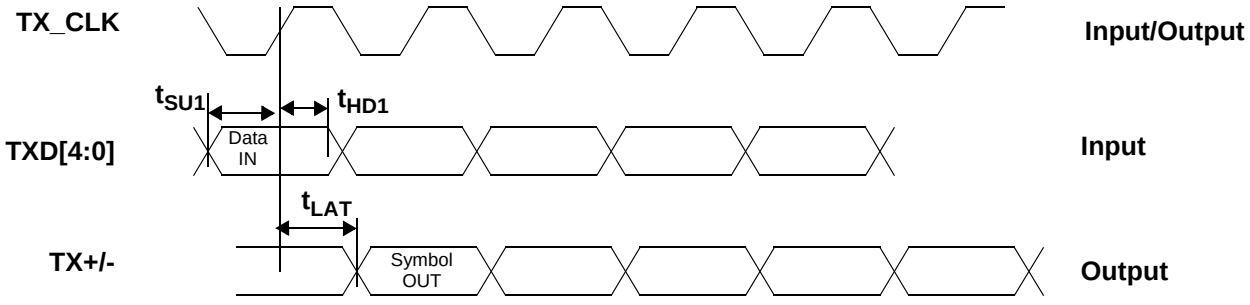
100BASE-TX MII TRANSMIT TIMING - 4B/5B ALIGN MODES

Parameter	Symbol	Min	Typ	Max	Unit
TXD[3:0] Setup to TX_CLK High	t_{SU1}	10	-	-	ns
TX_EN Setup to TX_CLK High	t_{SU2}	10	-	-	ns
TXD[3:0] Hold after TX_CLK High	t_{HD1}	0	-	-	ns
TX_ER Hold after TX_CLK High	t_{HD2}	0	-	-	ns
TX_EN Hold after TX_CLK High	t_{HD3}	0	-	-	ns
TX_EN “high” to CRS asserted latency	t_{CRS1}	-		8	BT
TX_EN “low” to CRS de-asserted latency	t_{CRS2}	-		8	BT
TX_EN “high” to TX+/- output (TX Latency)	t_{LAT}	6	7	8	BT



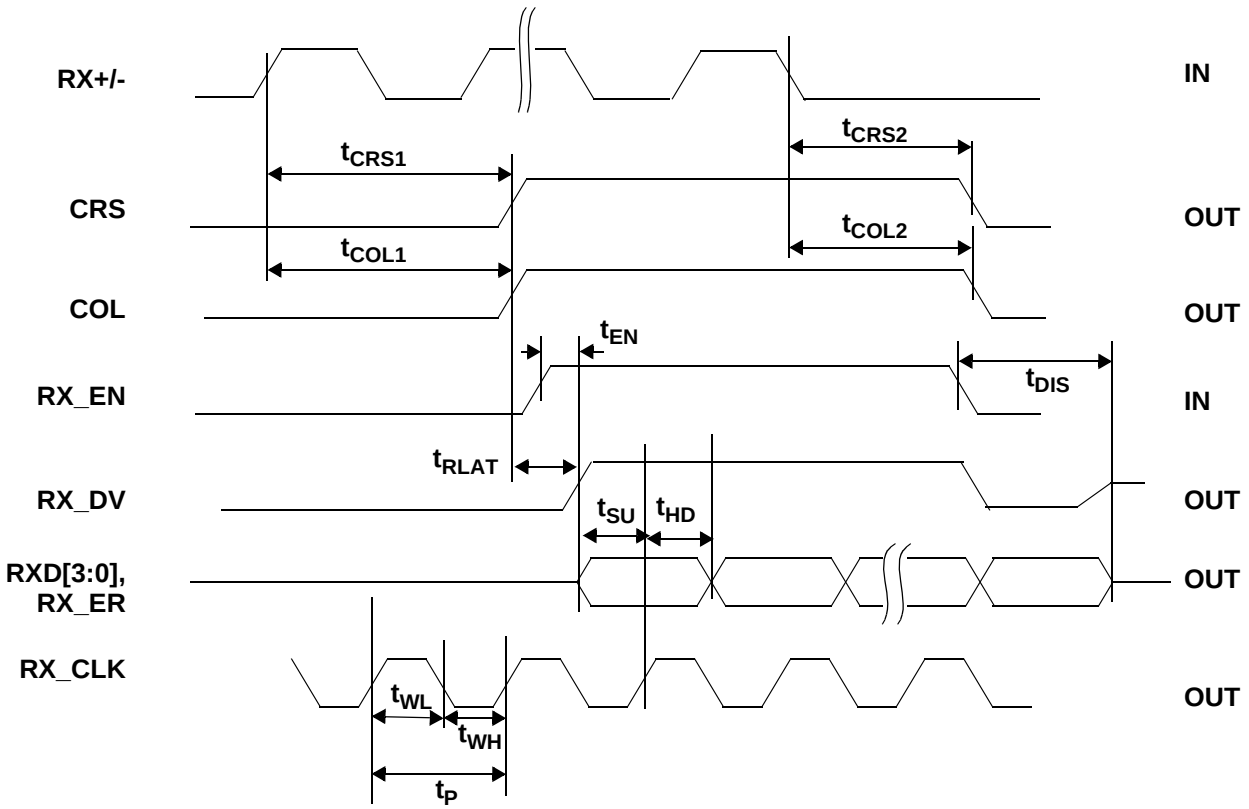
100BASE-TX MII TRANSMIT TIMING - 5B BYPASS ALIGN MODE

Parameter	Symbol	Min	Typ	Max	Unit
TXD[4:0] Setup to TX_CLK High	t_{SU1}	10	-	-	ns
TXD[4:0] Hold after TX_CLK High	t_{HD1}	0	-	-	ns
TX_ER Hold after TX_CLK High	t_{HD2}	0	-	-	ns
TXD[4:0] Sampled to TX+/- output (TX Latency)	t_{LAT}	-	6	7	ns



10BASE-T MII RECEIVE TIMING

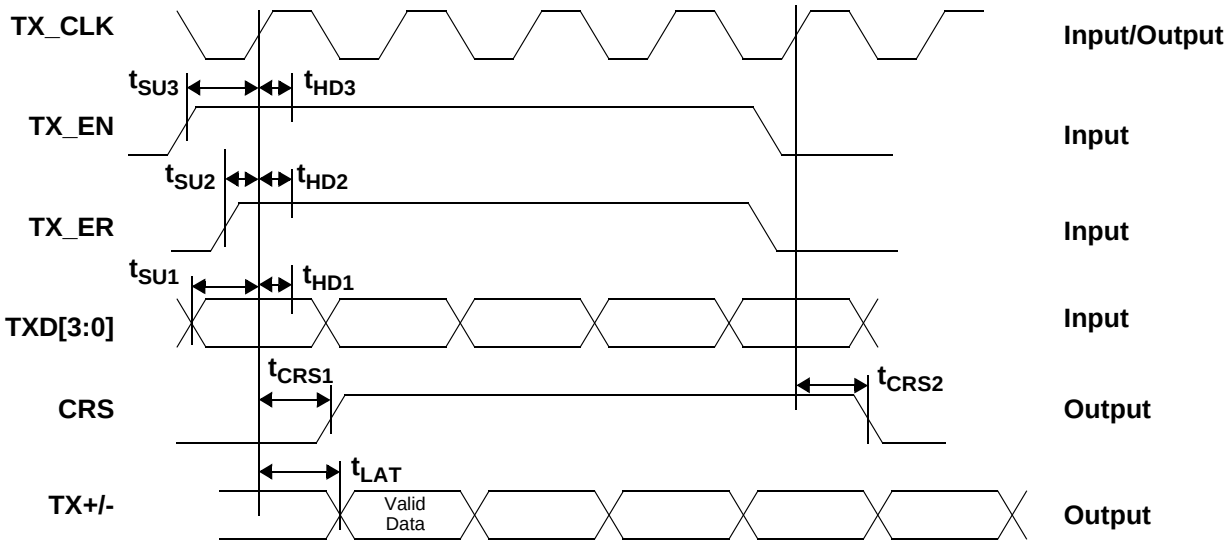
Parameter	Symbol	Min	Typ	Max	Unit
RX_CLK Period	t_P	-	400	-	ns
RX_CLK Pulse Width	t_{WL}, t_{WH}	-	200	-	ns
RXD[3:0], RX_ER, RX_DV setup to rising edge of RX_CLK	t_{SU}	30	-	-	ns
RXD[3:0], RX_ER, RX_DV hold from rising edge of RX_CLK	t_{HD}	30	-	-	ns
RX data valid from CRS	t_{RLAT}	-	8	10	BT
RX+/- preamble to CRS asserted	t_{CRS1}	-	5	7	BT
RX+/- end of packet to CRS de-asserted	t_{CRS2}		2.5	3	BT
RX+/- preamble to COL asserted	t_{COL1}	0	-	7	BT
RX+/- end of packet to COL de-asserted	t_{COL2}	-	-	3	BT
RX_EN asserted to RX_DV, RXD[3:0], RX_ER valid	t_{EN}	-	-	60	ns
RX_EN de-asserted to RX_DV, RXD[3:0]. RX_ER in high impedance state	t_{DIS}	-	-	60	ns



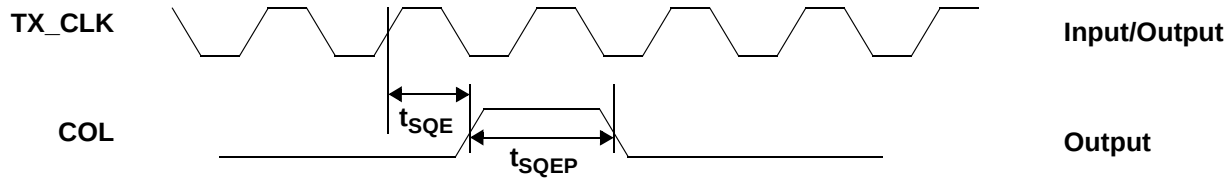
10BASE-T MII TRANSMIT TIMING

Parameter	Symbol	Min	Typ	Max	Unit
TXD[3:0] Setup to TX_CLK High	t_{SU1}	10	-	-	ns
TX_ER Setup to TX_CLK High	t_{SU2}	10	-	-	ns
TX_EN Setup to TX_CLK High	t_{SU3}	10	-	-	ns
TXD[3:0] Hold after TX_CLK High	t_{HD1}	0	-	-	ns
TX_ER Hold after TX_CLK High	t_{HD2}	0	-	-	ns
TX_EN Hold after TX_CLK High	t_{HD3}	0	-	-	ns
TX_EN “high” to CRS asserted latency	t_{CRS1}	0	-	4	BT
TX_EN “low” to CRS de-asserted latency	t_{CRS2}	0	-	16	BT
TX_EN “high” to TX+/- output (TX Latency)	t_{LAT}	6	-	14	BT
SQE Timing					
COL (SQE) Delay after CRS de-asserted	t_{COL}	0.65	0.9	1.6	µs
COL (SQE) Pulse Duration	t_{COLP}	0.65	1.0	1.6	µs

10BASE-T Transmit Timing

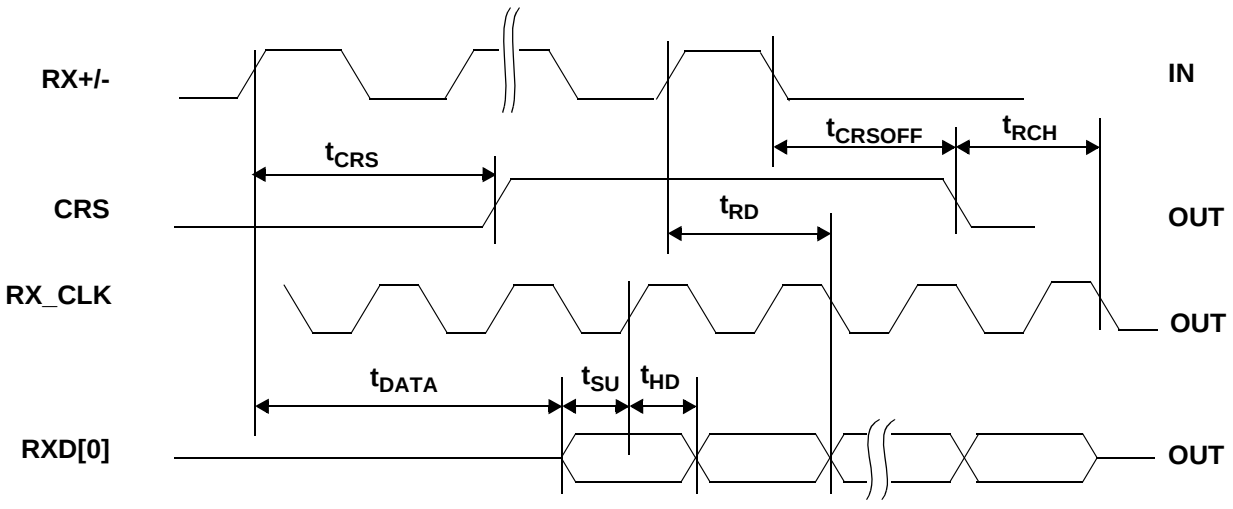


SQE Timing



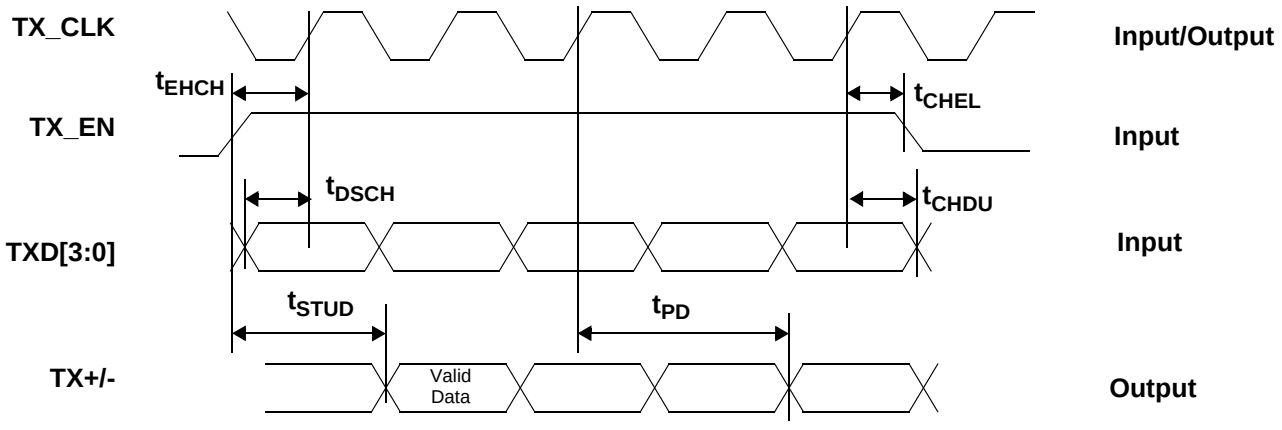
10BASE-T SERIAL RECEIVE TIMING

Parameter	Symbol	Min	Typ	Max	Unit
RX+/- active to RXD[0] active	t_{DATA}	-	-	1200	ns
RX+/- active to CRS active	t_{CRS}	-	-	600	ns
RXD[0] setup from RX_CLK	t_{RDS}	35	-	-	ns
RXD[0] hold from RX_CLK	t_{RDH}	50	-	-	ns
RX_CLK hold after CRS off	t_{RCH}	5	-	-	ns
RXD[0] throughput delay	t_{RD}	-	-	250	ns
CRS turn off delay	t_{CRSOFF}	-	-	400	ns



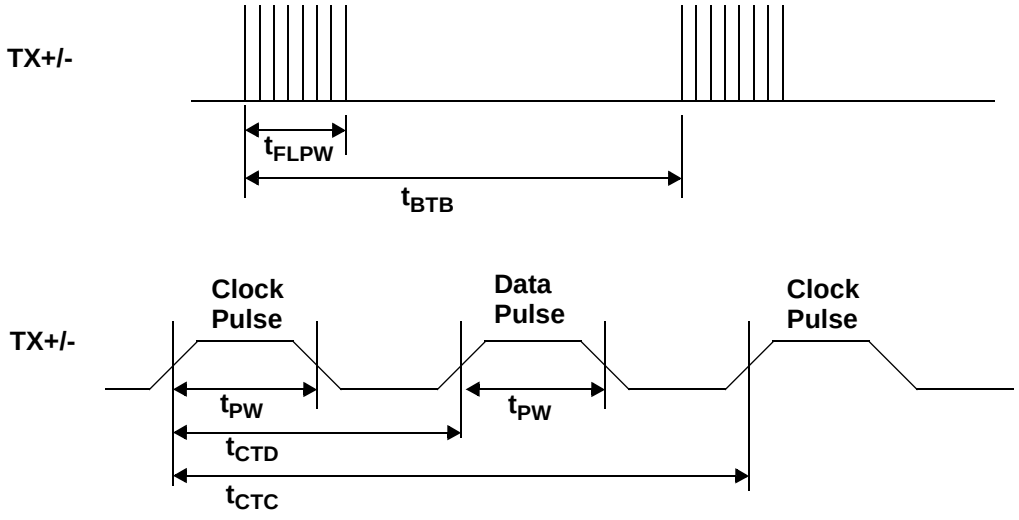
10BASE-T SERIAL TRANSMIT TIMING

Parameter	Symbol	Min	Typ	Max	Unit
TX_EN Setup from TX_CLK	t_{EHCH}	10	-	-	ns
TX_EN Hold after TX_CLK	t_{CHEL}	10	-	-	ns
TXD[0] Setup from TX_CLK	t_{DSCH}	10	-	-	ns
TXD[0] Hold after TX_CLK	t_{CHDU}	10	-	-	ns
Transmit start-up delay	t_{STUD}	-	-	500	ns
Transmit throughput delay	t_{TPD}	-	-	500	ns



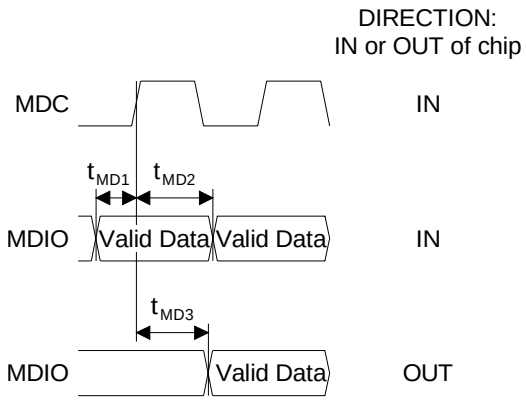
AUTO NEGOTIATION / FAST LINK PULSE TIMING

Parameter	Symbol	Min	Typ	Max	Unit
FLP burst to FLP burst	t_{BTB}	15	16	17	ms
FLP burst width	t_{FLPW}	-	2	-	ms
Clock/Data pulses per burst	-	17	-	33	ea.
Clock/Data pulse width	t_{PW}	-	100	-	ns
Clock pulse to Data pulse	t_{CTD}	55.5	64	69.5	µs
Clock pulse to clock pulse	t_{CTC}	111	128	139	µs



SERIAL MANAGEMENT INTERFACE TIMING

Parameter	Symbol	Min	Typ	Max	Unit
MDC Period	t_p	60	-	-	ns
MDC Pulse Width	t_{WL},t_{WH}	40	-	60	%
MDIO Setup to MDC (MDIO as input)	t_{MD1}	10	-	-	ns
MDIO Hold after MDC (MDIO as input)	t_{MD2}	10	-	-	ns
MDC to MDIO valid (MDIO as output)	t_{MD3}	0	-	40	ns



2. INTRODUCTION

The CS8952 is a complete physical-layer transceiver for 100BASE-TX and 10BASE-T applications. Additionally, the CS8952 can be used with an external optical module for 100BASE-FX.

2.1 High Performance Analog

The highly integrated mixed-signal design of the CS8952 eliminates the need for external analog circuitry such as external transmit or receive filters. The CS8952 builds upon Cirrus Logic's experience in pioneering the high-volume manufacturing of 10BASE-T integrated circuits with "true" internal filters. The CS8952, CS8920, CS8904, and CS8900 include fifth-order, continuous-time Butterworth 10BASE-T transmit and receive filters, allowing those products to meet 10BASE-T wave shape, emission, and frequency content requirements without external filters.

2.2 Low Power Consumption

The CS8952 is implemented in low power CMOS, consuming only 135 mA typically. Three low-power modes are provided to make the CS8952 ideal for power sensitive applications such as CardBus.

2.3 Application Flexibility

The CS8952's digital interface and operating modes can be tailored to efficiently support a wide variety of applications. For example, the Media Independent Interface (MII) supports 100BASE-TX, 100BASE-FX and 10BASE-T NIC cards, switch ports and router ports. Additionally, the low-latency "repeater" interface mode minimizes data delay through the CS8952, facilitating system compliance with overall network delay budgets. To support 10BASE-T applications, the CS8952 provides a 10BASE-T serial port (Seven-wire ENDEC interface).

2.4 Typical Connection Diagram

Figure 1 illustrates a typical MII to CS8952 application with twisted-pair and fiber interfaces. Refer to the Analog Design Considerations section for detailed information on power supply requirements and decoupling, crystal and magnetics requirements, and twisted-pair and fiber transceiver connections.

3. FUNCTIONAL DESCRIPTION

The CS8952 is a complete physical-layer transceiver for 100BASE-TX and 10BASE-T applications. It provides a Physical Coding Sub-layer for communication with an external MAC (Media Access Controller). The CS8952 also includes a complete Physical Medium Attachment layer and a 100BASE-TX and 10BASE-T Physical Medium Dependent layer. Additionally, the CS8952 provides a PECL interface to an external optical module for 100BASE-FX applications.

The primary digital interface to the CS8952 is an enhanced IEEE 802.3 Media Independent Interface (MII). The MII supports parallel data transfer, access to the CS8952 Control and Status registers, and several status and control pins. The CS8952's operating modes can be tailored to support a wide variety of applications, including low-latency 100BASE-TX repeaters, switches and MII-based network interface cards.

For 100BASE-TX applications, the digital data interface can be either 4-bit parallel (nibbles) or 5-bit parallel (code-groups). For 10BASE-T applications, the digital data format can be either 4-bit parallel (nibbles) or one-bit serial.

The CS8952 is controlled primarily by configuration registers via the MII Management Interface. Additionally, a number of the most fundamental register bits can be set at power-up and reset time by connecting pull-up or pull-down resistors to external pins.

The CS8952's MII interface is enhanced beyond IEEE requirements by register extensions and the addition of pins for $\overline{\text{MII\_IRQ}}$, RX_EN, and ISODEF signals. The $\overline{\text{MII\_IRQ}}$ pin provides an inter-

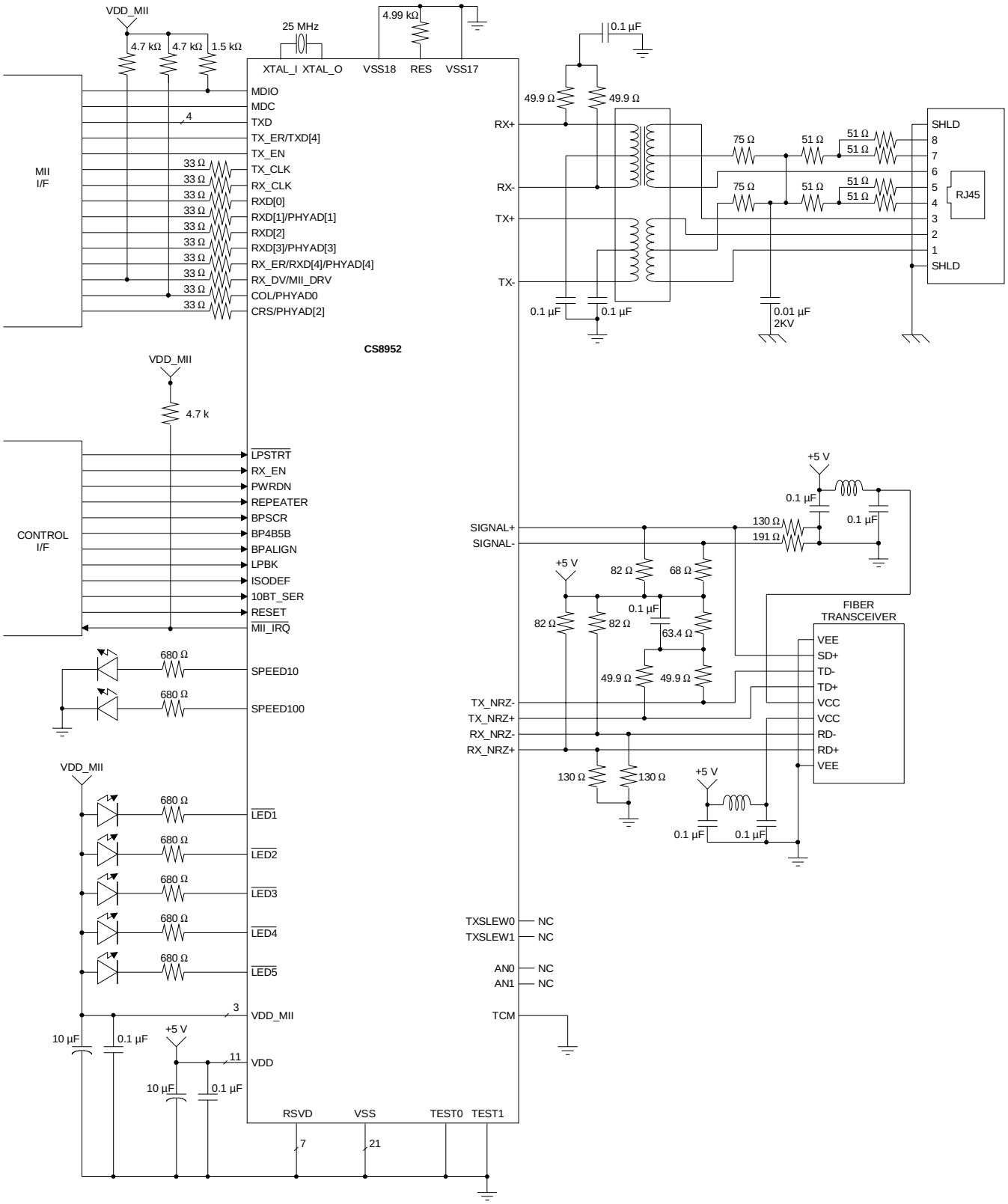


Figure 1. Typical Connection Diagram

rupt signal to the controller when a change of state has occurred in the CS8952, eliminating the need for the system to poll the CS8952 for state changes. The RX_EN signal allows the receiver outputs to be electrically isolated. The ISODEF pin controls the value of register bit ISOLATE in the Basic Mode Control Register (address 00h) which in turn electrically isolates the CS8952's MII data path.

3.1 Major Operating Modes

The following sections describe the four major operating modes of the CS8952:

- 100BASE-X MII Modes (TX and FX)
- 100BASE-X Repeater Modes
- 10BASE-T MII Mode
- 10BASE-T Serial Mode

The choice of operating speed (10 Mb/s versus 100 Mb/s) is made using the auto-negotiation input pins (AN0, AN1) and/or the auto-negotiation MII registers. The auto-negotiation capability also is used to select a duplex mode (full or half duplex). Both speed and duplex modes can either be forced or negotiated with the far-end link partner.

The digital interface mode (MII, repeater, or 10BASE-T serial) is selected by input pins BPALIGN, BP4B5B and 10BT_SER as shown in Table **1**. Speed and duplex selection are made through the AN[1:0] pins as shown in Table **5**.

Operating Mode	BPALIGN	BP4B5B	10BT_SER
100BASE-X MII	0	0	0
10BASE-T MII	0	0	0

Table 1.

Operating Mode	BPALIGN	BP4B5B	10BT_SER
100BASE-X Repeater	1	Don't Care	0
	0	1	0
10BASE-T Serial	Don't Care	Don't Care	1

Table 1.

3.1.1 100BASE-X MII Application (TX and FX)

The CS8952 provides an IEEE 802.3-compliant MII interface. Data is transferred across the MII in four-bit parallel (nibble) mode. TX_CLK and RX_CLK are nominally 25 MHz for 100BASE-X.

The 100BASE-X mode includes both the TX and FX modes, as determined by pin BPSCR (bypass scrambler), or the BPSCR bit (bit 13) in the Loopback, Bypass, and Receiver Error Mask Register (address 18h). In FX mode, an external optical module is connected to the CS8952 via pins TX_NRZ+, TX_NRZ-, RX_NRZ+, RX_NRZ-, SIGNAL+, and SIGNAL-. In FX mode, the MLT-3/NRZI conversion blocks and the scrambler/descrambler are bypassed.

3.1.1.1 Symbol Encoding and Decoding

In 100BASE-X modes, 4-bit nibble transmit data is encoded into 5-bit symbols for transmission onto the media as shown in Tables **2** and **3**. The encoding is necessary to allow data and control symbols to be sent consecutively along the same media transparent to the MAC layer. This encoding causes the symbol rate transmitted across the wire (125 symbols/second) to be greater than the actual data rate of the system (100 symbols/second).

DATA and CONTROL Codes (RX_ER = 0 or TX_ER = 0)			
Name	**5-bit Symbol**	**4-bit Nibble**	**Comments**
DATA (Note **1**)			
0	11110	0000	
1	01001	0001	

DATA and CONTROL Codes (RX_ER = 0 or TX_ER = 0)			
Name	**5-bit Symbol**	**4-bit Nibble**	**Comments**
2	10100	0010	
3	10101	0011	
4	01010	0100	
5	01011	0101	
6	01110	0110	
7	01111	0111	
8	10010	1000	
9	10011	1001	
A	10110	1010	
B	10111	1011	
C	11010	1100	
D	11011	1101	
E	11100	1110	
F	11101	1111	
CONTROL (Note **2**)			
I	11111	0101	IDLE (Note **3**)
J	11000	0101	First Start of Stream Symbol
K	10001	0101	Second Start of Stream Symbol
T	01101	0000	First End of Stream Symbol
R	00111	0000	Second End of Stream Symbol

1. DATA code groups are indicated by RX_DV = 1
2. CONTROL code groups are inserted automatically during transmission in response to TX_EN. They are not generated through any combination of TXD[3:0] or TX_ER.
3. IDLE is indicated by RX_DV = 0.

Table 2. 4B5B Symbol Encoding/Decoding

Code Violations (RX_ER = 1 or TX_ER = 1)				
Name	**5-bit Symbol**	**Normal Mode 4-bit Nibble**	**Error Report Mode 4-bit Nibble**	**Comments**
CONTROL (Note **1**)				
I	11111	0000	0000	This portion of the table relates received 5-bit symbols to received 4-bit nibbles only. The control code groups may not be transmitted in the data portion of the frame.
J	11000	0000	0000	
K	10001	0000	0000	
T	01101	0000	0000	
R	00111	0000	0000	
CODE VIOLATIONS				
H	00100	0000	0000	
V0	00000	0110 or 0101 (Note **2**)	0001	
V1	00001	0110 or 0101 (Note **2**)	0111	
V2	00010	0110 or 0101 (Note **2**)	1000	
V3	00011	0110 or 0101 (Note **2**)	1001	
V4	00101	0110 or 0101 (Note **2**)	1010	
V5	00110	0110 or 0101 (Note **2**)	1011	

Code Violations (RX_ER = 1 or TX_ER = 1)				
Name	**5-bit Symbol**	**Normal Mode 4-bit Nibble**	**Error Report Mode 4-bit Nibble**	**Comments**
V6	01000	0110 or 0101 (Note **2**)	1100	
V7	01100	0110 or 0101 (Note **2**)	1101	
V8	10000	0110 or 0101 (Note **2**)	1110	
V9	11001	0110 or 0101 (Note **2**)	1111	

1. CONTROL code groups become violations when found in the data portion of the frame.
2. Invalid code groups are mapped to 5h unless the Code Error Report select bit in the Loopback, Bypass, and Receiver Error Mask Register (address 18h) is set, in which case invalid code groups are mapped to 6h.

Table 3. 4B5B Code Violation Decoding

3.1.1.2 100 Mb/s Loopback

One of two internal 100BASE-TX loopback modes can be selected. Local loopback redirects the TXD[3:0] input data to RXD[3:0] data outputs through the 4B5B coders and scramblers. Local loopback is selected by asserting pin LPBK, by setting the LPBK bit (bit 14) in the Basic Mode Control Register (address 00h) or by setting bits 8 and 11 in the Loopback, Bypass, and Receiver Error Mask Register (address 18h) as shown in Table **4**.

Remote loopback redirects the analog line interface inputs to the analog line driver outputs. Remote loopback is selected by setting bit 9 in the Loopback, Bypass, and Receiver Error Mask Register (address 18h) as shown in Table **4**.

Remote Loopback (bit 9)	PMD Loopback (bit 8)	Function
0	0	No Loopback
0	1	Local Loopback (toward MII)
1	0	Remote Loopback (toward line)
1	1	Operation is undefined

Table 4.

When changing between local and non-loopback modes, the data on RXD[3:0] will be undefined for approximately 330 µs.

3.1.2 100BASE-X Repeater Application

The CS8952 provides two low latency modes for repeater applications. These are selected by asserting either pin BPALIGN or BP4B5B. Both pins have the effect of bypassing the 4B5B encoder and decoder. Bypassing the coders decreases latency, and uses a 5-bit wide parallel code group interface on pins RXD[4:0] and TXD[4:0] instead of the 4-bit wide MII nibble interface on pins RXD[3:0] and TXD[3:0]. In repeater mode, pin RX_ER is redefined as the fifth receive data bit (RXD4), and pin TX_ER is redefined as the fifth transmit data bit (TXD4).

BPALIGN can also be selected by setting bit 12 in Loopback, Bypass, and Receiver Error Mask Register (address 18h). BP4B5B can be selected by setting bit 14 of the same register.

Pin BPALIGN causes more of the CS8952 to be bypassed than the BP4B5B pin. BPALIGN also bypasses the scrambler/descrambler, and the NRZI to NRZ converters (see Figure **1**). Also, for repeater applications, pin REPEATER should be asserted to redefine the function of the CRS (carrier sense) pin. The REPEATER function may also be invoked by setting bit 12 in the PCS Sublayer Configuration Register (address 17h).

For repeater applications, the RX_EN pin can be used to gate the receive data pins (RXD[4:0],

RX_CLK, RX_DV, COL, and CRS) onto a shared, external repeater system bus.

3.1.3 10BASE-T MII Application

The digital interface used in this mode is the same as that used in the 100BASE-X MII mode except that TX_CLK and RX_CLK are nominally 2.5 MHz.

The CS8952 includes a full-featured 10BASE-T interface, as described in the following sections.

3.1.3.1 Full and Half Duplex operation

The 10BASE-T function supports full and half duplex operation as determined by pins AN[1:0] and/or the corresponding MII register bits. (See Table **5**).

3.1.3.2 Collision Detection

If half duplex operation is selected, the CS8952 detects a 10BASE-T collision whenever the receiver and transmitter are active simultaneously. When a collision is present, the collision is reported on pin COL. Collision detection is undefined for full-duplex operation.

3.1.3.3 Jabber

The jabber timer monitors the transmitter and disables the transmission if the transmitter is active for greater than approximately 105 ms. The transmitter stays disabled until approximately 406 ms after the internal transmit request is no longer enabled.

3.1.3.4 Link Pulses

To prevent disruption of network operation due to a faulty link segment, the CS8952 continually monitors the 10BASE-T receive pair (RXD+ and RXD-) for packets and link pulses. After each packet or link pulse is received, an internal Link-Loss timer is started. As long as a packet or link pulse is received before the Link-Loss timer finishes (between 50 and 100 ms), the CS8952 maintains normal operation. If no receive activity is detected, the CS8952 disables packet transmission to prevent “blind” transmissions onto the network (link pulses are still sent while packet transmission is disabled). To reactivate transmission, the receiver must detect a single packet (the packet itself is ignored), or two normal link pulses separated by more than 6 ms and no more than 50 ms.

The CS8952 automatically checks the polarity of the receive half of the twisted pair cable. To detect a reversed pair, the receiver examines received link pulses and the End-of-Frame (EOF) sequence of incoming packets. If it detects at least one reversed link pulse and at least four frames in a row with negative polarity after the EOF, the receive pair is considered reversed. If the polarity is reversed and bit 1 of the 10BASE-T Configuration Register (address 1Ch), is set, the CS8952 automatically corrects a reversal.

In the absence of transmit packets, the transmitter generates link pulses in accordance with Section 14.2.1.1 of the Ethernet standard. Transmitted link pulses are positive pulses, one bit time wide, typically generated at a rate of one every 16 ms. The 16 ms timer also starts whenever the transmitter completes an End-of-Frame (EOF) sequence. Thus, a link pulse will be generated 16 ms after an EOF unless there is another transmitted packet.

3.1.3.5 Receiver Squelch

The 10BASE-T squelch circuit determines when valid data is present on the RXD+/RXD- pair. Incoming signals passing through the receive filter are tested by the squelch circuit. Any signal with amplitude less than the squelch threshold (either positive or negative, depending on polarity) is rejected.

3.1.3.6 10BASE-T Loopback

When Loopback is selected, the TXD[3:0] pins are looped back into the RXD[3:0] pins through the

Manchester Encoder and Decoder. Selection is made via:

- setting bit 14 in the Basic Mode Control Register (address 00h) or
- setting bits 8 and 11 in the Loopback, Bypass, and Receiver Error Mask Register (address 18h) or
- asserting the LPBK pin.

3.1.3.7 Carrier Detection

The carrier detect circuit informs the MAC that valid receive data is present by asserting the Carrier Sense signal (CRS) as soon it detects a valid bit pattern (1010b or 0101b for 10BASE-T). During normal packet reception, CRS remains asserted while the frame is being received, and is de-asserted within 2.3 bit times after the last low-to-high transition of the End-of-Frame (EOF) sequence. Whenever the receiver is idle (no receive activity), CRS is de-asserted.

3.1.4 10BASE-T Serial Application

This mode is selected when pin 10BT_SERis asserted during power-up or reset, and operates similar to the 10BASE_T MII mode except that data is transferred serially on pins RXD0 and TXD0 using a 10 MHz RX_CLK and TX_CLK. Receive data is framed by CRS rather than RX_DV.

3.2 Auto-Negotiation

The CS8952 supports auto-negotiation, which is the mechanism that allows the two devices on either end of an Ethernet link segment to share information and automatically configure both devices for maximum performance. When configured for auto-negotiation, the CS8952 will detect and automatically operate full-duplex at 100 Mb/s if the device on the other end of the link segment also supports full-duplex, 100 Mb/s operation, and auto-negotiation. The CS8952 auto-negotiation capability is fully compliant with the relevant portions of section 28 of the IEEE 802.3u standard.

The CS8952 can auto-negotiate both operating speed (10 versus 100 Mb/s), duplex mode (half duplex versus full duplex), and flow control (pause frames), or alternatively can be set not to negotiate. At power-up and reset times, the auto-negotiation mode is selected via the auto-negotiation input pins (AN[1:0]). This selection can later be changed using the Auto-Negotiation Advertisement Register (address 04h).

Pins AN[1:0] are three level inputs, and have the function shown in Table **5**.

AN1	AN0	Forced/ Auto	Speed (Mb/s)	Full/Half Duplex
Low	Floating	Forced	10	Half
High	Floating	Forced	10	Full
Floating	Low	Forced	100	Half
Floating	High	Forced	100	Full
Floating	Floating	Auto-Neg	100/10	Full/Half
Low	Low	Auto-Neg	10	Half
Low	High	Auto-Neg	10	Full
High	Low	Auto-Neg	100	Half
High	High	Auto-Neg	100	Full

Table 5.

Auto-Negotiation encapsulates information within a burst of closely spaced Link Integrity Test Pulses, referred to as a Fast Link Pulse (FLP) Burst. The FLP Burst consists of a series of Link Integrity Pulses which form an alternating clock / data sequence. Extraction of the data bits from the FLP Burst yields a Link Code Word which identifies the capability of the remote device.

In order to support legacy 10 and 100 Mb/s devices, the CS8952 also supports parallel detection. In parallel detection, the CS8952 monitors activity on the media to determine the capability of the link partner even without auto-negotiation having occurred.

3.3 Reset Operation

Reset occurs in response to six different conditions:

1) There is a chip-wide reset whenever the RESET pin is high for at least 200 ns. During a chip-wide reset, all circuitry and registers in the CS8952 are reset.

2) When power is applied, the CS8952 maintains reset until the voltage at the VDD supply pins reaches approximately 3.6 V. The CS8952 comes out of reset once VDD is greater than approximately 3.6 V and the crystal oscillator has stabilized.

3) There is a chip-wide reset whenever the RESET bit (bit 15 of the Basic Mode Control Register (address 00h)) is set.

4) Digital circuitry is reset whenever bit 0 of the PCS Sub-Layer Configuration Register (address 17h) is set. Analog circuitry is unaffected.

5) Analog circuitry is reset and recalibrated whenever the CS8952 enters or exits the power-down state, as requested by pin PWRDN.

6) Analog circuitry is reset and recalibrated whenever the CS8952 changes between 10 Mb/s and 100 Mb/s modes.

After a reset, the CS8952 latches the signals on various input pins in order to initialize key registers and goes through a self configuration. This includes calibrating on-chip analog circuitry. Time required for the reset calibration is typically 40 ms. External circuitry may access registers internal to the CS8952 during this time. Reset and calibration complete is indicated when bit 15 of the Basic Mode Control Register (address 00h) is clear.

3.4 LED Indicators

The $\overline{\text{LEDx}}$, SPD100, and SPD10 output pins provide status information that can be used to drive LEDs or can be used as inputs to external control circuitry. Indication options include: receive activity, transmit activity, collision, carrier sense, polarity OK, descrambler synchronization status, auto-negotiation status, speed (10 vs. 100), and duplex mode.

4. MEDIA INDEPENDENT INTERFACE (MII)

The Media Independent Interface (MII) provides a simple interconnect to an external Media Access Controller (MAC). This connection may be chip to chip, motherboard to daughterboard, or a connection between two assemblies attached by a limited length of shielded cable and an appropriate connector.

The MII interface uses the following pins:

STATUS Pins

- COL - Collision indication, valid only for half duplex modes.
- CRS - Carrier Sense indication

SERIAL MANAGEMENT Pins

- MDIO - a bi-directional serial data path
- MDC - clock for MDIO (16.7 MHz max)
- $\overline{\text{MII\_IRQ}}$ - Interrupt indicating change in the Interrupt Status Register (address 11h)

RECEIVE DATA Pins

- RXD[3:0] - Parallel data output path
- RX_CLK - Recovered clock output
- RX_DV - Indicates when receive data is present and valid
- RX_ER - Indicates presence of error in received data
- RX_EN - Can be used to tri-state receiver output pins

TRANSMIT DATA Pins

- TXD[3:0] - Parallel data input path
- TX_CLK - Transmit clock
- TX_EN - Indicates when transmit data is present and valid
- TX_ER - Request to transmit a 100BASE-T HALT symbol, ignored for 10BASE-T operation.

The interface uses TTL signal levels, which are compatible with devices operating at a nominal supply voltage of either 5.0 or 3.3 volts. It is capable of supporting either 10 Mb/s or 100 Mb/s data rates transparently. That is, all signaling remains identical at either data rate; only the nominal clock frequency is changed.

4.1 MII Frame Structure

Data frames transmitted through the MII have the following format:

Preamble (7 Bytes)	Start of Frame Delimiter (1 Byte)	Data	End of Frame Delimiter

Each frame is preceded by an inter-frame gap. The inter-frame gap is an unspecified time during which no data activity occurs on the media as indicated by the de-assertion of CRS for the receive path and TX_EN for the transmit path.

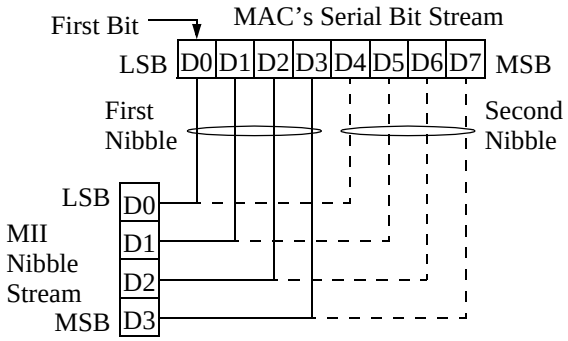
The Preamble consists of seven bytes of 10101010.

The Start of Frame Delimiter consists of a single byte of 10101011.

Data may be any number of bytes.

The End of Frame Delimiter is conveyed by the de-assertion of RX_DV and TX_EN for receive and transmit paths, respectively.

Transmission and/or reception of each byte of data is done one nibble at a time in the following order:



4.2 MII Receive Data

The presence of recovered data on the RXD[3:0] bus is indicated by the assertion of RX_DV. RX_DV will remain asserted from the beginning of the preamble (or Start of Frame Delimiter if preamble is not used) to the End of Frame Delimiter. Once RX_DV is asserted, valid data will be driven

onto RXD[3:0] synchronously with respect to RX_CLK.

Receive errors are indicated during frame reception by the assertion of RX_ER. It indicates that an error was detected somewhere in the frame currently being transferred across the MII. RX_ER will transition synchronously with respect to the RX_CLK, and will be held high for one cycle for each error received. It is up to the MAC to ensure that a CRC error is detected in that frame by the Logical Link Control. Figure **2** illustrates reception without errors, and Figure **3** illustrates reception with errors.

4.3 MII Transmit Data

TX_EN is used by the MAC to signal to the CS8952 that valid nibbles of data are being presented across the MII via TXD[3:0]. TX_EN must be asserted synchronously with the first nibble of preamble, and must remain asserted as long as valid data is being presented to the MII.

TX_EN must be de-asserted within one TX_CLK cycle after the last nibble of data (CRC) has been presented to the CS8952. When TX_EN is not asserted, data on TXD[3:0] is ignored.

Transmit errors should be signaled by the MAC by asserting TX_ER for one or more TX_CLK cycles. TX_ER must be synchronous with TX_CLK. This will cause the CS8952 to replace the nibble with a HALT symbol in the frame being transmitted. This invalid data will be detected by the receiving PHY and flagged as a bad frame. Figure **4** illustrates transmission without errors, and Figure **5** illustrates transmission with errors.

4.4 MII Management Interface

The CS8952 provides an enhanced IEEE 802.3 MII Management Interface. The interface consists of three signals: a bi-directional serial data line (MDIO), a data clock (MDC), and an optional interrupt signal ($\overline{\text{MII\_IRQ}}$). The Management Interface can be used to access status and control registers internal to the CS8952. The CS8952 implements an extended set of 16-bit MII registers. Eight of the registers are defined by the IEEE 802.3

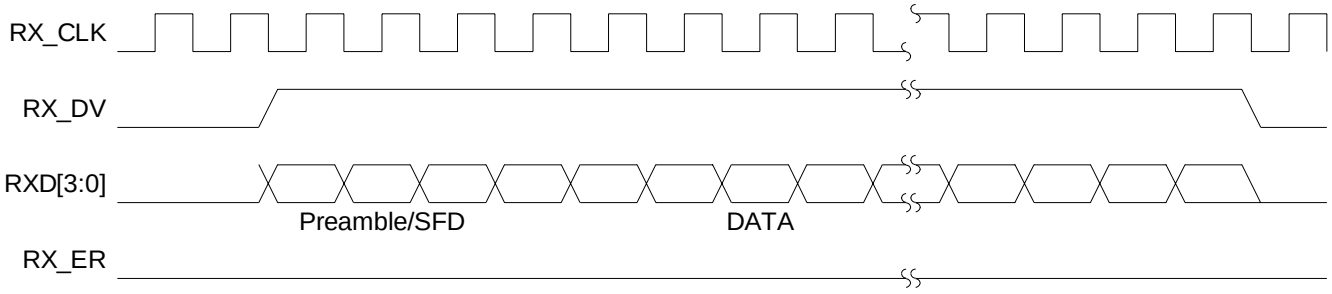


Figure 2. Reception without errors

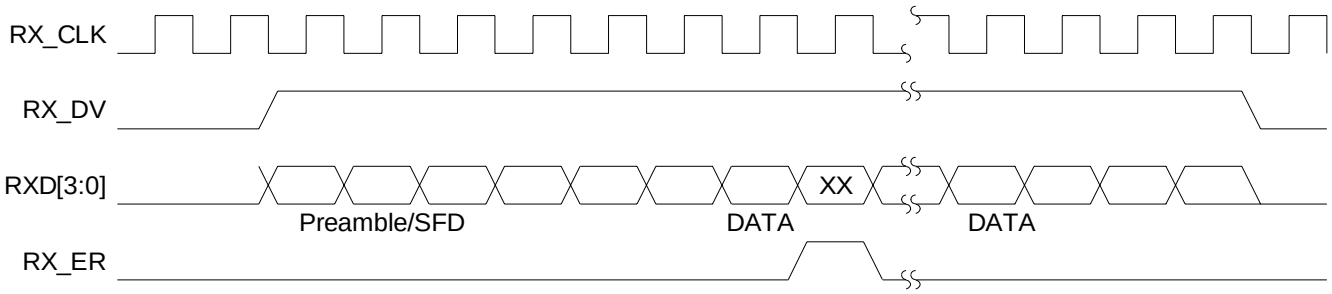


Figure 3. Reception with errors

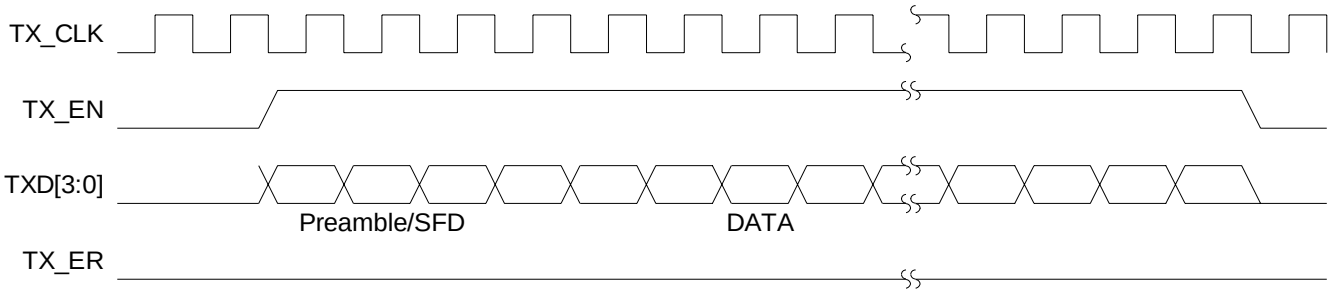


Figure 4. Transmission without errors

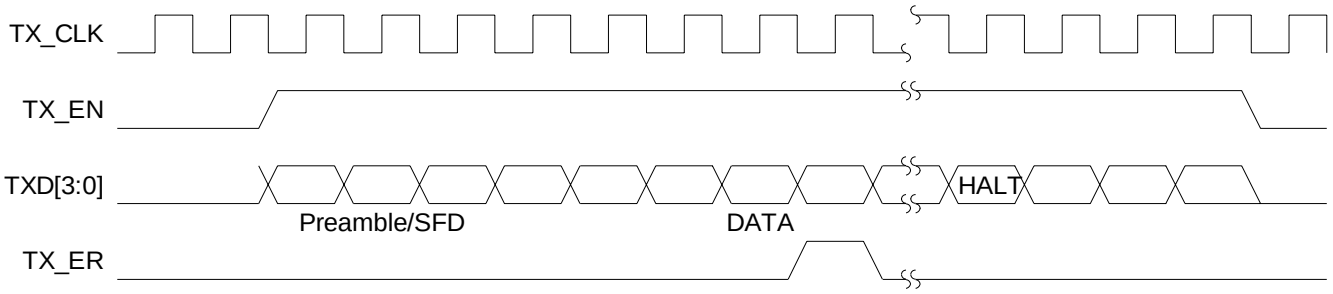


Figure 5. Transmission with errors

specification, while the remaining registers provide enhanced monitoring and control capabilities.

As many as 31 devices may share a single Management Interface. A unique five-bit PHY address is associated with each device, with all devices responding to PHY address 00000. The CS8952 determines its PHY address at power-up or reset through the PHYAD[4:0] pins.

4.5 MII Management Frame Structure

Frames transmitted through the MII Management Interface have the following format (Table **6**):

When the management interface is idle, the MDIO signal will be tri-stated, and the MAC is required to keep MDIO pulled to a logic ONE.

At the beginning of each transaction, the MAC will typically send a sequence of 32 contiguous logic ONE bits on MDIO with 32 corresponding clock cycles on MDC to provide the CS8952 with a pattern that it can use to establish synchronization. Optionally, the CS8952 may be configured to operate without the preamble through bit 9 of the PCS Sub-Layer Configuration Register (address 17h).

Preamble (32 bits)	Start of Frame (2 bits)	Opcode (2 bits)	PHY Address (5 bits)	Register Address (5 bits)	Turnaround (2 bits)	Data (16 bits)	Idle

Table 6. Format for Frame Transmitted through the MII Management Interface

The Start of Frame is indicated by a 01 bit pattern.

A read transaction is indicated by an Opcode of 10 and a write by 01.

The PHY Address is five bits, with the most significant bit sent first. If the PHY address included in the frame is not 00000 or does not match the PHYAD field of the Self Status Register (address 19h), the rest of the frame is ignored.

The register address is five bits, with the most significant bit sent first, and indicates the CS8952 register to be written to/read from.

The Turnaround time is a two bit time spacing between when the MAC drives the last register address bit onto MDIO and the data field of a management frame in order to avoid contention during a read transaction. For a read transaction, the MAC should tri-state the MDIO pin beginning on the first bit time, and the CS8952 will begin driving the MDIO signal to a logic ZERO during the second bit time. During write transactions, since the MDIO direction does not need to be reversed, the MAC will drive the MDIO to a logic ONE for the first bit time and a logic ZERO for the second.

The data field is always 16 bits in length, with the most significant bit sent first.

5. CONFIGURATION

The CS8952 can be configured in a variety of ways. All control and status information can be accessed via the MII Serial Management Interface. Additionally, many configuration options can be set at power-up or reset times via individual control lines. Some configuration capabilities are available at any time via individual control lines.

5.1 Configuration At Power-up/Reset Time

At power-up and reset time, the following pins are

Pin Name	Function
10BT_SER	Select 10BASE-T serial mode
AN[1:0]	Select auto-negotiation mode
BP4B5B	Bypass 4B5B coders
BPALIGN	Bypass 4B5B coders and scramblers
BPSCR	Bypass scramblers, enter FX mode
ISODEF	Electrically isolate MII after reset
LPSTRT	Start in low power mode
PHYAD[4:0]	Set MII PHY address
REPEATER	Control definition of CRS pin, enable carrier integrity monitor and SQE function
MII_DRV	Set MII driver strength
TCM	Set TX_CLK mode
TXSLEW[1:0]	Set 100BASE-TX transmitter output slew rate

5.2 Configuration Via Control Pins

The following pins are for dedicated control signals and can be used at any time to configure the CS8952.

Pin Name	Function
LPBK	Enter loopback mode
PWRDN	Enter power-down mode
RESET	Reset

5.3 Configuration via the MII

The CS8952 supports configuration by software control through the use of 16-bit configuration and status registers accessed via the MDIO/MDC pins (MII Management Interface). The first seven registers are defined by the IEEE 802.3 specification. Additional registers extend the register set to provide enhanced monitoring and control capabilities.

6. CS8952 REGISTERS

The CS8952 register set is comprised of the 16-bit status and control registers described below. A detailed description each register follows.

Register Address	Description	Type
0h	Basic Mode Control Register	Read/Write
1h	Basic Mode Status Register	Read-Only

Register Address	Description	Type
2h	PHY Identifier #1	Read-Only
3h	PHY Identifier #2	Read-Only
4h	Auto-Negotiation Advertisement Register	Read/Write
5h	Auto-Negotiation Link Partner Ability Register	Read-Only
6h	Auto-Negotiation Expansion Register	Read-Only
7h	Auto-Negotiation Next Page Transmit Register	Read/Write
8h through Fh	Reserved by IEEE 802.3 Working Group	-
10h	Interrupt Mask Register	Read/Write
11h	Interrupt Status Register	Read-Only
12h	Disconnect Count Register	Read-Only
13h	False Carrier Count Register	Read-Only
14h	Scrambler Key Initialization Register	Read/Write
15h	Receive Error Count Register	Read-Only
16h	Descrambler Key Initialization Register	Read/Write
17h	PCS Sub-Layer Configuration Register	Read/Write
18h	Loopback, Bypass and Receiver Error Mask Register	Read/Write
19h	Self-Status Register	Read/Write
1Ah	Reserved	-
1Bh	10BASE-T Status Register	Read-Only
1Ch	10BASE-T Configuration Register	Read/Write
1Dh through 1Fh	Reserved	-

6.1 Basic Mode Control Register - Address 00h

15	14	13	12	11	10	9	8
Software Reset	Loopback	Speed Selection	Auto-Neg Enable	Power Down	Isolate	Restart Auto-Neg	Duplex Mode

7	6	5	4	3	2	1	0
Collision Test	Reserved						

BIT	NAME	TYPE	RESET	DESCRIPTION
15	Software Reset	Read/Set	0	Setting this bit performs a chip-wide reset. All status and control registers are set to their default states, and the analog circuitry is re-calibrated. This bit is an Act-Once bit which is cleared once the reset and re-calibration have completed. This bit will also be set automatically while the analog circuitry is reset and re-calibrated during mode changes.
14	Loopback	Read/Write	0	When set, the CS8952 is placed in a loop back mode. Any data sent on the transmit data path is returned on the receive data path. Loopback mode is entered regardless of whether 10 Mb/s or 100 Mb/s operation has been configured. This bit will be set upon the assertion of the LPBK pin, and will be automatically cleared upon its deassertion.
13	Speed Selection	Read/Write	If auto-negotiation is enabled via the AN[1:0] pins, reset to 1; otherwise, reset to 0	When bit 12 is clear, setting this bit configures the CS8952 for 100 Mb/s operation. Clearing this bit sets the configuration at 10 Mb/s. When bit 12 is set, this bit is ignored.
12	Auto-Neg Enable	Read/Write	If auto-negotiation is enabled via the AN[1:0] pins, reset to 1; otherwise, reset to 0	Setting this bit enables the auto-negotiation process. When this bit is set, bits 13 and 8 have no affect on the link configuration. The link configuration is determined by the auto-negotiation process. Clearing this bit disables auto-negotiation.
11	Power Down	Read/Write	0	When this bit is set, the CS8952 enters a low power consumption state. Clearing this bit allows normal operation. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
10	Isolate	Read/Write	If PHYAD = 00000, reset to 1; otherwise reset to the value on the ISODEF pin	Setting this bit causes the MII data path to be electrically isolated by tri-stating all data outputs (i.e. TX_CLK, RX_CLK, RX_DV, RX_ER, RXD[3:0], COL, and CRS). In addition the CS8952 will not respond to the TXD[3:0], TX_EN, and TX_ER inputs. It will, however, respond to MDIO and MDC. Clearing this bit allows normal operation.

BIT	NAME	TYPE	RESET	DESCRIPTION
9	Restart Auto-Neg	Read/Set	0	Setting this bit causes auto-negotiation to be restarted. It is an Act-Once bit which is cleared once auto-negotiation has begun. Clearing this bit has no effect on the auto-negotiation process.
8	Duplex Mode	R/W	If auto-negotiation is enabled via the AN[1:0] pins, reset to 0; otherwise, reset to 1	When bit 12 is clear, this bit controls the Full-Duplex/Half-Duplex operation of the part. When set, the part is configured for Full-Duplex operation, and when clear the part is configured for Half Duplex operation. The setting of this bit is superseded by auto-negotiation, and thus has no effect if bit 12 is set.
7	Collision Test	R/W	0	When set, the COL pin will be asserted within 10 bit times in response to the assertion of TX_EN. Upon the deassertion of TX_EN, COL will be deasserted within 4 bit times. When Collision Test is clear, COL functions normally.
6:0	Reserved	Read Only	000 0000	

6.2 Basic Mode Status Register - Address 01h

15	14	13	12	11	10	9	8
100BASE-T4	100BASE-TX/ Full Duplex	100BASE-TX/ Half Duplex	10BASE-T/ Full Duplex	10BASE-T/ Half Duplex	Reserved		

7	6	5	4	3	2	1	0
Reserved	MF Preamble Suppression	Auto-Neg Complete	Remote Fault	Auto-Neg Ability	Link Status	Jabber Detect	Extended Capability

BIT	NAME	TYPE	RESET	DESCRIPTION
15	100BASE-T4	Read Only	0	The CS8952 does not support 100BASE-T4 operation, so this bit will always read 0.
14	100BASE-TX/Full Duplex	Read Only	1	When this bit is set, it indicates that the CS8952 is capable of 100BASE-TX Full-Duplex operation. This bit reflects the status of the 100BASE-TX/Full-Duplex bit in the Auto-Negotiation Advertisement Register (address 04h).
13	100BASE-TX/Half Duplex	Read Only	1	When this bit is set, it indicates that the CS8952 is capable of 100BASE-TX Half-Duplex operation. This bit reflects the status of the 100BASE-TX/Half Duplex bit in the Auto-Negotiation Advertisement Register (address 04h).
12	10BASE-T/Full Duplex	Read Only	1	When this bit is set, it indicates that the CS8952 is capable of 10BASE-T Full-Duplex operation. This bit reflects the status of the 10BASE-T/Full Duplex bit in the Auto-Negotiation Advertisement Register (address 04h).
11	10BASE-T/Half Duplex	Read Only	1	When this bit is set, it indicates that the CS8952 is capable of 10BASE-T Half-Duplex operation. This bit reflects the status of the 10BASE-T/Half Duplex bit in the Auto-Negotiation Advertisement Register (address 04h).
10:7	Reserved	Read Only	0000	
6	MF Preamble Suppression	Read Only	1	When set, this bit indicates that the CS8952 is capable of accepting management frames regardless of whether they are preceded by the preamble pattern. When clear, it indicates that the management frame must be preceded by the preamble pattern to be considered valid. This bit reflects the status of the MR Preamble Enable bit in the PCS Sub-Layer Configuration Register (address 17h).
5	Auto-Neg Complete	Read Only	0	This bit is set to a 1 when the auto-negotiation process has completed. This is an indication that data is valid in the Auto-Negotiation Advertisement Register (address 04h), the Auto-Negotiation Link Partner Ability Register (address 05h), and the Auto-Negotiation Expansion Register (address 06h).
4	Remote Fault	Read Only	0	When auto-negotiation is enabled, this bit is set if the Remote Fault bit is set in the Auto-Negotiation Link Partner Ability Register (address 05h). When auto-negotiation is disabled, this bit will be set when a Far-End Fault Indication for 100BASE-TX is detected.

BIT	NAME	TYPE	RESET	DESCRIPTION
3	Auto-Neg Ability	Read Only	1	This bit indicates that the CS8952 has auto-negotiation capability. Therefore this bit will always read back a value of 1.
2	Link Status	Read Only	0	When set, this bit indicates that a valid link has been established. Upon a link failure, this bit is cleared and latched. It will remain cleared until this register is read.
1	Jabber Detect	Read Only	0	In 10BASE-T mode, if the last transmission is longer than 105 ms, then the packet output is terminated by the jabber logic and this bit is set. If JabberiE (Interrupt Mask Register (address 10h), bit 3) is set, an MII Interrupt will be generated. This bit is implemented with a latching function so that the occurrence of a jabber condition causes it to become set until it is cleared by a read to this register, a read to the Interrupt Status Register (address 11h), or a reset. No jabber detect function has been defined for 100BASE-TX.
0	Extended Capability	Read Only	1	This bit indicates that an extended register set may be accessed (registers beyond address 01h). This bit always reads back a value of 1.

6.3 PHY Identifier, Part 1 - Address 02h

15	14	13	12	11	10	9	8
Organizationally Unique Identifier: Bits[3:10]							

7	6	5	4	3	2	1	0
Organizationally Unique Identifier: Bits[11:18]							

BIT	NAME	TYPE	RESET	DESCRIPTION
15:0	Organizationally Unique Identifier (bits 3:18)	Read/Write	001Ah	This identifier is assigned to PHY manufacturers by the IEEE. Its intention is to provide sufficient information to support 10/100 Management as defined in Clause 30.1.2 of the IEEE 802.3 specification. This register contains bits [3:18] of the OUI. Bit 3 of the OUI is located in bit 15 of the PHY Identifier, bit 4 of the OUI is in bit 14, and so on. **Note:** This field is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.

6.4 PHY Identifier, Part 2 - Address 03h

15	14	13	12	11	10	9	8
Organizationally Unique Identifier - Bits[19:24]						Part Number	

7	6	5	4	3	2	1	0
Part Number				Revision Number			

BIT	NAME	TYPE	RESET	DESCRIPTION
15:10	Organizationally Unique Identifier (bits 19:24)	Read/Write	00 1000	This identifier is assigned to PHY manufacturers by the IEEE. Its intention is to provide sufficient information to support 10/100 Management as defined in Clause 30.1.2 of the IEEE 802.3 specification. This register contains bits [19:24] of the OUI. Bit 19 of the OUI is located in bit 15 of this register, bit 20 of the OUI is in bit 14, and so on. **Note:** This field is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
9:4	Part Number	Read/Write	10 0000	These bits indicate the CS8952 part number. It has been set to a value of 100000. **Note:** This field is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
3:0	Revision Number	Read/Write	0001	These bits indicate the CS8952 part revision. Rev. A 0000 Rev. B 0001 etc. **Note:** This field is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.

6.5 *Auto-Negotiation Advertisement Register - Address 04h*

15	14	13	12	11	10	9	8
Next Page	Acknowledge	Remote Fault	Technology Ability Field				

7	6	5	4	3	2	1	0
Technology Ability Field			Protocol Selector Field				

BIT	NAME	TYPE	RESET	DESCRIPTION
15	Next Page	Read/Write	0	When set, this bit enables the ability to exchange Next-Pages with the link partner. This bit should be cleared if it is not desired to engage in Next Page exchange. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
14	Acknowledge	Read Only	0	When set, this bit indicates consistent reception of the link partner's data.
13	Remote Fault	Read/Write	0	This bit may be used to indicate a fault condition to the link partner. Setting this bit will signal to the link partner that a fault condition has occurred.
12:5	Technology Ability Field	Read/Write	0000 1111	This field determines the advertised capabilities of the CS8952 as shown below. When the bit is set, the corresponding technology will be advertised during auto-negotiation. BIT Capability 12 Reserved 11 Reserved 10 PAUSE operation for full duplex links. Set only if supported by the host MAC. 9 100BASE-T4 (Note: this technology is not supported and can not be set. 8 100BASE-TX Full Duplex 7 100Base-TX Half Duplex 6 10BASE-T Full Duplex 5 10BASE-T Half Duplex
4:0	Protocol Selector Field	Read/Write	0 0001	This field is used to identify the type of message being sent by auto-negotiation. This field defaults to a value of "00001" for IEEE 802.3 messages.

6.6 *Auto-Negotiation Link Partner Ability Register - Address 05h*

15	14	13	12	11	10	9	8
Next Page	Acknowledge	Remote Fault	Technology Ability Field				

7	6	5	4	3	2	1	0
Technology Ability Field			Protocol Selector Field				

BIT	NAME	TYPE	RESET	DESCRIPTION
15	Next Page	Read Only	0	When set, this bit indicates that the link partner is capable of participating in the Next Page exchange.
14	Acknowledge	Read Only	0	When set, this bit indicates that the link partner has received consistent data from the CS8952.
13	Remote Fault	Read Only	0	This bit indicates that a fault condition occurred on the far end. When this bit is set and auto-negotiation is enabled, the Remote Fault bit in the Basic Mode Status Register (address 01h) will also be set.
12:5	Technology Ability Field	Read Only	0000 0000	This field indicates the advertised capabilities of the link partner as shown below. When the bit is set, the corresponding technology has been advertised during auto-negotiation. BIT Capability 12 Reserved 11 Reserved 10 PAUSE operation for full duplex links. 9 100BASE-T4 (Note: this technology is not 8 100BASE-TX Full Duplex 7 100Base-TX Half Duplex 6 10BASE-T Full Duplex 5 10BASE-T Half Duplex
4:0	Protocol Selector Field	Read Only	0 0000	This field is used to identify the type of message being received during auto-negotiation.

6.7 Auto-Negotiation Expansion Register - Address 06h

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved			Parallel Detection Fault	Link Partner Next Page Able	Next Page Able	Page Received	Link Partner Auto-Neg Able

BIT	NAME	TYPE	RESET	DESCRIPTION
15:5	Reserved	Read Only	000 0000 0000	
4	Parallel Detection Fault	Read Only	0	When set, this bit indicates an error condition in which both the 10BASE-T and 100BASE-TX links came up valid, or that one of the technologies established a link but was unable to maintain the link. This bit is self-clearing.
3	Link Partner Next Page Able	Read Only	0	When set, this bit indicates that the link partner is capable of Next Page exchange.
2	Next Page Able	Read Only	1	This bit is a status bit which indicates to the Management Layer that the CS8952 supports Next Page capability. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
1	Page Received	Read Only	0	When set, this bit indicates that a valid word of auto-negotiation data has been received and its integrity verified. The first page of data will consist of the Base Page, and all successive pages will consist of Next Page data. This bit is self-clearing.
0	Link Partner Auto-Neg Able	Read Only	0	When set, this bit indicates that the link partner has auto-negotiation capability.

6.8 *Auto-Negotiation Next-Page Transmit Register - Address 07h*

15	14	13	12	11	10	9	8
Next Page	Acknowledge	Message Page	Acknowledge 2	Toggle	Message/Unformatted Code Field		

7	6	5	4	3	2	1	0
Message/Unformatted Code Field							

BIT	NAME	TYPE	RESET	DESCRIPTION
15	Next Page	Read/Write	0	When set, this bit indicates that more Next Pages follow. When clear, the current page is the last page of data to be sent. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
14	Acknowledge	Read Only	0	This bit is used for Link Code Word verification. When set, it indicates that consistent data has been successfully read from the link partner.
13	Message Page	Read/Write	1	When set, this bit indicates that the data in the Message/Unformatted Code Field is one of the predefined message pages. When low, the data is unformatted data. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
12	Acknowledge 2	Read/Write	0	When set, this bit indicates to the link partner that the CS8952 can comply with the last received message. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
11	Toggle	Read Only	0	This bit is used to maintain synchronization with the link partner during Next Page exchange.
10:0	Message/Unformatted Code Field	Read/Write	000 0000 0001	This field contains the 11 bit data for the Message or Unformatted Page. It defaults to the Null Message. **Note:** This field is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.

6.9 Interrupt Mask Register - Address 10h

15	14	13	12	11	10	9	8
CIM Link Unstable	Link Status Change	Descrambler Lock Change	Premature End Error	DCR Rollover	FCCR Rollover	RECR Rollover	Remote Loopback Fault
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset Complete	Jabber Detect	Auto-Neg Complete	Parallel Detection Fault	Parallel Fail	Remote Fault	Page Received	Reserved

This register indicates which events will cause an interrupt event on the $\overline{\text{MII\_IRQ}}$ pin. Each bit acts as an enable to the interrupt. Thus, when set, the event will cause the $\overline{\text{MII\_IRQ}}$ pin to be asserted. When clear, the event will not affect the $\overline{\text{MII\_IRQ}}$ pin, but the status will still be reported via the Interrupt Status Register (address 11h).

BIT	NAME	TYPE	RESET	DESCRIPTION
15	CIM Link Unstable	Read/Write	0	When set, an interrupt will be generated if an unstable link condition is detected by the Carrier Integrity Monitor function. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
14	Link Status Change	Read Write	1	When set, an interrupt will be generated each time the CS8952 detects a change in the link status. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
13	Descrambler Lock Change	Read/Write	0	When set, an interrupt will be generated each time the 100BASE-TX receive descrambler loses or regains synchronization with the far-end. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
12	Premature End Error	Read/Write	0	When set, an interrupt will be generated when two consecutive IDLES are detected in a 100BASE-TX frame without the ESD sequence. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.

BIT	NAME	TYPE	RESET	DESCRIPTION
11	DCR Rollover	Read/Write	0	When set, an interrupt will be generated if the MSB in the DCR counter becomes set. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
10	FCCR Rollover	Read/Write	0	When set, an interrupt will be generated if the MSB in the FCCR counter becomes set. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
9	RECR Rollover	Read/Write	0	When set, an interrupt will be generated if the MSB in the RECR counter becomes set. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
8	Remote Loopback Fault	Read/Write	0	When set, an interrupt will be generated if the elastic buffer in the PMA is under-run or over-run during Remote Loopback. This should not occur for normal length 802.3 frames. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
7	Reset Complete	Read/Write	1	When set, an interrupt will be generated once the digital and analog sections have been reset, and a calibration cycle has been performed. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
6	Jabber Detect	Read/Write	0	When set, an interrupt will be generated when a Jabber condition is detected by the 10BASE-T MAU. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.

BIT	NAME	TYPE	RESET	DESCRIPTION
5	Auto-Neg Complete	Read/Write	0	When set, an interrupt will be generated once auto-negotiation has completed successfully. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
4	Parallel Detection Fault	Read/Write	0	When set, an interrupt will be generated if auto-negotiation determines that unstable legacy link signaling was received. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
3	Parallel Fail	Read/Write	0	When set, an interrupt will be generated when parallel detection has occurred for a technology that is not currently advertised by the local device. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
2	Remote Fault	Read/Write	0	When set, an interrupt will be generated if a remote fault condition is detected either by auto-negotiation or by the Far-End Fault Detect state machine. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
1	Page Received	Read/Write	0	When set, an interrupt is generated each time a page is received during auto-negotiation. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
0	Reserved	Read Only	0	

6.10 Interrupt Status Register - Address 11h

15	14	13	12	11	10	9	8
CIM Link Unstable	Link Status Change	Descrambler Lock Change	Premature End Error	DCR Rollover	FCCR Rollover	RECR Rollover	Remote Loopback Fault
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset Complete	Jabber Detect	Auto-Neg Complete	Parallel Detection Fault	Parallel Fail	Remote Fault	Page Received	Reserved

This register indicates which event(s) caused an interrupt event on the $\overline{\text{MII\_IRQ}}$ pin. All bits are self-clearing, and will thus be cleared upon readout.

BIT	NAME	TYPE	RESET	DESCRIPTION
15	CIM Link Unstable	Read Only	0	When set, this bit indicates that an unstable link condition was detected by the Carrier Integrity Monitor function.
14	Link Status Change	Read Only	0	When set, this bit indicates that a change has occurred to the status of the link. The Self Status Register (address 19h) may be read to determine the current status of the link.
13	Descrambler Lock Change	Read Only	0	When set, this bit indicates that a change has occurred in the status of the descrambler. The Self Status Register (address 19h) may be read to determine the current status of the scrambler lock.
12	Premature End Error	Read Only	0	This bit is set when a premature end of frame is detected for 100 Mb/s operation. A premature end is defined as two consecutive IDLE patterns detected in a frame prior to the End of Stream Delimiter.
11	DCR Rollover	Read Only	0	This bit is set when the MSB of the Disconnect Count Register (address 12h) becomes set. This should provide ample warning to the management layer so that the DCR may be read before rolling over.
10	FCCR Rollover	Read Only	0	This bit is set when the MSB of the False Carrier Count Register (address 13h) becomes set. This should provide ample warning to the management layer so that the FCCR may be read before saturating.
9	RECR Rollover	Read Only	0	This bit is set when the MSB of the Receive Error Count Register (address 15h) becomes set. This should provide ample warning to the management layer so that the RECR may be read before rolling over.

BIT	NAME	TYPE	RESET	DESCRIPTION
8	Remote Loopback Fault	Read Only	0	When set, this bit indicates that the Elastic Buffer has detected an over-run or an under-run condition. In any case, the frame generating this fault will be terminated. This should never happen since the depth of the elastic buffer (10 bits) is greater than twice the maximum number of bit times the receive and transmit clocks may slip during a maximum length packet assuming clock frequency tolerances of 100 ppm or less.
7	Reset Complete	Read Only	0	When set, this bit indicates that the internal analog calibration cycle has completed, and all analog and digital circuitry is ready for normal operation.
6	Jabber Detect	Read Only	0	In 10BASE-T mode, if the last transmission is longer than 105 ms, then the packet output is terminated by the jabber logic and this bit is set. This bit is implemented with a latching function so that the occurrence of a jabber condition causes it to become set until it is cleared by a read to this register, a read to the Basic Mode Status Register (address 01h), or a reset. No jabber detect function has been defined for 100BASE-TX. This bit is the same as in the Basic Mode Status Register (address 01h).
5	Auto-Neg Complete	Read Only	0	This bit is set when the auto-negotiation process has completed. This is an indication that the Auto-Negotiation Advertisement Register (address 04h), the Auto-Negotiation Link Partner Ability Register (address 05h), and the Auto-Negotiation Expansion Register (address 06h) are valid. This bit is the same as in the Basic Mode Status Register (address 01h).
4	Parallel Detection Fault	Read Only	0	When set, this bit indicates an error condition in which auto-negotiation has detected that unstable 10BASE-T or 100BASE-TX link signalling was received. This bit is self-clearing. This bit is the same as in the Auto-Negotiation Expansion Register (address 06h)
3	Parallel Fail	Read Only	0	When set, this bit indicates that a parallel detection has occurred for a technology that is not currently advertised by the local device.

BIT	NAME	TYPE	RESET	DESCRIPTION
2	Remote Fault	Read Only	0	When auto-negotiation is enabled, this bit is set if the Remote Fault bit is set in the Auto-Negotiation Link Partner Ability Register (address 05h). When auto-negotiation is disabled, this bit will be set when the Far-End Fault Indication for 100BASE-TX is detected.
1	Page Received	Read Only	0	When set, this bit indicates that a valid word of auto-negotiation data has been received and its integrity verified. The first page of data will consist of the Base Page, and all successive pages will consist of Next Page data. This bit is self-clearing. This bit is the same as in the Auto-Negotiation Expansion Register (address 06h).
0	Reserved	Read Only	0	

6.11 Disconnect Count Register - Address 12h

15	14	13	12	11	10	9	8
Disconnect Counter							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Disconnect Counter							

BIT	NAME	TYPE	RESET	DESCRIPTION
15:0	Disconnect Counter	Read/Write	0000h	This field contains a count of the number of times the CS8952 has lost a Link OK condition. This counter is cleared upon readout and will roll-over to 0000h.

6.12 False Carrier Count Register - Address 13h

15	14	13	12	11	10	9	8
False Carrier Counter							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
False Carrier Counter							

BIT	NAME	TYPE	RESET	DESCRIPTION
15:0	False Carrier Counter	Read Only	0000h	This field contains a count of the number of times the CS8952 has detected a false-carrier -- that is, the reception of a poorly formed Start-of-Stream Delimiter (SSD). The counter is incremented at the end of such events to prevent multiple increments. This counter is cleared upon readout and will saturate at FFFFh.

6.13 Scrambler Key Initialization Register - Address 14h

15	14	13	12	11	10	9	8
Load	Reserved				Scrambler Initialization Key		

7	6	5	4	3	2	1	0
Scrambler Initialization Key							

BIT	NAME	TYPE	RESET	DESCRIPTION
15	Load	Read/Set	0	When this bit is set, the scrambler will be loaded with the value in the Scrambler Initialization Key field. When the load is complete, this bit will clear automatically.
14:11	Reserved	Read Only	0000	These bits should be read as don't cares and, when written, should be written to 0.
10:0	Scrambler Initialization Key	Read/Write	Reset value is dependent on the PHY Address field of the Self Status Register (address 19h).	This field allows the Scrambler to be loaded with a user-definable key sequence. A value of 000h has the effect of bypassing the scrambler function. This is valuable for testing purposes to allow a deterministic response to test stimulus without a synchronization delay. **Note:** This field is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.

6.14 Receive Error Count Register - Address 15h

15	14	13	12	11	10	9	8
Receive Error Counter							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Receive Error Counter							

BIT	NAME	TYPE	RESET	DESCRIPTION
15:0	Receive Error Counter	Read Only	0000h	This counter increments for each packet in which one or more receive errors is detected that is not due to a collision event. This counter is cleared upon readout and will roll-over to 0000h.

6.15 Descrambler Key Initialization Register - Address 16h

15	14	13	12	11	10	9	8
Load	Reserved				Descrambler Initialization Key		

7	6	5	4	3	2	1	0
Descrambler Initialization Key							

BIT	NAME	TYPE	RESET	DESCRIPTION
15	Load	Read/Set	0	When this bit is set, the descrambler will be loaded with the value in the Descrambler Initialization Key field. When the load is complete, this bit will clear automatically.
14:11	Reserved	Read Only	0000	These bits should be read as don't cares and, when written, should be written to 0.
10:0	Descrambler Initialization Key	Read/Write	Reset value is dependent on the PHY Address field of the Self Status Register (address 19h).	This register allows the Descrambler to be loaded with a user-definable key sequence. A value of 000h has the effect of bypassing the descrambler function. This is valuable for testing purposes to allow a deterministic response to test stimulus without a synchronization delay. **Note:** This field is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.

6.16 PCS Sub-Layer Configuration Register - Address 17h

15	14	13	12	11	10	9	8
NRZI Enable	Time-Out Select	Time-Out Disable	Repeater Mode	LED5 Mode	Unlock Regs	MR Preamble Enable	Fast Test
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLK25 Disable	Enable LT/100	CIM Disable	Tx Disable	Rx Disable	LED1 Mode	LED4 Mode	Digital Reset

BIT	NAME	TYPE	RESET	DESCRIPTION
15	NRZI Enable	Read/Write	1	When this bit is set, the NRZI encoder and decoder are enabled. When this bit is clear, NRZI encoding and decoding are disabled.
14	Time-Out Select	Read/Write	0	When this bit is set, the time-out counter in the receive descrambler is set to time-out after 2 ms without IDLES. When clear the counter is set to time-out after 722 µs without IDLES.
13	Time-Out Disable	Read/Write	0	When this bit is set, the time-out counter in the receive descrambler is disabled. When this bit is clear, the time-out counter is enabled.
12	Repeater Mode	Read/Write	Reset to the value on the REPEATER pin.	This bit defines the mode of the Carrier Sense (CRS) signal. When this bit is set, CRS is asserted due to receive activity only. When this bit is clear, CRS is asserted due to either transmit or receive activity.
11	LED5 Mode	Read/Write	0	This bit defines the mode of Pin $\overline{\text{LED5}}$. When this bit is set, pin $\overline{\text{LED5}}$ indicates the synchronization status of the 100BASE-TX descrambler. When this bit is clear, $\overline{\text{LED5}}$ indicates a collision. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
10	Unlock Regs	Read/Write	0	When set, this bit unlocks certain read only control registers for factory testing. Leave clear for proper operation. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.

BIT	NAME	TYPE	RESET	DESCRIPTION
9	MF Preamble Enable	Read/Write	0	When set, this bit will force all management frames (via MDIO, MDC) to be preceded by a 32 bit preamble pattern of contiguous ones to be considered valid. When cleared, it allows management frames with or without the preamble pattern. The status of this register is (inversely) reflected in the MF Preamble bit in the Basic Mode Status Register (address 01h). **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
8	Fast Test	Read/Write	0	When set, internal timers are sped up significantly in order to facilitate production test. Leave clear for proper operation. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
7	CLK25 Disable	Read/Write	When TCM pin is low, reset to 1; otherwise, reset to 0	Setting this bit will disable (tri-state) the CLK25 output pin, reducing digital noise and power consumption.
6	Enable LT/100	Read/Write	1	When set, normal link status checking is enabled. When clear, this bit forces the link status to Link OK (at 100 Mb/s), and will assert the LINK_OK LED.
5	CIM Disable	Read/Write	Reset to the logic inverse of the value on the REPEATER pin.	When set, this bit forces the Carrier Integrity Monitor function to be disabled. When low, the Carrier Integrity Monitor function is enabled, and detection of an unstable link will disable the receive and transmit functions.
4	Tx Disable	Read/Write	0	When set, this bit forces the 10 Mb/s and 100 Mb/s outputs to be inactive. When clear, normal transmission is enabled. If Tx Disable is set while a packet is being transmitted, transmission is completed and no subsequent packets are transmitted until Tx Disable is cleared again. Also, if Tx Disable is cleared while TX_EN is high, the transmitter will remain disabled until TX_EN is deasserted. This prevents fragments from being transmitted onto the network.

BIT	NAME	TYPE	RESET	DESCRIPTION
3	Rx Disable	Read/Write	0	When set, the receiver is disabled and no incoming packets pass through the receiver. The link will remain established and, if operating at 100 Mb/s, the descrambler will remain locked. When clear, the receiver is enabled. If Rx Disable is set while a packet is being received, reception is completed and no subsequent receive packets are allowed until Rx Disable is cleared again. Also, if Rx Disable is cleared while a packet is being received, the receiver will remain disabled until the end of the incoming packet. This prevents fragments from being sent to the MAC. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
2	LED1 Mode	Read/Write	0	This bit defines the mode of Pin $\overline{\text{LED1}}$. When this bit is set, pin $\overline{\text{LED1}}$ indicates Carrier Integrity Monitor status as determined by the CIM Status bit in the Self Status Register (address 19h). When this bit is clear, $\overline{\text{LED1}}$ indicates 10 Mb/s or 100 Mb/s transmission activity.
1	LED4 Mode	Read/Write	0	This bit defines the mode of Pin $\overline{\text{LED4}}$. When this bit is set, pin $\overline{\text{LED4}}$ indicates full duplex mode for 10 Mb/s or 100 Mb/s. When this bit is clear, $\overline{\text{LED4}}$ indicates Polarity in 10 Mb/s mode or full-duplex in 100 Mb/s mode.
0	Digital Reset	Read/Write	0	When set, this bit will reset all digital logic and registers to their initial values. The analog circuitry will not be affected. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.

6.17 Loopback, Bypass, and Receiver Error Mask Register - Address 18h

15	14	13	12	11	10	9	8
Bad SSD Enable	Bypass 4B5B	Bypass Scrambler	Bypass Symbol Alignment	ENDEC Loopback	FX Drive	Remote Loopback	PMD Loopback
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Strip Preamble	Alternate FDX CRS	Loopback Transmit Disable	Code Error Report Select	Premature End Error Report Select	Link Error Report Enable	Packet Error Report Enable	Code Error Report Enable

BIT	NAME	TYPE	RESET	DESCRIPTION
15	Bad SSD Enable	Read/Write	1	When set, this bit enables the reporting of a bad SSD (False-Carrier event) on the MII. These events will be reported by setting RX_ER=1, RX_DV=0, and RXD[3:0]=1110. If the 4B5B encoders are being bypassed, this event will be reported by setting RX_DV=0 and RXD[4:0]=11110. If symbol alignment is bypassed, the CS8952 does not detect carrier, and thus will not report bad SSD events.
14	Bypass 4B5B	Read/Write	Reset to the value on the BP4B5B pin.	When set, this bit causes the receive 5B4B decoder and the transmit 4B5B encoder to be bypassed.
13	Bypass Scrambler	Read/Write	Reset to the value on the BPSCR pin.	When set, this bit causes the receive descrambler and the transmit scrambler blocks to be bypassed, and the CS8952 accepts NRZI data from an external 100BASE-FX optical module through pins RX_NRZ+ and RX_NRZ-.
12	Bypass Symbol Alignment	Read/Write	Reset to the value on the BPALIGN pin.	When set, this bit causes the following functions to be bypassed: receiver descrambling, symbol alignment and decoding, transmit symbol encoding, and transmit scrambling.
11	ENDEC Loopback	Read/Write	0	When set, the 10BASE-T internal Manchester encoder output is connected to the decoder input. When clear, the CS8952 is configured for normal operation.
10	FX Drive	Read/Write	0	This bit controls the drive strength of the 100BASE-FX PECL interface drivers. When clear, the drivers are optimized for a 50 Ω load. When set, the drivers are optimized for a 150 Ω load.
9	Remote Loopback	Read/Write	0	When set, data received from the link is looped back at the MII and sent back out to the link. Received data will be presented on the MII pins. Transmit data at the MII will be ignored. **Note:** Setting Remote Loopback and PMD Loopback simultaneously will cause neither loopback mode to be entered, and should not be done.

BIT	NAME	TYPE	RESET	DESCRIPTION
8	PMD Loopback	Read/Write	0	When set, the scrambled NRZI transmit data is connected directly to the NRZI receive port on the descrambler. The loopback includes all of the 100BASE-TX functionality except for the MLT-3 encoding/decoding and the analog line-interface blocks. When clear, the CS8952 is configured for normal operation. **Note:** Setting Remote Loopback and PMD Loopback simultaneously will cause neither loopback mode to be entered, and should not be done.
7	Strip Preamble	Read/Write	0	When set this bit causes the 7 bytes of MAC preamble to be stripped off of incoming 100 Mb/s frames. The data received across the MII will begin with the 1 byte Start of Frame Delimiter (SFD). **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.
6	Alternate FDX CRS	Read/Write	0	This bit changes the behavior of the CRS pin only in the full-duplex (FDX) mode of operation. When set, CRS will be asserted for transmit data only. When clear, CRS will be asserted only for receive data.
5	Loopback Transmit Disable	Read/Write	1	This bit controls whether loopback data is transmitted onto the network. When set, any data transmitted during PMD or ENDEC loopback mode will NOT be transmitted onto the network. When clear, data will be transmitted on the TX+/- pins as well as looped back onto the MII pins.
4	Code Error Report Select	Read/Write	0	When set, this bit causes code errors to be reported by a value of 5h on RXD[3:0] and the assertion of RX_ER. When clear, this bit causes code errors to be reported by a value of 6h on RXD[3:0] and the assertion of RX_ER. This bit is superseded by the Code Error Report Enable bit.
3	Premature End Error Report Select	Read/Write	0	When set, this bit causes premature end errors to be reported by a value of 4h on RXD[3:0] and the assertion of RX_ER. When clear, this bit causes premature end errors to be reported by a value of 6h on RXD[3:0] and the assertion of RX_ER. A premature end error is caused by the detection of two IDLE symbols in the 100 Mb/s receive data stream prior to the End of Stream Delimiter.

BIT	NAME	TYPE	RESET	DESCRIPTION
2	Link Error Report Enable	Read/Write	0	When set, this bit causes link errors to be reported by a value of 3h on RXD[3:0] and the assertion of RX_ER. When clear, link errors are not reported across the MII.
1	Packet Error Report Enable	Read/Write	0	When set, this bit causes packet errors to be reported by a value of 2h on RXD[3:0] and the assertion of RX_ER. When clear, packet errors are not reported across the MII.
0	Code Error Report Enable	Read/Write	0	When set, code errors are reported and transmitted on RXD[3:0]. When clear, this bit enables the Code Error Report values on RXD[3:0] as selected by the Code Error Report Select bit and also causes the assertion of TX_ER to transmit a HALT code group. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit of the 10BASE-T Configuration Register (address 1Ch) is set.

6.18 Self Status Register - Address 19h

15	14	13	12	11	10	9	8
Link OK	Power Down	Receiving Data	Descrambler Lock	Disable CRS on Time-out	Auto-Neg Enable Status	PAUSE	FEFI Enable
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Full Duplex	10BASE-T Mode	CIM Status	PHY Address				

BIT	NAME	TYPE	RESET	DESCRIPTION
15	Link OK	Read Only	0	When set, this bit indicates that a valid link connection has been detected. The type of link established may be determined from bits 6, 7, and 9. When clear, this bit indicates that a valid link connection does not exist. This bit may be used to determine the current status of the link.
14	Power Down	Read Only	1	When high, this bit indicates that the CS8952 is in a low power state.
13	Receiving Data	Read Only	0	This bit is high whenever the CS8952 is receiving valid data. It is a direct copy of the state of the RX_DV pin accessible by software.
12	Descrambler Lock	Read Only	0	When high, this bit indicates that the descrambler has successfully locked to the scrambler seed of the far-end transmitter and is able to descramble received data.
11	Disable CRS on Time-out	Read/Write	Reset to the logic inverse of the value on the REPEATER pin.	This bit controls the state of the CRS pin upon a descrambler time-out. When set, CRS will be forced low upon a descrambler time-out, and will not be released until the descrambler has re-acquired synchronization.
10	Auto-Neg Enable Status	Read Only	If auto-negotiation is enabled via the AN[1:0] pins, reset to 1; otherwise, reset to 0.	This bit reflects the value of bit 12 in the Basic Mode Control Register (address 00h). When set, it indicates that auto-negotiation has been enabled. When clear, this bit indicates that the mode of the CS8952 has been forced to that indicated by bits 6, and 7.
9	PAUSE	Read Only	0	When set, this bit indicates that the Flow-Control PAUSE function has been negotiated. This indicates that both the local device and the link partner have advertised this capability.
8	FEFI Enable	Read/Write	0	This bit controls the Far-End Fault Generate and Detect state machines. When this bit is set and auto-negotiation is disabled (bit 10 is clear), both state machines are enabled. When clear, this bit disables both state machines.
7	Full Duplex	Read Only	If a full duplex mode is enabled via the AN[1:0] pins, reset to 1; otherwise, reset to 0.	When set, this bit indicates that the CS8952 has been configured for Full-Duplex operation.
6	10BASE-T Mode	Read Only	0	When set, this bit indicates that the CS8952 has been configured for 10 Mb/s operation.

BIT	NAME	TYPE	RESET	DESCRIPTION
5	CIM Status	Read Only	0	When clear, this bit indicates that a stable link connection has been detected. When an unstable link is detected and the Carrier Integrity Monitor Disable bit in the PCS Sub-Layer Configuration Register (address 17h) is clear, this bit is set and latched. It will remain set until this register is read.
4:0	PHY Address Field	Read/Write	Reset to the values on the PHYAD[4:0] pins.	The value on pins PHYAD[4:0] are latched into this field at power-up or reset. These bits define the PHY address used by the management layer to address the PHY. The external logic must know this address in order to select this particular CS8952's registers individually via the MDIO and MDC pins.

6.19 10BASE-T Status Register - Address 1Bh

15	14	13	12	11	10	9	8
Reserved					Polarity OK	10BASE-T Serial	Reserved

7	6	5	4	3	2	1	0
Reserved							

BIT	NAME	TYPE	RESET	DESCRIPTION
15:11	Reserved	Read Only	0 0000	
10	Polarity OK	Read Only	0	When high, the polarity of the receive signal (at the RXD+/RXD- inputs) is correct. If clear, the polarity is reversed. If the Polarity Disable bit of 10BASE-T Configuration Register (address 1Ch) is clear, then the polarity is automatically corrected, if needed. The Polarity OK status bit shows the true state of the incoming polarity independent of the Polarity Disable bit.
9	10BASE-T Serial	Read/Write	Reset to the value on the 10BT_SER pin.	When set, this bit selects 10BASE-T serial mode. When low, this bit selects 10BASE-T nibble mode. This bit will only affect the CS8952 if it has been configured for 10 Mb/s operation.
8:0	Reserved	Read Only	0 0000 0000	

6.20 10BASE-T Configuration Register - Address 1Ch

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
National Compatibility Mode	LED3 Blink Enable	Enable LT/10	SQE Enable	Reserved	Low Rx Squelch	Polarity Disable	Jabber Enable

BIT	NAME	TYPE	RESET	DESCRIPTION
15:8	Reserved	Read Only	0000 0000	
7	National Compatibility Mode	Read/Write	1	When set, registers and bits that are not compatible with the National DP83840 are disabled and writes to these registers are ignored.
6	LED3 Blink Enable	Read/Write	0	When set, LED3 will blink during auto-negotiation and will indicate Link Good status upon completion of auto-negotiation. When clear, LED3 indicates Link Good status only. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit (bit 7) is set.
5	Enable LT/10	Read/Write	1	When set, this bit enables the transmission of link pulses. When clear, link pulses are disabled and a good link condition is forced. If link pulses are disabled during 100 Mb/s operation with auto-negotiation enabled, the CS8952 will go into 10 Mb/s mode. If operating in 100 Mb/s mode with no auto-negotiation, then clearing this bit has no effect.
4	SQE Enable	Read/Write	Reset to the logic inverse of the value on the REPEATER pin.	When set, and if the CS8952 is in half-duplex mode, this bit enables the 10BASE-T SQE function. When the part is in repeater mode, this bit is cleared and may not be set.
3	Reserved	Read Only	1	This bit should be read as a don't care and, when written, should be written to 1.
2	Low Rx Squelch	Read/Write	0	When clear, the 10BASE-T receiver squelch thresholds are set to levels defined by the ISO/IEC 8802-3 specification. When set, the thresholds are reduced by approximately 6 dB. This is useful for operating with "quiet" cables that are longer than 100 meters.
1	Polarity Disable	Read/Write	0	The 10BASE-T receiver automatically determines the polarity of the received signal at the RXD+/RXD- input. When this bit is clear, the polarity is corrected, if necessary. When set, no effort is made to correct the polarity. Polarity correction will only be performed during 10BASE-T packet reception. **Note:** This bit is disabled, and writes to this bit are ignored when the National Compatibility Mode bit (bit 7) is set.

BIT	NAME	TYPE	RESET	DESCRIPTION
0	Jabber Enable	Read/Write	1	When set, the jabber function is enabled. When clear, and if the CS8952 is in 10BASE-T full-duplex or 10BASE-T ENDEC loopback mode, the jabber function is disabled. **Note:** When the National Compatibility Mode bit (bit 7) is set, the Jabber function may also be disabled for 10BASE-T half-duplex, although this is not recommended.

7. DESIGN CONSIDERATIONS

The CS8952 is a mixed-signal device containing the high-speed digital and analog circuits required to implement Fast Ethernet communication. It is important the designer adhere to the following guidelines and recommendations for proper and reliable operation of the CS8952. These guidelines will also benefit the design with good EMC performance.

7.1 Twisted Pair Interface

The recommended connection of the twisted-pair interface is shown if Figure **6**. The unused cable pairs are terminated to increase the common-mode performance. Common-mode performance is also improved by connecting the center taps of the RX and TX input circuits to the DC-isolated ground plane. The 0.01 µF capacitor C1 must provide 2KV (1,500 Vrms for 60 seconds) of isolation to meet 802.3 requirements. If a shielded RJ45 connector is used (recommended), the shield should be connected to chassis ground.

7.2 100BASE-FX Interface

Figure **7** shows the recommended connection for a 100BASE-FX interface to a Hewlett-Packard HFBR-5103 fiber transceiver. Termination circuitry may need to be revised for other fiber transceivers. The FX Drive bit in the Loopback, Bypass, and Receiver Error Mask Register (address 18h) may be used to tailor the PECL interface for 50 Ω or 150 Ω loads.

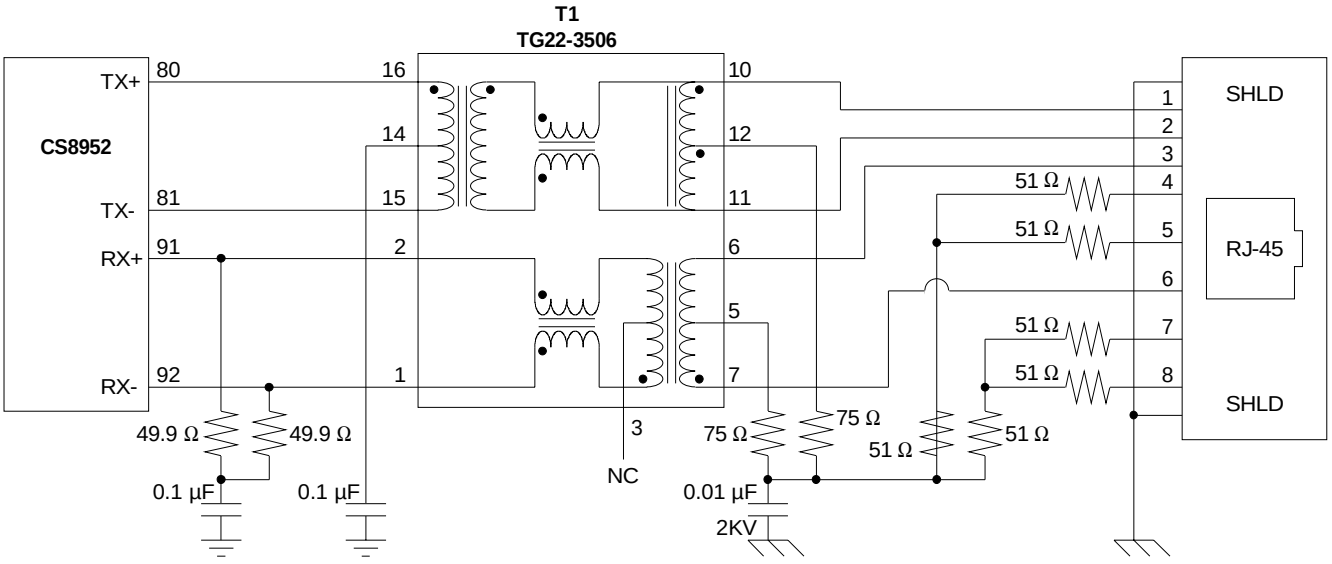


Figure 6. Recommended Connection of Twisted-Pair Ports (Network Interface Card)

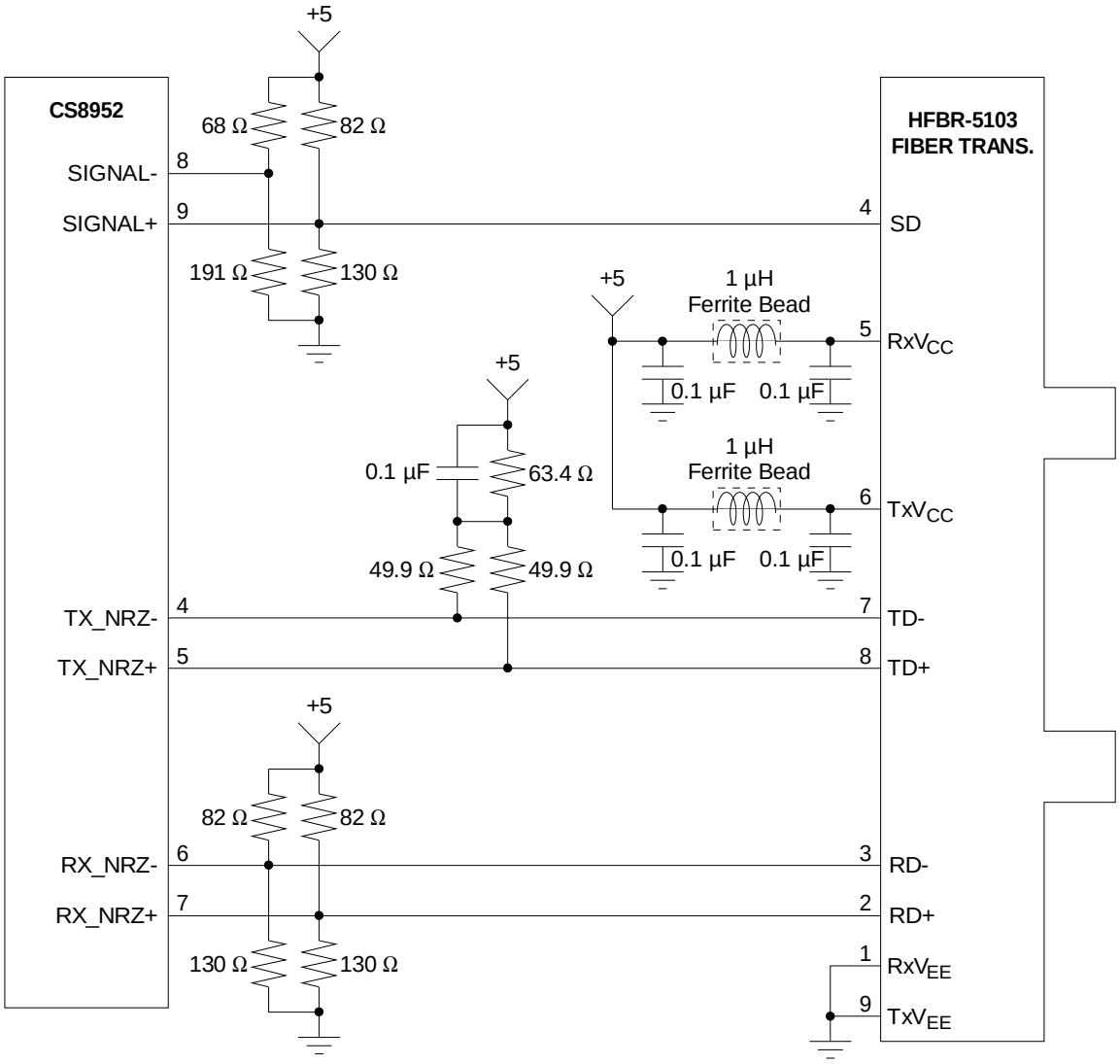


Figure 7. Recommended Connection of Fiber Port

TX_NRZ+/- termination components should be placed as close to the fiber transceiver as possible, while RX_NRZ+/- and SIGNAL+/- termination components should be placed close to the CS8952.

The CS8952 100BASE-FX interface IO pins (TX_NRZ+, TX_NRZ-, RX_NRZ+, RX_NRZ-, SIGNAL+, and SIGNAL-) may be left unconnected if a fiber interface is not used.

7.3 Internal Voltage Reference

A 4.99 kΩ biasing resistor must be connected between the CS8952 RES pin and ground. This resistor biases the internal analog circuits of the CS8952 and should be placed as close as possible to RES pin. Connect the other end of this resistor directly to the ground plane. Connect the adjacent CS8952 ground pins (pins 85 and 87) to the grounded end of the resistor forming a “shield” around the RES connection.

7.4 Clocking Schemes

The CS8952 may be clocked using one of three possible schemes: using a 25 MHz crystal and the internal oscillator, using an external oscillator sup-

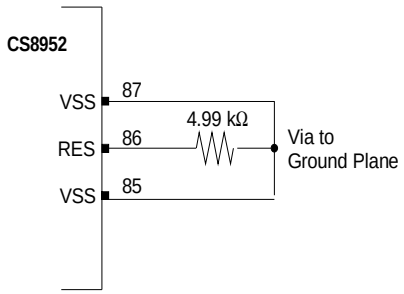


Figure 8. Biasing Resistor Connection and Layout

plied through the XTAL_I pin, or using an external clock source supplied through the TX_CLK pin.

When a 25 MHz crystal is used, it should be placed within one inch of the XTAL_I and XTAL_O pins of the CS8952. The crystal traces should be short, have no vias, and run on the component side. Table **7** lists examples of manufacturers of suitable crystals. The designer should evaluate their crystal selection for suitability in their specific design.

An external CMOS clock source may be connected to the XTAL_I pin, with the XTAL_O pin left open. The input capacitance of the XTAL_I pin is larger than the other inputs (a maximum of 35pF), since it includes the additional load capacitance of the crystal oscillator. Care should be taken to assure any external clock source attached to XTAL_I is capable of driving higher capacitive loads. The clock signal should be 25 MHz ±0.01% with a duty cycle between 45% and 55%.

When the XTAL_I pin load is a problem, or only a TTL level clock source is available, the CS8952 can be clocked through the TX_CLK pin, providing the TX_CLK mode is set appropriately using the TCM pin. The clock frequency will be dependent on the operating mode.

7.5 Recommended Magnetics

The CS8952 requires an isolation transformer with a 1:1 turns ratio for both the transmit and receive signals. Table **7** lists examples of manufacturers with transformers meeting these requirements. However, the designer should evaluate the magnetics for suitability in their specific design.

7.6 Power Supply and Decoupling

The CS8952 supports connection to either a 3.3 V or 5.0 V MII. When connected to a +5.0 V MII, all power pins should be provided +5.0 V +/- 5%, and all signal inputs should be referenced to +5.0V. When interfaced with a 3.3 V MII, VDD_MII power pins should be provided +3.3 V +/- 5%, VDD power pins should be provided +5.0 V +/- 5%, and all signal inputs should be referenced to +3.3 V.

Component	Manufacturer	Part Number
Crystal	Raltron Electronics Corp. 10651 NW 19th St. Miami, FL 33172 (305) 593-6033 www.raltron.com	AS-25.000-15-F-EXT-SMD-TR-CIR
Transformer	Halo Electronics, Inc. P.O. Box 5826 Redwood City, CA 94063 USA (650) 568-5800 www.haloelectronics.com	TG22-3506ND
	Bel Fuse, Inc. 198 Van Vorst Street Jersey City, NJ 07302 USA (201) 432-0463 www.belfuse.com	S5558-5999-46
	Pulse Engineering 12220 World Trade Drive San Diego, CA 92128 USA (619) 674-8100 www.pulseeng.com	PE-68515
Fiber Interface	Hewlett Packard Component Sales Response Center (408) 654-8675 www.hp.com/HP-COMP	HFBR-5103

Table 7. Support Component Manufactures

Each CS8952 power pin should be connected to a 0.1 µF bypass capacitor and then to the power plane. The bypass capacitors should be located as close to its corresponding power pin as possible. Connect ground pins directly to the ground plane.

7.7 General Layout Recommendations

The following PCB layout recommendations will help ensure reliable operation of the CS8952 and good EMC performance.

- Use a multilayer Printed Circuit Board with at least one ground and one power plane. A typical +5V MII application would be as follows:

  Layer 1: (top) Components and first choice signal routing
  Layer 2: Ground
  Layer 3: Power (+5V)
  Layer 4: (bottom) Second choice signal routing, bypass components
- Place transformer TI as close to the RJ45 connector as possible with the secondary (network) side facing the RJ45 and the primary (chip) side facing the analog side (pins 76-100) of CS8952. Place the CS8952 in turn as close to T1 as possible.
- Use the bottom layer for signal routing as a second choice. You may place all components on the top layer. However, bypass capacitors are optimally placed as close to the chip as possible and may be best located underneath the CS8952 on the bottom layer. Termination components at the RJ-45 and fiber transceiver may also be optimally placed on the bottom layer.
- Connect a 0.1 µF bypass capacitor to each CS8952 VDD and VDD_MII pin. Place it as close to its corresponding power pin as possible and connect the other lead directly to the ground plane.
- The 4.99K reference resistor should be placed as close to the RES pin as possible. Connect the other end of this resistor to the ground plane using a via. Connect the adjacent VSS pins (pins 85 and 87) to the grounded end of the resistor forming a shield as illustrated in Figure **8**.
- Controlled impedance is necessary for critical signals TX+/-, RX+/-, TX_NRZ+/-, and RX_NRZ+/-. These should be run as microstrip transmission lines (100 Ω differential, 50 Ω single-ended). The MII signals should be 68 Ω microstrip transmission lines. (For short MII signal paths one may standardize on a given trace width for all traces without significant degradation in signal integrity.)
- Avoid routing traces other than the TX and RX signals under transformer T1 and the RJ45 connector. Signals may run on the bottom side underneath the CS8952 as long as they stay away from critical analog traces.
- Connect all CS8952 ground and power pins directly to the ground and power planes, respectively. Note: The VDD_MII power pins may need their own power plane or plane segment in +3.3 V MII applications.
- Depending on the orientation and location of the transformer, the CS8952, and the RJ-45, and on whether the application is for a NIC or a switch, the RX and TX pairs may need to cross. This should be done by changing layers on a pair by pair basis only, using the minimum number of vias, and making sure that each trace within a pair “sees” the same path as its peer.

  Figure **6** shows the CS8952 in a NIC or adapter configuration. It may be configured for a hub or repeater application by changing the wiring to the RJ-45 as shown in Table **8**.
- Differential pair transmission lines should be routed close together (one trace width spacing edge-to-edge) and kept at least two trace widths away from other traces, components, etc. TX and RX pairs should be routed away from each other and may use opposite sides of the PCB as necessary, Each member of the differential pair should “see” the same PCB terrain as its peer.
- Unused spaces on the signal layers should be filled with ground fill (pour). Vias should connect the ground patches to the ground plane. This is especially recommended (symmetrical-

ly) on both sides of the TX+/- traces.

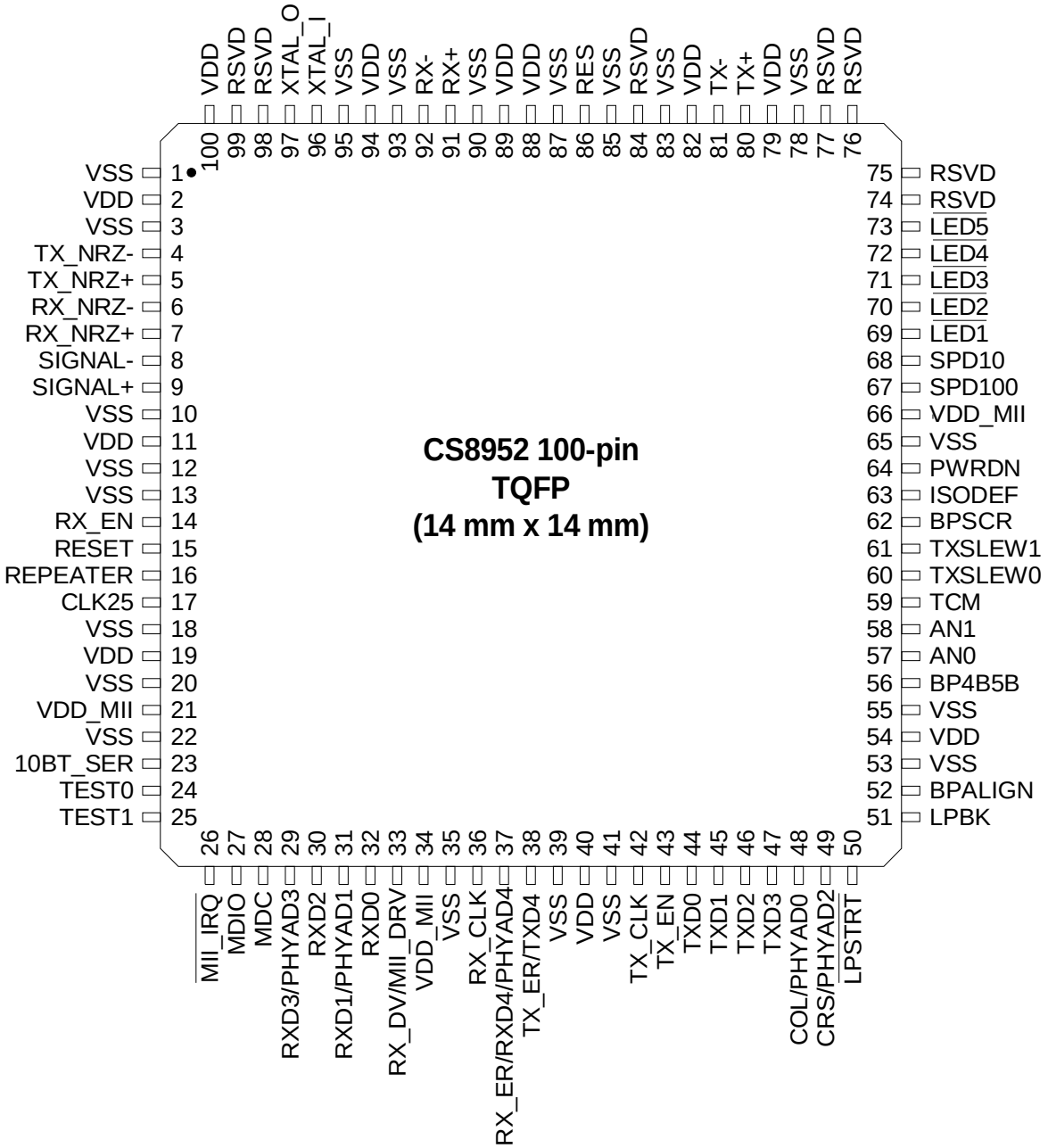
CS8952 Pin Assignment	T1 Primary Pin Assignment	T1 Secondary Pin Assignment	RJ-45 Pin Assignment	
			Adapter/NIC Configuration	Hub/Repeater Configuration
91 (RX+)	1 (RX+)	7 (RX+)	3 (RD+)	1 (RD+)
92 (RX-)	2 (RX-)	6 (RX-)	6 (RD-)	2 (RD-)
81 (TX-)	16 (TX-)	10 (TX-)	2 (TD+)	6 (TD-)
80 (TX+)	15 (TX+)	11 (TX+)	1 (TD+)	3 (TD+)

Table 8. RJ-45 Wiring

- No signal current carrying planes, i.e. no ground or power plane, should be present underneath the region between the transformer secondary (network) side and the RJ-45. However, a chassis plane may be added in this region to pick up the metal tabs of a shielded RJ-45. This chassis plane should be separated from the ground and power planes by at least 50 mils. That is, all other ground and power planes should be “cookie cuttered” so they are voided in the area of the chassis plane. Generally speaking, parts should not cross the moat except for the transformer.
- Proper termination practices must be used with all transmission lines, especially if sending and receiving high speed signals on and off the board. Series terminations must be kept close to the source and load terminations close to the load. Thus the TX_NRZ+/- termination components must be kept close to the fiber optic transceiver, and the RX_NRZ+/- and SIGNAL+/- termination components must be kept close to the CS8952.
- Locate the crystal as close to the CS8952 as possible, running short traces on the component side in order to reduce parasitic load capacitance.
- Add bulk capacitance at each connector where power may be supplied. For example, MII power may be provided at the MII connector and at a separate connector for test purposes. If so, and the two connectors are not adjacent, then the bulk capacitors should be duplicated in each locations.
- Use wide traces to connect the “Bob Smith” termination resistors at T1 and the RJ-45 to the 2 KV capacitor or capacitors in order to minimize their lead inductance.

8. PIN DESCRIPTIONS

Pin Diagram



MII Interface Pins

COL/PHYAD0 - Collision Detect/PHY Address 0. Input/Tri-State Output, Pin 48.

Asserted active-high to indicate a collision on the medium during half-duplex operation. In full-duplex operation, COL is undefined and should be ignored. When configured for 10 Mb/s operation, COL is also used to indicate a Signal Quality Error (SQE) condition.

At power-up or at reset, the logic value on this pin is latched into bit 0 of the PHY Address field of the Self Status Register (address 19h). This pin includes a weak internal pull-up (> 150 KΩ), or the value may be set by an external 4.7 KΩ pull-up or pull-down resistor.

CRS/PHYAD2 - Carrier Sense/PHY Address 2. Input/Tri-State Output, Pin 49.

The operation of CRS is controlled by the REPEATER pin as follows:

REPEATER pin	DUPLEX mode	CRS Indicates
high	don't care	receive activity only
low	full duplex	receive activity only
low	half duplex	receive or transmit activity

At power-up or at reset, the logic value of this pin is latched into bit 2 of the PHY Address Field of the Self Status Register (address 19h). This pin includes a weak internal pull-down (> 20 KΩ), or the value may be set by an external 4.7 KΩ pull-up or pull-down resistor.

MDC - Management Data Clock. Input, Pin 28.

Input clock used to transfer serial data on MDIO. The maximum clock rate is 16.67 MHz. This clock may be asynchronous to RX_CLK and TX_CLK.

MDIO - Management Data Input/Output. Bi-Directional, Pin 27.

Bi-directional signal used to transfer management data between the CS8952 and the Ethernet controller.

In order to conform with Annex 22B of the IEEE 802.3u specification, the MII_DRV pin should be pulled high during power-up or reset, and the MDIO pin should have an external 1.5 KΩ pull-up resistor. For systems not required to drive external connectors and cables as described in the IEEE802.3u specification, the external pull-up resistor may not be necessary.

$\overline{\text{MII\_IRQ}}$ - MII Interrupt. Open Drain Output, Pin 26.

Asserted low to indicate the status corresponding to one of the unmasked interrupt status bits in the Interrupt Status Register (address 11h) has changed. It will remain low until the ISR is read, clearing all status bits.

This open drain pin requires a 4.7 kΩ pull-up resistor.

RX_CLK - Receive Clock. Tri-State Output, Pin 36

Continuous clock output used as a reference clock for sampling RXD[3:0], RX_ER, and RX_DV. RX_CLK will have the following nominal frequency:

Speed	10BT_SER pin	Nominal frequency
100 Mb/s	n/a	25 MHz
10 Mb/s	low (parallel)	2.5 MHz
10 Mb/s	high (serial)	10 MHz

In order to conform with Annex 22B of the IEEE 802.3u specification, the MII_DRV pin should be pulled high during power-up or reset, and the RX_CLK pin should have an external 33 Ω series resistor. For systems not required to drive external connectors and cables as described in the IEEE802.3u specification, the external series resistor may not be necessary.

RX_DV/MII_DRV - Receive Data Valid/MII Drive Strength. Input/Tri-State Output, Pin 33.

Asserted high to indicate valid data nibbles are present on RXD[3:0].

At power-up or at reset, this pin is used as an input to determine the drive strength of the MII output drivers. When the pin is low, all MII output drivers will be standard 4 mA CMOS drivers. When high, additional drive strength will be added to the MII output drivers. This pin includes a weak internal pull-down (> 20 KΩ), or the value may be set by an external 4.7 KΩ pull-up or pull-down resistor.

In order to conform with Annex 22B of the IEEE 802.3u specification, this pin should be pulled high during power-up or reset and should have an external 33 Ω series resistor. For systems not required to drive external connectors and cables as described in the IEEE802.3u specification, it may be possible to reduce overall power consumption by pulling the pin low at power-up or reset, and the external series resistor may not be necessary.

RX_EN - Receive Enable. Input, Pin 14.

When high, signals RXD[3:0], RX_CLK, RX_DV, and RX_ER are enabled. When low, these signals are tri-stated. RX_EN allows the received data signals of multiple PHY transceivers to share the same MII bus.

This pin includes a weak internal pull-up (> 150 KΩ), or the value may be set by an external 10 KΩ pull-up or pull-down resistor.

RX_ER/PHYAD4/RXD4 - Receive Error/PHY Address 4/Receive Data 4. Input/Tri-State Output, Pin 37.

During normal MII operation, this pin is defined as RX_ER (Receive Error). When RX_DV is high, RX_ER asserted high indicates that an error has been detected in the current receive frame. When RX_DV is low and RXD[3:0] = “1110”, RX_ER high indicates a False Carrier condition.

If either BPALIGN or BP4B5B is asserted, then this pin is re-defined as RXD4 (Receive Data 4), the most-significant bit of the received five-bit code-group. If the 4B5B encoder is being bypassed, receive data is present when RX_DV is asserted. If alignment is being bypassed, data reception is continuous.

At power-up or at reset, the logic value on this pin is latched into bit 4 of the PHY Address field of the Self Status Register (address 19h). This pin includes a weak internal pull-down (> 20 KΩ), or the value may be set by an external 4.7 KΩ pull-up or pull-down resistor.

In order to conform with Annex 22B of the IEEE 802.3u specification, the MII_DRV pin should be pulled high during power-up or reset, and the RX_ER pin should have an external 33 Ω series resistor. For systems not required to drive external connectors and cables as described in the IEEE802.3u specification, the external series resistor may not be necessary.

RXD3/PHYAD3 - Receive Data 3/PHY Address 3. Tri-State Output, Pin 29.
RXD2 - Receive Data 2. Tri-State Output, Pin 30.
RXD1/PHYAD1 - Receive Data 1/PHY Address 1. Tri-State Output, Pin 31.
RXD0 - Receive Data 0. Tri-State Output, Pin 32.

Receive data output. Receive data is present when RX_DV is asserted. RXD0 is the least-significant bit. For MII modes, nibble-wide data (synchronous to RX_CLK) is transferred on pins RXD[3:0]. In 10 Mb/s serial mode, pin RXD0 is used as the serial output pin, and RXD[3:1] are ignored. When either BP4B5B or BPALIGN is selected, pin RXD4 contains the most-significant bit of the five-bit code-group.

At power-up or at reset, the value on RXD1/PHYAD1 is latched into bit 1 of the PHY Address field of the Self Status Register (address 19h). This pin includes a weak internal pull-down (> 20 KΩ), or the value may be set by an external 4.7 KΩ pull-up or pull-down resistor.

At power-up or at reset, the logic value on RXD3/PHYAD3 is latched into bit 3 of the PHY Address field of the Self Status Register (address 19h). This pin includes a weak internal pull-down (> 20 KΩ), or the value may be set by an external 4.7 KΩ pull-up or pull-down resistor.

In order to conform with Annex 22B of the IEEE 802.3u specification, the MII_DRV pin should be pulled high during power-up or reset, and the RXD[3:0] pins should have external 33 Ω series resistors. For systems not required to drive external connectors and cables as described in the IEEE802.3u specification, the external series resistors may not be necessary.

TX_CLK - Transmit Clock. Input/Tri-State Output, Pin 42.

Continuous clock signal used by the CS8952 as a reference clock to sample TXD[3:0], TX_ER, and TX_EN. TX_CLK can be referenced either internally (Output Mode) or externally (Input Mode) based upon the value of the TCM pin at power-up or at reset.

TCM pin	TX_CLK mode	CLK25 status
high	TX_CLK is input	CLK25 pin is an output
floating	TX_CLK is input	CLK25 is disabled
low	TX_CLK is output	CLK25 is disabled

When the TCM pin is high on power-up or reset, the CLK25 pin may be used as a source for the TX_CLK pin. When the TCM pin is floating on power-up or reset, TX_CLK must be supplied externally. TX_CLK should have the following nominal frequency:

Speed	10BT_SER pin	Nominal frequency
100 Mb/s	n/a	25 MHz
10 Mb/s	low (parallel)	2.5 MHz
10 Mb/s	high (serial)	10 MHz

TX_EN - Transmit Enable. Input, Pin 43.

Asserted high to indicate valid data nibbles are present on TXD[3:0]. When BPALIGN is selected, TX_EN must be pulled up to VDD_MII.

TX_ER/TXD4 - Transmit Error Encoding/Transmit Data 4. Input, Pin 38.

When high, TX_ER indicates to the CS8952 that a transmit error has occurred. If TX_ER is asserted simultaneously with TX_EN in 100 Mb/s mode, the CS8952 will ignore the data on the TXD[3:0] pins and transmit one or more 100 Mb/s HALT symbols in its place. In 10 Mb/s mode, TX_ER has no effect on the transmitted data.

If BP4B5B or BPALIGN are set, TX_ER/TXD4 is used to transmit the most-significant bit of the five-bit code group.

TXD[3:0] - Transmit Data. Input, Pins 47, 46, 45, and 44.

Transmit data input pins. For MII modes, nibble-wide data (synchronous to TX_CLK) must be presented on pins TXD[3:0] when TX_EN is asserted high. TXD0 is the least significant bit. In 10 Mb/s serial mode, pin TXD0 is used as the serial input pin, and TXD[3:1] are ignored.

When either BP4B5B or BPALIGN is selected, pin TXD4 contains the most significant bit of the five-bit code-group.

Control and Status Pins

10BT_SER - 10 Mb/s Serial Mode Select. Input, Pin 23.

When asserted high during power-up or reset and 10 Mb/s operation is selected, serial data will be transferred on pins RXD0 and TXD0. When low during power-up or reset and 10 Mb/s operation is selected, data is transferred a nibble at a time on RXD[3:0] and TXD[3:0]. This pin is ignored during 100 Mb/s operation.

10 Mb/s serial mode may also be entered under software control through bit 9 of the 10BASE-T Status Register (address 1Bh).

At power-up or at reset, the value on this pin is latched into bit 9 of the 10BASE-T Status Register (address 1Bh). This pin includes a weak internal pull-down (> 20 KΩ), or the value may be set by an external 4.7 KΩ pull-up or pull-down resistor.

AN[1:0] - Auto-Negotiate Control. Input, Pins 58 and 57.

These three-level input pins are sampled during power-up or reset. They control the forced or advertised auto-negotiation operating modes. If one of these pins is left unconnected, internal logic pulls its signal to a mid-range value, 'M'.

AN1 pin	AN0 pin	Speed	Forced/Auto	Full/Half Duplex
0	M	10 Mb/s	Forced	Half

AN1 pin	AN0 pin	Speed	Forced/Auto	Full/Half Duplex
1	M	10 Mb/s	Forced	Full
M	0	100 Mb/s	Forced	Half
M	1	100 Mb/s	Forced	Full
M	M	100/10 Mb/s	Auto-Neg	Full/Half
0	0	10 Mb/s	Auto-Neg	Half
0	1	10 Mb/s	Auto-Neg	Full
1	0	100 Mb/s	Auto-Neg	Half
1	1	100 Mb/s	Auto-Neg	Full

Auto-Negotiation may also be enabled and the advertised capabilities modified under software control through bit 8 of the Basic Mode Control Register (address 00h), and bits 5, 6, 7, 8, and 10 of the Auto-Negotiation Advertisement Register (address 04h).

These pins are pulled to 'M' through weak internal resistors (> 150 KΩ). Other values may be set by tying them directly to VDD_MII or VSS, or through external 10 KΩ pull-up or pull-down resistors.

BP4B5B - Bypass 4B5B Coders. Input, Pin 56.

When driven high during power-up or reset, the transmit 4B5B encoder and receiver 5B4B decoder are bypassed. Five-bit code groups are output and input on pins RXD[4:0] and TXD[4:0].

The 4B5B Coders may also be bypassed under software control through bit 14 of the Loopback, Bypass, and Receiver Error Mask Register (address 18h).

At power-up or at reset, the value on this pin is latched into bit 14 of the Loopback, Bypass and Receiver Error Mask Register (address 18h). This pin includes a weak internal pull-down (> 20 KΩ), or the value may be set by an external 4.7 KΩ pull-up or pull-down resistor.

BPALIGN - Bypass Symbol Alignment. Input, Pin 52.

When driven high during power-up or reset, the following blocks are bypassed: 4B5B encoder, 5B4B decoder, scrambler, descrambler, NRZI encoder, and NRZI decoder. Five-bit code groups are output and input on pins RXD[4:0] and TXD[4:0]. The receiver will output five-bit data with no attempt to identify code-group boundaries; therefore, the data in one RXD[4:0] word may contain data from two code groups.

Symbol alignment may also be bypassed under software control through bit 12 of the Loopback, Bypass, and Receiver Error Mask Register (address 18h).

At power-up or at reset, the value on this pin is latched into bit 12 of the Loopback, Bypass and Receiver Error Mask Register (address 18h). This pin includes a weak internal pull-down (> 20 KΩ), or the value may be set by an external 4.7 KΩ pull-up or pull-down resistor.

BPSCR - Bypass Scrambler. Input, Pin 62.

When driven high during power-up or reset, the scrambler and descrambler is bypassed and NRZI FX mode is selected.

The 100BASE-FX mode may also be entered under software control through bit 13 of the Loopback, Bypass, and Receiver Error Mask Register (address 18h).

At power-up or at reset, the value on this pin is latched into bit 13 of the Loopback, Bypass and Receiver Error Mask Register (address 18h). This pin includes a weak internal pull-down (> 20 KΩ), or the value may be set by an external 4.7 KΩ pull-up or pull-down resistor.

ISODEF - Isolate Default. Input, Pin 63.

When asserted high during power-up or reset, the MII will power-up electrically isolated except for the MDIO and MDC pins. When low, the part will exit reset fully electrically connected to the MII.

The MII may also be isolated under software control through bit 10 of the Basic Mode Control Register (address 00h).

At power-up or at reset, the value on this pin is latched into bit 10 of the Basic Mode Control Register (address 00h). This pin includes a weak internal pull-down (> 20 KΩ), or the value may be set by an external 4.7 KΩ pull-up or pull-down resistor.

$\overline{\text{LED1}}$ - Transmit Active LED. Open Drain Output, Pin 69.

This active-low output indicates transmit activity. It contains a pulse stretcher to insure that the transmit events are visible when the pin is used to drive an LED. The definition of this pin may be modified to indicate Disconnect Detection (bit 5 of the Self Status Register (address 19h)) by setting bit 2 of the PCS Sub-layer Configuration Register (address 17h).

This pin can be simultaneously connected to an LED and to a TTL-compatible, CMOS input pin.

$\overline{\text{LED2}}$ - Receive Activity LED. Open Drain Output, Pin 70.

This active-low output indicates receive activity. It contains a pulse stretcher to insure that the receive events are visible when the pin is used to drive an LED.

This pin can be simultaneously connected to an LED and to a TTL-compatible, CMOS input pin.

$\overline{\text{LED3}}$ - Link Good LED. Open Drain Output, Pin 71.

This active-low output indicates the CS8952 has detected a valid link.

This pin can be simultaneously connected to an LED and to a TTL-compatible, CMOS input pin.

$\overline{\text{LED4}}$ - Polarity/Full Duplex LED. Open Drain Output, Pin 72.

This active-low output indicates:
1) for 100 Mb/s operation, the CS8952 is in full-duplex operation,
2) for 10 Mb/s operation, either good polarity exists or full duplex is selected (see bit 1 in the PCS Sub-layer Configuration Register (address 17h)).

This pin can be simultaneously connected to an LED and to a TTL-compatible, CMOS input pin.

$\overline{\text{LED5}}$ - Collision/Descrambler Lock LED. Open Drain Output, Pin 73.

This active-low output is asserted when either the CS8952 detects a collision (bit 11 of the PCS Sub-Layer Configuration Register (address 17h) is clear), or the 100BASE-TX descrambler is synchronized (bit 11 of the PCS Sub-Layer Configuration Register (address 17h) is set). It contains a pulse stretcher to insure that the collision events are visible when the pin is used to drive an LED.

This pin can be simultaneously connected to an LED and to a TTL-compatible, CMOS input pin.

LPBK - Loopback Enable. Input, Pin 51.

When this pin is asserted high and the CS8952 is operating in 100 Mb/s mode, the CS8952 will perform a local loopback inside the PMD block, routing the scrambled NRZI output to the NRZI input port on the descrambler. The loopback includes all CS8952 100 Mb/s functionality except the MLT-3 coders and the analog line interface blocks.

When asserted high and the CS8952 is operating in 10 Mb/s mode, the CS8952 will perform a local ENDEC loopback.

LPSTRT - Low Power Start. Input, Pin 50.

When this active-low input is asserted during power-up or reset, the CS8952 will exit reset in a low power configuration, where the only circuitry enabled is that necessary to maintain the media impedance. The CS8952 will remain in a low power state until RESET pin is asserted or the MDC pin toggles.

This pin includes a weak internal pull-down (> 20 KΩ), or the value may be set by an external 4.7 KΩ pull-up or pull-down resistor.

PWRDN - Power Down. Input, Pin 64.

When this pin is asserted high, the CS8952 powers down all circuitry except that circuitry needed to maintain the network line impedance. This is the lowest power mode possible. The CS8952 will remain in low power mode until the PWRDN pin is deasserted.

A slightly higher power power-down mode may also be entered under software control through bit 11 of the Basic Mode Control Register (address 00h).

REPEATER - REPEATER Mode Select. Input, Pin 16.

This pin controls the operation of the CRS (Carrier Sense) pin as shown below:

REPEATER pin	DUPLEX mode	CRS Indicates
high	don't care	receive activity only
low	full duplex	receive activity only
low	half duplex	receive or transmit activity

At power-up or at reset, the value on this pin is latched into bit 12 of the PCS Sub-Layer Configuration Register (address 17h). This pin includes a weak internal pull-down (> 20 KΩ), or the value may be set by an external 4.7 KΩ pull-up or pull-down resistor.

SPD10 - 10 Mb/s Speed Indication. Output, Pin 68.

This pin is asserted high when the CS8952 is configured for 10 Mb/s operation. This pin can be used to drive a low-current LED to indicate 10 Mb/s operation.

SPD100 - 100 Mb/s Speed Indication. Output, Pin 67.

This pin is asserted high when the CS8952 is configured for 100 Mb/s operation. This pin can be used to drive a low-current LED to indicate 100 Mb/s operation.

TCM - Transmit Clock Mode Initialization. Input, Pin 59.

The logic value on this three-level pin during power-up or reset determines whether TX_CLK is used as an input or an output, and whether an external 25 MHz clock reference is provided on the CLK25 output pin.

TCM pin	TX_CLK mode	CLK25 status
high	TX_CLK is input	CLK25 pin is an output
floating	TX_CLK is input	CLK25 is disabled
low	TX_CLK is output	CLK25 is disabled

TEST[1:0] - Factory Test. Input, Pins 24 and 25.

These pins are for factory test only. They include weak internal pull-downs (> 20 KΩ), and should be tied directly to VSS for normal operation.

TXSLEW[1:0] - Transmit Slew Rate Control. Input, Pins 61 and 60.

These three-level pins allow adjustment to the rise and fall times of the 10BASE-TX transmitter output waveform. The rise and fall times are symmetric.

TXSLEW0 pin	TXSLEW1 mode	Rise/Fall time
low	low	0.5 ns
low	floating	1.0 ns
low	high	1.5 ns
floating	low	2.0 ns
floating	floating	2.5 ns
floating	high	3.0 ns
high	low	3.5 ns
high	floating	4.0 ns
high	high	4.5 ns

Media Interface Pins

RX+, RX- - 10/100 Receive. Differential Input Pair, Pins 91 and 92.

Differential input pair receives 10 or 100 Mb/s data from the receive port of the transformer primary.

TX+, TX- - 10/100 Transmit. Differential Output Pair, Pins 80 and 81.

Differential output pair drives 10 or 100 Mb/s data to the transmit port of the transformer primary.

RX_NRZ+, RX_NRZ- - FX Receive. Differential Input Pair, Pins 6 and 7.

PECL output pair receives 100 Mb/s NRZI-encoded data from an external optical module.

SIGNAL+, SIGNAL- - Signal Detect. Differential Input Pair, Pins 9 and 8.

PECL input pair receives signal detection indication from an external optical module.

TX_NRZ+, TX_NRZ- - FX Transmit. Differential Output Pair, Pins 5 and 4.

PECL output pair drives 100 Mb/s NRZI-encoded data to an external optical module.

General Pins

CLK25 - 25 MHz Clock. Output, Pin 17.

A 25 MHz Clock is output on this pin when the CS8952 is configured to use an external reference transmit clock in TX_CLK IN MASTER mode. See the pin description for the Transmit Clock Mode Initialization pin (TCM) for more information on TX_CLK operating modes.

CLK25 may also be enabled regardless of the TCM pin state by clearing bit 7 of the PCS Sub-layer Configuration Register (address 17h).

RES - Reference Resistor. Input, Pin 86.

This input should be connected to ground with a 4.99 kΩ +/-1% series resistor. The resistor is needed for the biasing of internal analog circuits.

RESET - Reset. Input, Pin 15.

This active high input initializes the CS8952, and causes the CS8952 to latch the input signal on the following pins: COL/PHYAD0, CRS/PHYAD2, RX_ER/PHYAD4/RXD4, 10BT_SER, BP4B5B, BPALIGN, BPSCR, ISODEF, REPEATER, RXD[1]/PHYAD1, and RXD[3]/PHYAD3.

XTAL_I - Crystal Input, Pin 96.

XTAL_O - Crystal Output, Pin 97.

A 25 MHz crystal should be connected across pins XTAL_I and XTAL_O. If a crystal is not used, a 25 MHz CMOS level clock may be connected to XTAL_I and XTAL_O left open.

NOTE: The XTAL_I pin capacitive load may be as high as 35pF. Any external clock source connected to this pin must be capable of driving larger capacitive loads.

RSVD - Reserved. Pins 74, 75, 76, 77, 84, 98, and 99.

These seven pins are reserved and should be tied to VSS.

VDD_MII - MII Power. Pins 21, 34, and 66.

These pins provide power to the CS8952 MII interface. Typically VDD_MII will be either +5V or +3.3V.

VDD - Core Power. Pins 2, 11, 19, 40, 54, 79, 82, 88, 89, 94, and 100.

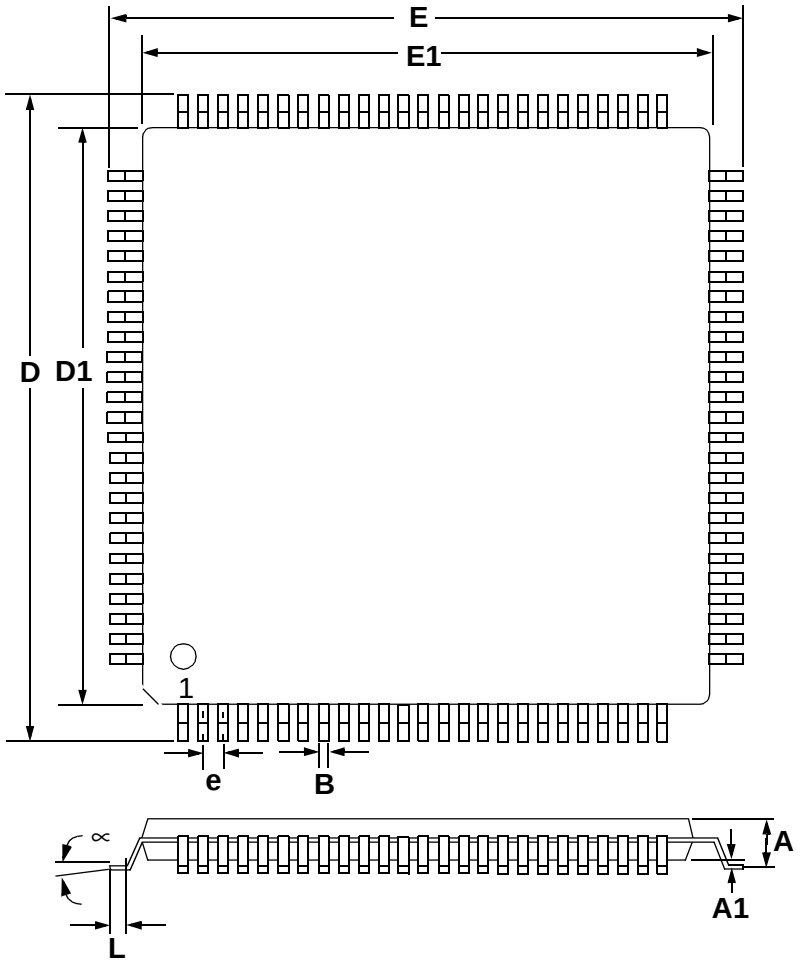
These pins provide power to the CS8952 core. Typically, VDD should be +5V.

VSS - Ground. Pins 1, 3, 10, 12, 13, 18, 20, 22, 35, 39, 41, 53, 55, 65, 78, 83, 85, 87, 90, 93, and 95.

These pins provide a ground reference for the CS8952.

9. PACKAGE DIMENSIONS

100L TQFP PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	---	0.063	---	1.60
A1	0.002	0.006	0.05	0.15
B	0.007	0.011	0.17	0.27
D	0.618	0.642	15.70	16.30
D1	0.547	0.555	13.90	14.10
E	0.618	0.642	15.70	16.30
E1	0.547	0.555	13.90	14.10
e*	0.016	0.024	0.40	0.60
L	0.018	0.030	0.45	0.75
∝	0.000°	7.000°	0.00°	7.00°

* Nominal pin pitch is 0.50 mm

Controlling dimension is mm.
JEDEC Designation: MS026

• Notes •


CIRRUS LOGIC®