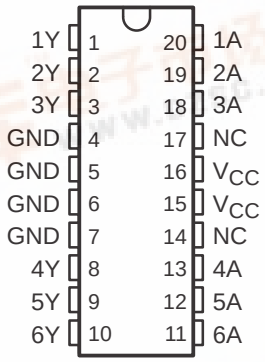
# CDC204
# HEX INVERTER/CLOCK DRIVER

SCAS098E – OCTOBER 1989– REVISED OCTOBER 1998

- CDC204 Replaces 74AC11204
- Low-Skew Propagation Delay Specifications for Clock-Driver Applications
- CMOS-Compatible Inputs and Outputs
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin $V_{CC}$ and GND Pin Configurations Minimize High-Speed Switching Noise
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Package (DW))

**DW PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

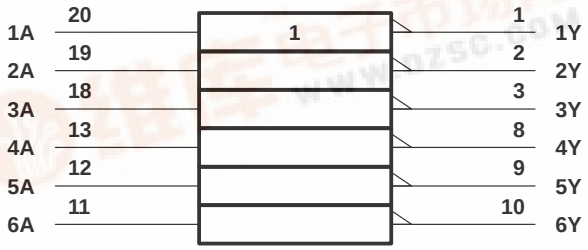
The CDC204 contains six independent inverters. The device performs the Boolean function $Y = \overline{A}$. It is designed specifically for applications requiring low skew between switching outputs.

The CDC204 is characterized for operation from $T_A$ = 25°C to 70°C.

**FUNCTION TABLE**

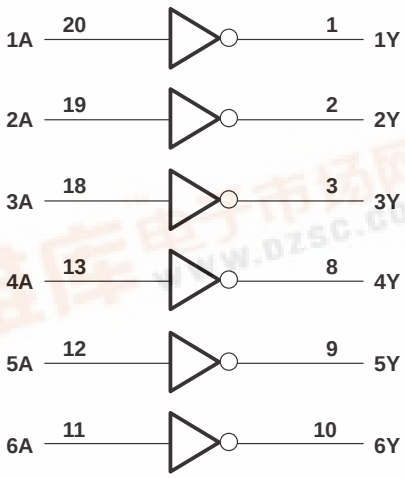
| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | H |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CC}$) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±50 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±50 mA
Continuous current through $V_{CC}$ or GND . . . . . ±150 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 2) . . . . . 1.6 W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

### recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 4.75 V | 3.3 | | | V |
| | | $V_{CC}$ = 5.25 V | 3.7 | | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 4.75 V | | | 1.4 | V |
| | | $V_{CC}$ = 5.25 V | | | 1.6 | |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 4.75 V | | | –24 | mA |
| | | $V_{CC}$ = 5.25 V | | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 4.75 V | | | 24 | mA |
| | | $V_{CC}$ = 5.25 V | | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 0 | | 10 | ns/V |
| $f_{clock}$ | Input clock frequency | | | | 80 | MHz |
| $T_A$ | Operating free-air temperature | | 25 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$† | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level voltage output | $I_{OH}$ = – 50 μA | $V_{CC}$ = 4.75 V | 25°C | 4.65 | | | V |
| | | | | Full range | 4.65 | | | |
| | | | $V_{CC}$ = 5.25 V | 25°C | 5.15 | | | |
| | | | | Full range | 5.15 | | | |
| | | $I_{OH}$ = – 24 mA | $V_{CC}$ = 4.75 V | 25°C | 4.19 | | | |
| | | | | Full range | 4.05 | | | |
| | | | $V_{CC}$ = 5.25 V | 25°C | 4.68 | | | |
| | | | | Full range | 4.55 | | | |
| | | $I_{OH}$ = –75 mA‡, | $V_{CC}$ = 5.25 V | Full range | 3.6 | | | |
| $V_{OL}$ | Low-level voltage output | $I_{OL}$ = 50 μA | $V_{CC}$ = 4.75 V | 25°C | | | 0.1 | V |
| | | | | Full range | | | 0.1 | |
| | | | $V_{CC}$ = 5.25 V | 25°C | | | 0.1 | |
| | | | | Full range | | | 0.1 | |
| | | $I_{OL}$ = 24 mA | $V_{CC}$ = 4.75 V | 25°C | | | 0.36 | |
| | | | | Full range | | | 0.44 | |
| | | | $V_{CC}$ = 5.25 V | 25°C | | | 0.36 | |
| | | | | Full range | | | 0.44 | |
| | | $I_{OL}$ = 75 mA‡, | $V_{CC}$ = 5.25 V | Full range | | | 1.65 | |
| $I_I$ | Input current | $V_I$ = $V_{CC}$ or GND | $V_{CC}$ = 5.25 V | 25°C | | | ±0.1 | μA |
| | | | | Full range | | | ±1 | |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | $V_{CC}$ = 5.25 V, | 25°C | | | 4 | μA |
| | | | | Full range | | | 40 | |
| $C_i$ | Input capacitance | $V_I$ = $V_{CC}$ or GND, | $V_{CC}$ = 5 V | 25°C | | 4 | | pF |

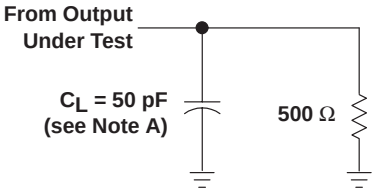
† Full range is $T_A$ = 25°C to 70°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.25 V (see Note 3 and Figures 1 and 2)

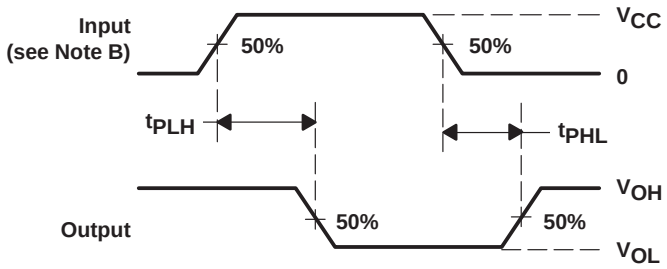
| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high level (see Figure 1) | A | Y | 3.7 | 5.7 | ns |
| $t_{PHL}$ | Proagation delay time, high-to-low level (see Figure 1) | | | 2.9 | 5.7 | |
| $t_{sk(o)}$ | Output skew time (see Figure 2) | A | Y | | 1 | ns |

NOTE 3: All specifications are valid only for all outputs switching simultaneously and in phase.

## PARAMETER MEASUREMENT INFORMATION




**LOAD CIRCUIT**

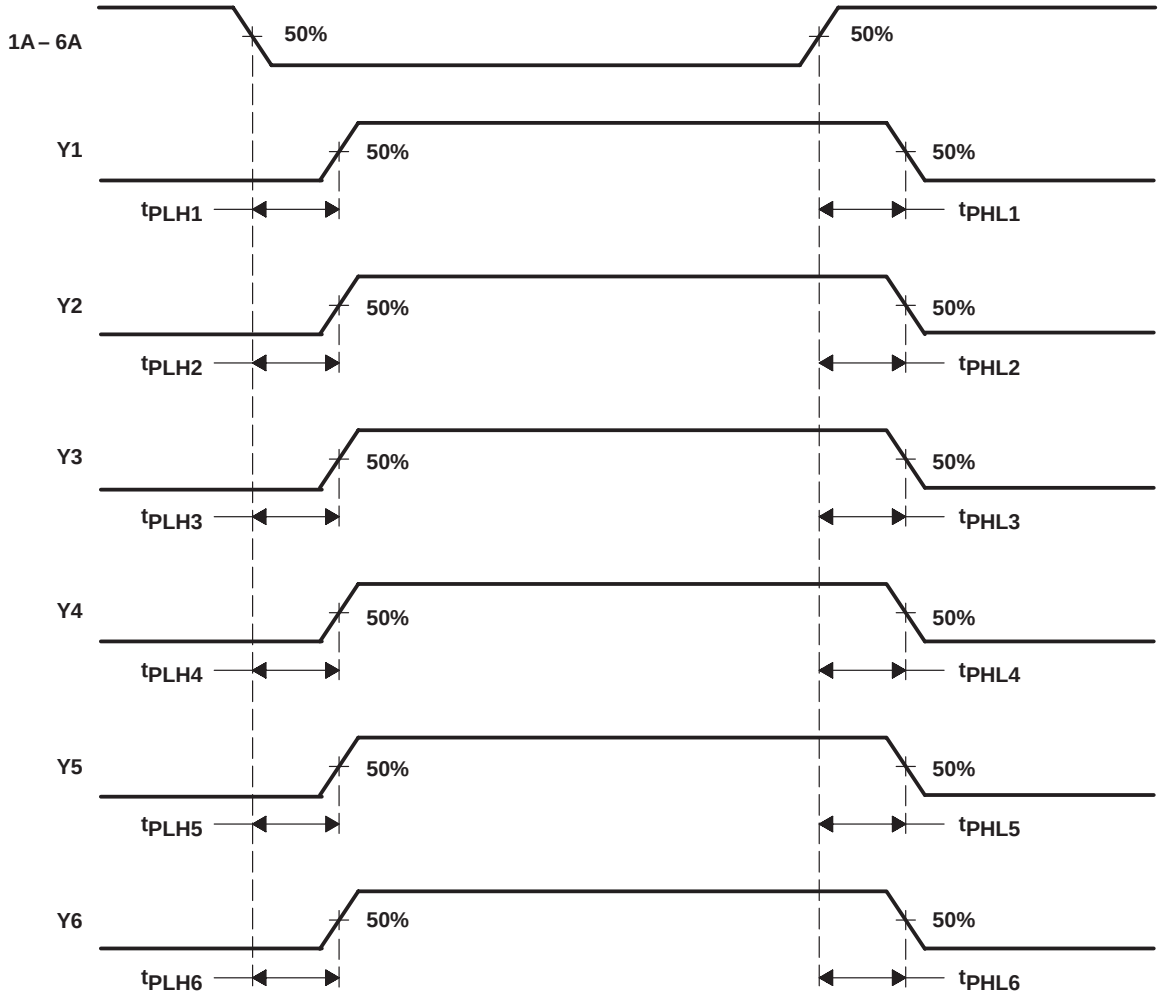



**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES**

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION



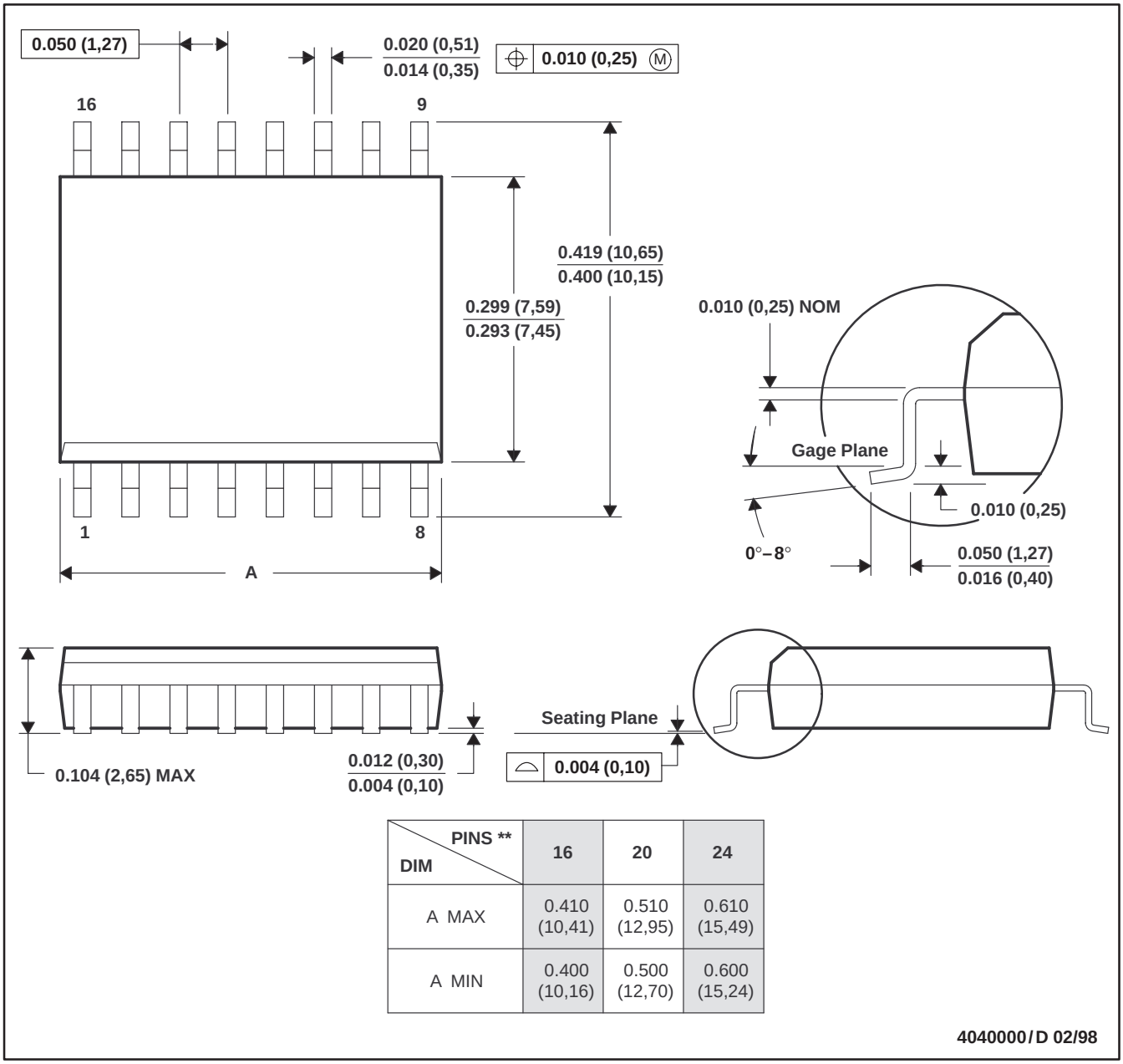

NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of $t_{PHLn}$ (n = 1, 2, . . . , 6)
- The difference between the fastest and slowest of $t_{PLHn}$ (n = 1, 2, . . . , 6)

**Figure 2. Waveforms for Calculation of $t_{sk(o)}$**

## MECHANICAL INFORMATION

**DW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**16 PIN SHOWN**




| DIM \ PINS ** | 16 | 20 | 24 |
|---|---|---|---|
| A MAX | 0.410 (10,41) | 0.510 (12,95) | 0.610 (15,49) |
| A MIN | 0.400 (10,16) | 0.500 (12,70) | 0.600 (15,24) |

**4040000/D 02/98**

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.