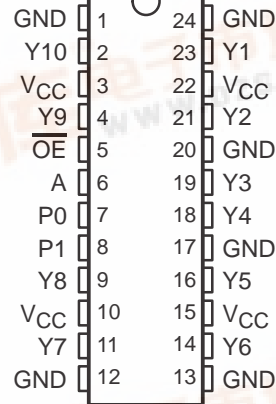


1-LINE TO 10-LINE CLOCK DRIVER WITH 3-STATE OUTPUTS

SCAS441C – FEBRUARY 1994 – REVISED NOVEMBER 1995

- Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications
- Operates at 3.3-V V_{CC}
- LVTTTL-Compatible Inputs and Outputs
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Distributes One Clock Input to Ten Outputs
- Distributed V_{CC} and Ground Pins Reduce Switching Noise
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $32\text{-mA } I_{OL}$)
- State-of-the-Art EPIC-II[™] BiCMOS Design Significantly Reduces Power Dissipation
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages

DB OR DW PACKAGE (TOP VIEW)



description

The CDC351 is a high-performance clock-driver circuit that distributes one input (A) to ten outputs (Y) with minimum skew for clock distribution. The output-enable (\overline{OE}) input disables the outputs to a high-impedance state. The CDC351 operates at nominal 3.3-V V_{CC} .

The propagation delays are adjusted at the factory using the P0 and P1 pins. The factory adjustments ensure that the part-to-part skew is minimized and is kept within a specified window. Pins P0 and P1 are not intended for customer use and should be connected to GND.

The CDC351 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS		OUTPUTS
A	\overline{OE}	Y_n
L	H	Z
H	H	Z
L	L	L
H	L	H

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

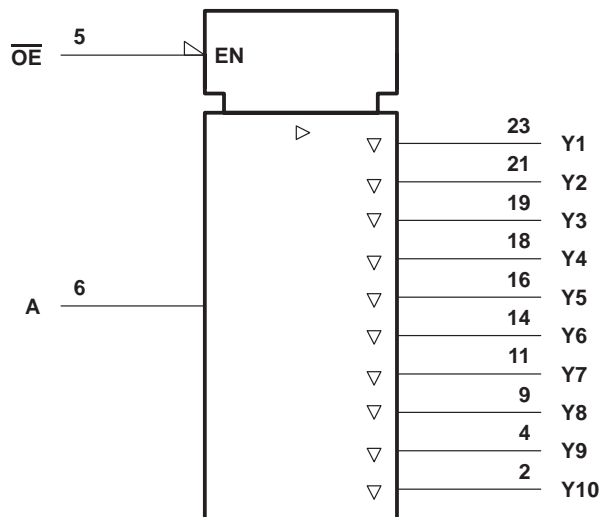
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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

CDC351 1-LINE TO 10-LINE CLOCK DRIVER WITH 3-STATE OUTPUTS

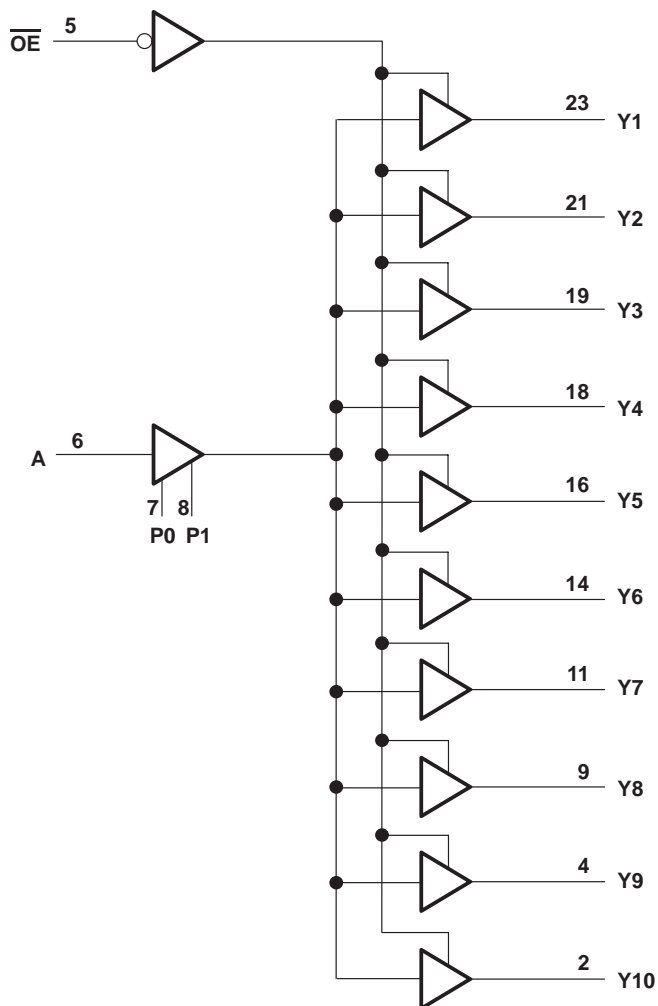
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 3.6 V
Current into any output in the low state, I_O	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_I < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DB package	0.65 W
DW package	1.7 W
Storage temperature range, T_{stg}	-65 to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
V_{CC} Supply voltage	3	3.6	V
V_{IH} High-level input voltage	2		V
V_{IL} Low-level input voltage		0.8	V
V_I Input voltage	0	5.5	V
I_{OH} High-level output current		-32	mA
I_{OL} Low-level output current		32	mA
f_{clock} Input clock frequency		100	MHz
T_A Operating free-air temperature	0	70	$^\circ\text{C}$

NOTE 3: Unused pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	$V_{CC} = 3\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
V_{OH}	$V_{CC} = 3\text{ V}$,	$I_{OH} = -32\text{ mA}$	2			V
V_{OL}	$V_{CC} = 3\text{ V}$,	$I_{OL} = 32\text{ mA}$			0.5	V
I_I	$V_{CC} = 3.6\text{ V}$,	$V_I = V_{CC}$ or GND			± 1	μA
I_O^\ddagger	$V_{CC} = 3.6\text{ V}$,	$V_O = 2.5\text{ V}$	-15		-150	mA
I_{OZ}	$V_{CC} = 3.6\text{ V}$,	$V_O = 3\text{ V}$ or 0			± 10	μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND	$I_O = 0$,	Outputs high		0.3	mA
			Outputs low		25	
			Outputs disabled		0.3	
C_i	$V_I = V_{CC}$ or GND,	$V_{CC} = 3.3\text{ V}$,	$f = 10\text{ MHz}$		4	pF
C_o	$V_O = V_{CC}$ or GND,	$V_{CC} = 3.3\text{ V}$,	$f = 10\text{ MHz}$		6	pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

CDC351
1-LINE TO 10-LINE CLOCK DRIVER
WITH 3-STATE OUTPUTS

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switching characteristics, $C_L = 50$ pF (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3$ V, $T_A = 25^\circ$ C			$V_{CC} = 3$ V to 3.6 V, $T_A = 0^\circ$ C to 70° C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	3.2	3.7	4.2			ns
t_{PHL}			3	3.5	4			
t_{PZH}	\overline{OE}	Y	1.8	3.8	5.5	1.3	5.9	ns
t_{PZL}			1.8	3.8	5.5	1.3	5.9	
t_{PHZ}	\overline{OE}	Y	1.8	3.9	5.9	1.7	6.3	ns
t_{PLZ}			1.8	4.2	5.9	1.7	6.4	
$t_{sk(o)}$	A	Y		0.3	0.5		0.5	ns
$t_{sk(p)}$	A	Y		0.2	0.8		0.8	ns
$t_{sk(pr)}$	A	Y			1		1	ns
t_r	A	Y					1.5	ns
t_f	A	Y					1.5	ns

switching characteristics temperature and V_{CC} coefficients over recommended operating free-air temperature and V_{CC} range (see Note 4)

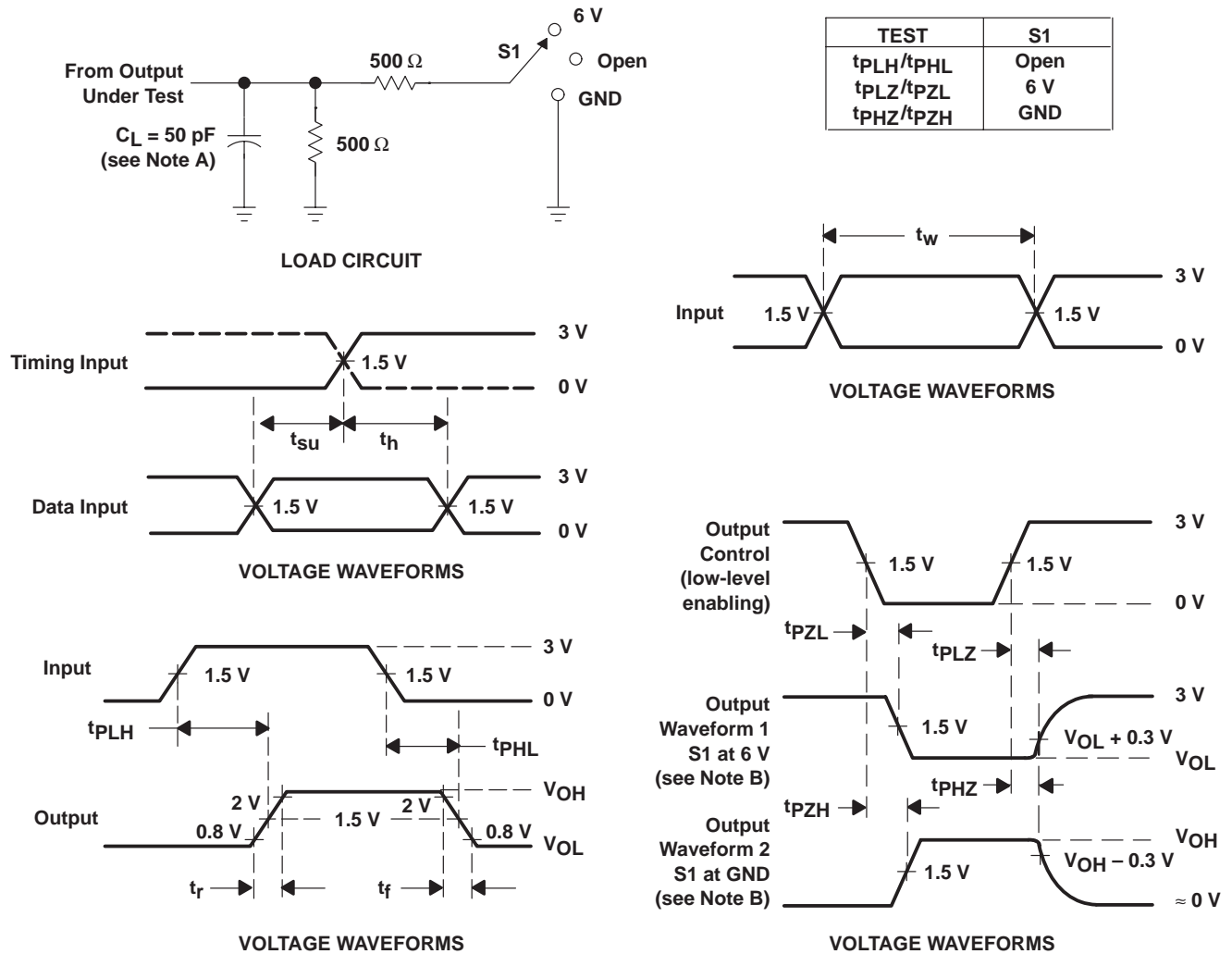
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$\propto t_{PLH}(T)$ Average temperature coefficient of low to high propagation delay	A	Y		65†	ps/ 10° C
$\propto t_{PHL}(T)$ Average temperature coefficient of high to low propagation delay	A	Y		45†	ps/ 10° C
$\propto t_{PLH}(V_{CC})$ Average V_{CC} coefficient of low to high propagation delay	A	Y		-140‡	ps/ 100 mV
$\propto t_{PHL}(V_{CC})$ Average V_{CC} coefficient of high to low propagation delay	A	Y		-120‡	ps/ 100 mV

† $\propto t_{PLH}(T)$ and $\propto t_{PHL}(T)$ are virtually independent of V_{CC} .

‡ $\propto t_{PLH}(V_{CC})$ and $\propto t_{PHL}(V_{CC})$ are virtually independent of temperature.

NOTE 4: These data were extracted from characterization material and are not tested at the factory.

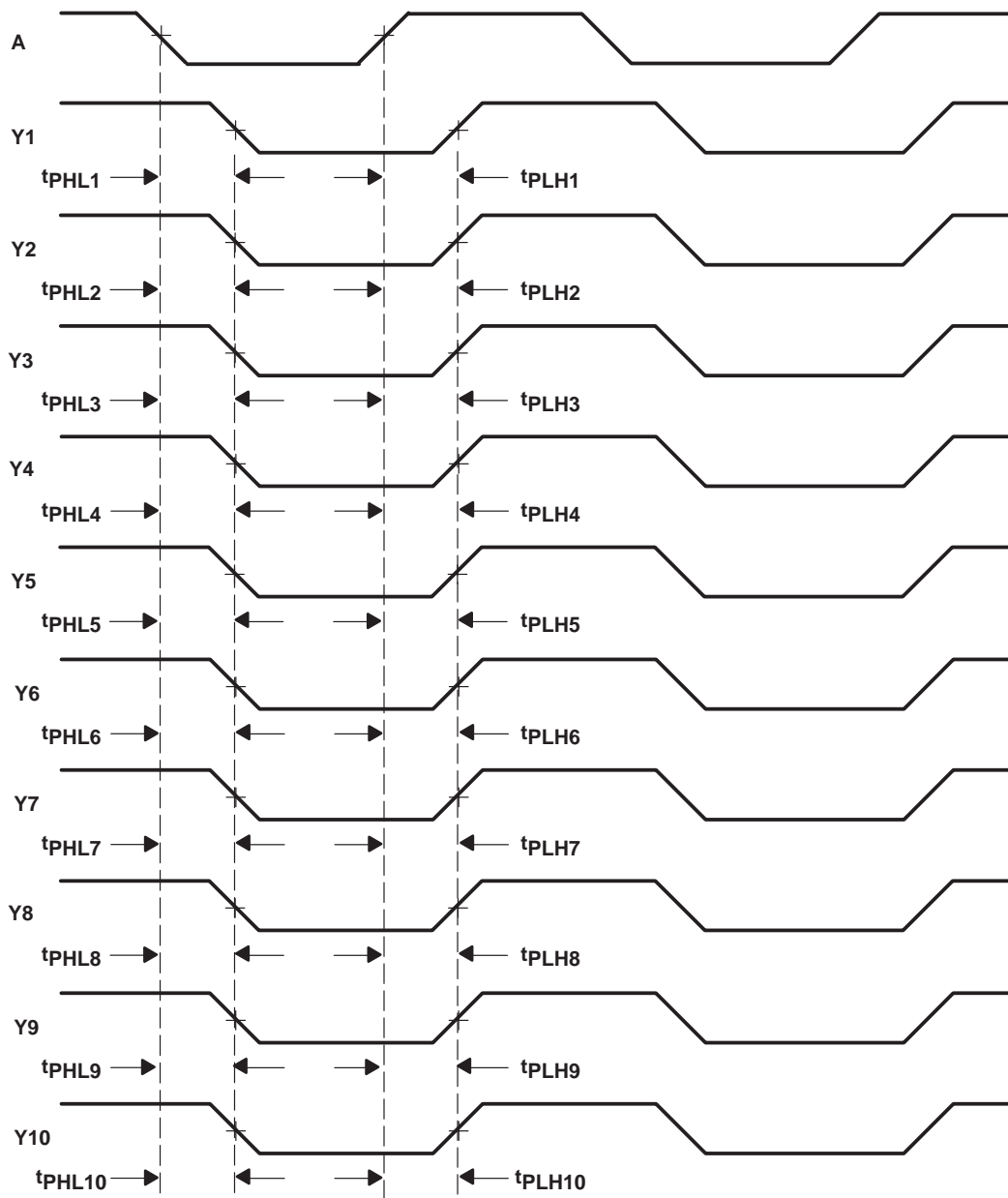
PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} ($n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10$)
 - The difference between the fastest and slowest of t_{PHLn} ($n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10$)
- B. Pulse skew, $t_{sk(p)}$, is calculated as the greater of $|t_{PLHn} - t_{PHLn}|$ ($n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10$).
- C. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} ($n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10$) across multiple devices under identical operating conditions
 - The difference between the fastest and slowest of t_{PHLn} ($n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10$) across multiple devices under identical operating conditions

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(p)}$, $t_{sk(pr)}$

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