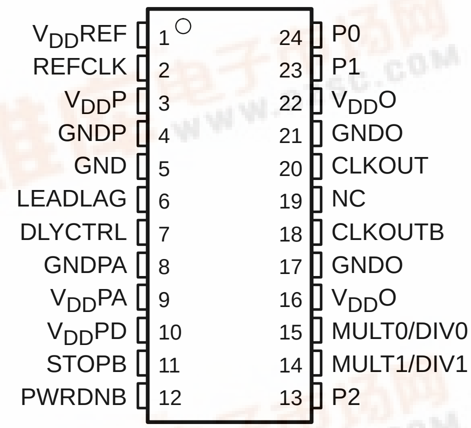
CDC5801
LOW JITTER CLOCK MULTIPLIER AND DIVIDER WITH PROGRAMMABLE DELAY AND PHASE ALIGNMENT

SCAS682A – OCTOBER 2002

- Low Jitter Clock Multiplier by x4, x6, x8. Input Frequency Range (19 MHz to 125 MHz). Supports Output Frequency From 150 MHz to 500 MHz
- Low Jitter Clock Divider by /2, /3, /4. Input Frequency Range (50 MHz to 125 MHz). Supports Ranges of Output Frequency From 12.5 MHz to 62.5 MHz
- 2.6 mUI Programmable Bidirectional Delay Steps
- Typical 8.0-ps Phase Jitter (12 kHz to 20 MHz) @ 500 MHz
- Typical 2.1-ps RMS Period Jitter (Entire Frequency Band) @ 500 MHz
- One Single-Ended Input and One Differential Output Pair
- Output Can Drive LVPECL, LVDS, and LVTTL
- Three Power Operating Modes to Minimize Power
- Low Power Consumption (Typical 200 mW at 500 MHz)
- Packaged in a Shrink Small-Outline Package (DBQ)
- No External Components Required for PLL
- Spread Spectrum Clock Tracking Ability to Reduce EMI
- Applications: Video Graphics, Gaming Products, Datacom, Telecom
- Accepts LVCMOS, LVTTL Inputs for REFCLK Terminal
- Accepts Other Single-Ended Signal Levels at REFCLK Terminal by Programming Proper V_{DD}REF Voltage Level (For Example, HSTL 1.5 if V_{DD}REF = 1.6 V)
- Supports Industrial Temperature Range of –40°C to 85°C

DBQ PACKAGE
(TOP VIEW)



NC – No internal connection

description

The CDC5801 device provides clock multiplication and division from a single-ended reference clock (REFCLK) to a differential output pair (CLKOUT/CLKOUTB). The multiply and divide terminals (MULT/DIV0:1) provide selection for frequency multiplication and division ratios, generating CLKOUT/CLOUTKB frequencies ranging from 12.5 MHz to 500 MHz with a clock input reference (REFCLK) ranging from 19 MHz to 125 MHz. Please see Table 1 and Table 2 for detail frequency support.

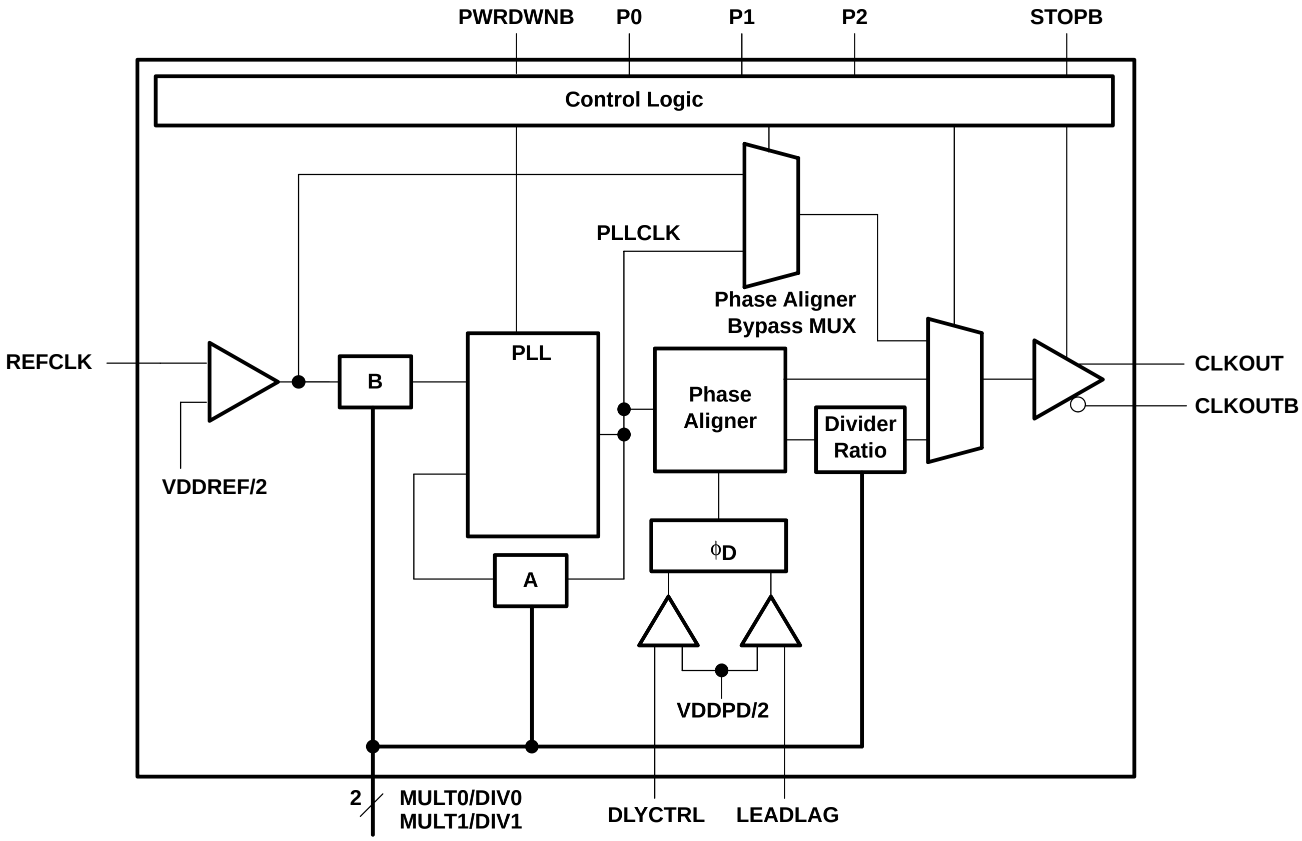
The implemented phase aligner provides the possibility to phase align (zero delay) between CLKOUT/CLKOUTB and REFCLK or any other CLK in the system by feeding the clocks that need to be aligned to the DLYCTRL and the LEADLAG terminals.

The phase aligner also allows the user to delay or advance the CLKOUT/CLKOUTB with steps of 2.6 mUI (unit interval). For every rising edge on the DLYCTRL terminal the output clocks are delayed by 2.6-mUI step size as long as there is low on the LEADLAG terminal. Similarly for every rising edge on the DLYCTRL terminal the output clocks are advanced by 2.6-mUI step size as long as there is high on the LEADLAG terminal. As the phase between REFCLK and CLKOUT/CLKOUTB is random after power up, the application may implement a self calibration routine at power up to produce a certain phase start position, before programming a fixed delay with the clock on the DLYCTRL terminal.

Depending on the selection of the mode terminals (P0:2), the device behaves as a multiplier (by 4, 6, or 8) with the phase aligner bypassed or as a multiplier or divider with programmable delay and phase aligner functionality. Through the select terminals (P0:2) user can also bypass the phase aligner and the PLL (test mode) and output the REFCLK directly on the CLKOUT/CLKOUTB terminals. Through P0:2 terminals the outputs could be in a high impedance state. This device has another unique capability to be able to function with a wide band of voltages on the REFCLK terminal by varying the voltage on the V_{DD}REF terminal.

The CDC5801 device is characterized for operation over free-air temperatures of –40°C to 85°C.

functional block diagram



FUNCTION TABLE†

MODE	P0	P1	P2	CLKOUT/CLKOUTB
Multiplication with programmable delay and phase alignment active‡	0	0	0	REFCLK multiplied by ratio per Table 1 selected by MULT/DIV terminals. Outputs are delayed or advanced based on DLYCTRL and LEADLAG terminal configuration.
Division with programmable delay and phase alignment active ‡	0	0	1	REFCLK divided by ratio per Table 2 selected by MULT/DIV terminals. Outputs are delayed or advanced based on DLYCTRL and LEADLAG terminal configuration.
Multiplication only mode (phase aligner bypassed) §	1	0	0	In this mode one can only multiply as per Table 1. Programmable delay capability and divider capability is deactivated. PLL is running.
Test mode	1	1	0	PLL and phase aligner both bypassed. REFCLK is directly channeled to output.
Hi-Z mode	0	1	X	Hi-Z

† X = don't care, Hi-Z = high impedance
‡ Please see Table 4 and Table 5 for explanation for the programmability and phase alignment functions.
§ In this mode the DLYCTRL and LEADLAG terminals must be strapped high or low. Lowest possible jitter is achieved in this mode, but a delay of 200 ps to 2 ns expected typically from REFCLK to CLKOUT depending on the output frequency.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLKOUT	20	O	Output clock
CLKOUTB	18	O	Output clock (complement)
DLYCTRL	7	I	Every rising edge on this terminal delays/advances the CLKOUT/CLKOUTB signal by 1/384th of the CLKOUT/CLKOUTB period. (e.g., for a 90 degree delay or advancement one needs to provide 96 rising edges). See Table 4.
GND	5		GND for V_{DD}REF and V_{DD}PD
GNDO	17, 21		GND for clock output terminals (CLKOUT, CLKOUTB)
GNDP	4		GND for PLL
GNDPA	8		GND for phase aligner
LEADLAG	6	I	Decides if the output clock is delayed or advanced with respect to REFCLK. See Table 4.
MULT0/DIV0	15	I	PLL multiplier and divider select
MULT1/DIV1	14	I	PLL multiplier and divider select
NC	19		Not used
PWRDNB	12	I	Active low power down state, CLKOUT/CLKOUTB goes low
P0	24	I	Mode control, see Function Table
P1	23	I	Mode control, see Function Table
P2	13	I	Mode control, see Function Table
REFCLK	2	I	Reference input clock
STOPB	11	I	Active low output disabler, PLL and PA still running, CLKOUT and CLKOUTB goes to a dc value as per Table 3
V_{DD}PA	9	I	Supply voltage for phase aligner
V_{DD}PD	10	I	Reference voltage for the DLYCTRL, LEADLAG terminals and STOPB function
V_{DD}REF	1	I	Reference voltage for REFCLK
V_{DD}O	16, 22	I	Supply voltage for the output terminals (CLKOUT, CLKOUTB)
V_{DD}P	3	I	Supply voltage for PLL

PLL divider/multiplier selection

Table 1 and Table 2 list the supported REFCLK and BUSCLK (CLKOUT/CLKOUTB) frequencies.

Table 1. Multiplication Ratios (P0:2 = 000 or 100)

MULT0	MULT1	REFCLK (MHZ)	MULTIPLICATION RATIO	BUSCLK (MHZ)
0	0	38–125	4	152–500
0	1	25–83.3	6	150–500
1	1	19–62.5	8	152–500

Table 2. Divider Ratio (P0:2 = 001)

MULT0	MULT1	REFCLK (MHZ)	DIVISION RATIO	BUSCLK (MHZ)
0	0	100–125	2	50–62.5
1	0	75–93	3	25–31
1	1	50–62	4	12.5–15.5

Table 3. Clock Output Driver States

STATE	PWRDNB	STOPB	CLKOUT	CLKOUTB
Powerdown	0	X	GND	GND
CLK stop	1	0	$V_{O, STOP}$	$V_{O, STOP}$
Normal	1	1	As per Function Table	As per Function Table

Table 4. Programmable Delay and Phase Alignment

DLYCTRL	LEADLAG	CLKOUT AND CLKOUTB
Each rising edge†	1	Will be advanced by one step size (see Table 5)
Each rising edge†	0	Will be delayed by one step size (see Table 5)

† For every 32^{nd} edge, there are one or two edges the phase aligner does not update. Therefore, CLKOUT phase is not updated on every 32^{nd} edge.

Table 5. Clock Output Driver States

FUNCTIONALITY	STEP SIZE
Multiply by 4, 6, 8	CLKOUT period/384 (for example, 6.5 ps @ 400 MHz)
Divide by 2	CLKOUT period/3072 (for example, 6.5 ps @ 50 MHz)
Divide by 3	CLKOUT period/6144 (for example, 6.5 ps @ 25 MHz)
Divide by 4	CLKOUT period/12288 (for example, 6.5 ps @ 12.5 MHz)

NOTE: The frequency of the DLYCTRL terminal must always be equal or less than the frequency of the LEADLAG terminal.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) . . . . –0.5 V to 4 V
Output voltage range, V_O, at any output terminal . . . . –0.5 V to V_{DD} + 0.5 V
Input voltage range,V_I, at any input terminal . . . . –0.5 V to V_{DD} + 0.5 V
Continuous total power dissipation . . . . see Dissipation Rating Table
Operating free-air temperature range, T_A . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$‡	$T_A = 85°C$ POWER RATING
DBQ	1400 mW	11 mW/°C	740 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (V_{DD}P, V_{DD}PA, V_{DD}O)	3.0	3.3	3.6	V
High-level input voltage, V_{IH} (CMOS)	0.7 × V_{DD}			V
Low-level input voltage, V_{IL} (CMOS)			0.3 × V_{DD}	V
REFCLK low-level input voltage, V_{IL}			0.3 × V_{DD}REF	V
REFCLK high-level input voltage, V_{IH}	0.7 × V_{DD}REF			V
Input signal low voltage, V_{IL} (STOPB, DLYCTRL, LEADLAG)			0.3 × V_{DD}PD	V
Input signal high voltage, V_{IH} (STOPB, DLYCTRL, LEADLAG)	0.7 × V_{DD}PD			V
Input reference voltage for (REFCLK) (V_{DD}REF)	1.235		V_{DD}	V
Input reference voltage for (DLYCTRL and LEADLAG) (V_{DD}PD)	1.235		V_{DD}	V
High-level output current, I_{OH}			–16	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	–40		85	°C

timing requirements

	MIN	MAX	UNIT
Input frequency of modulation, f_{mod} (if driven by SSC CLKIN)		33	kHz
Modulation index (nonlinear maximum 0.5%)		0.6%	
Input slew rate, SR	1	4	V/ns
Input duty cycle on REFCLK	40%	60%	
Input frequency on REFCLK	19	125	MHz
Allowable frequency on DLYCTRL		200	MHz
Allowable frequency on LEADLAG		400	MHz
Allowable duty cycle on DLYCTRL and LEADLAG	25%	75%	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{O(STOP)}$	Output voltage during CLK stop mode		See Figure 1		1.1		2	V
V_{OX}	Output crossing-point voltage		See Figure 1 and Figure 4		$0.5V_{DDO}$–0.2		$0.5V_{DDO}$+0.2	V
V_O	Output voltage swing (V_{OH} – V_{OL})		See Figure 1		1.7		2.9	V
V_{IK}	Input clamp voltage		V_{DD} = 3.0 V,	I_I = –18 mA			–1.2	V
V_{OH}	High-level output voltage		See Figure 1, V_{DD} = 3 to 3.6 V		2.0	2.6		V
			V_{DD} = 3.0 V,	I_{OH} = –16 mA	2.2			
V_{OL}	Low-level output voltage		See Figure 1, V_{DD} = 3 to 3.6 V			0.3	0.6	V
			V_{DD} = 3.0 V,	I_{OH} = –16 mA			0.5	
I_{OH}	High-level output current		V_{DD} = 3.135 V,	V_O = 1 V	–32	–52		mA
			V_{DD} = 3.3 V,	V_O = 1.65 V		–51		
			V_{DD} = 3.465 V,	V_O = 3.135 V		–14.5	–21	
I_{OL}	Low-level output current		V_{DD} = 3.135 V,	V_O = 1.95 V	43	61.5		mA
			V_{DD} = 3.3 V,	V_O = 1.65 V		65		
			V_{DD} = 3.465 V,	V_O = 0.4 V		25.5	36	
I_{OZ}	High-impedance-state output current		P0 = 0, P1 = 1				±10	µA
$I_{OZ(STOP)}$	High-impedance-state output current during CLK stop		Stop = 0, V_O = GND or V_{DD}				±100	µA
$I_{OZ(PD)}$	High-impedance-state output current in power-down state		PWRDNB = 0, V_O = GND or V_{DD}		–10		100	µA
I_{IH}	High-level input current	REFCLK, STOPB	V_{DD} = 3.6 V,	V_I = V_{DD}			10	µA
		PWRDNB, P0:2, MULT/DIV0:1	V_{DD} = 3.6 V,	V_I = V_{DD}			10	
I_{IL}	Low-level input current	REFCLK, STOPB	V_{DD} = 3.6 V,	V_I = 0			–10	µA
		PWRDNB, P0:2, MULT/DIV0:1	V_{DD} = 3.6 V,	V_I = 0			–10	
Z_O	Output impedance (single ended)	High state	R_I at I_O –14.5 mA to –16.5 mA		15	35	50	Ω
		Low state	R_I at I_O 14.5 mA to 16.5 mA		11	17	35	
	Reference current	V_{DD}REF, V_{DD}PD	V_{DD} = 3.6 V	PWRDNB = 0			50	µA
				PWRDNB = 1			0.5	mA
C_I	Input capacitance		V_I = V_{DD} or GND			2		pF
C_O	Output capacitance		V_O = V_{DD} or GND			3		pF
$I_{DD(PD)}$	Supply current in power-down state		REFCLK = 0 MHz to 100 MHz, PWDNB = 0, STOPB = 1				100	µA
$I_{DD(CLKSTOP)}$	Supply current in CLK stop state		BUSCLK configured for 500 MHz				40	mA
$I_{DD(NORMAL)}$	Supply current in normal state		BUSCLK = 500 MHz P0:2 = 000; load see Figure 1				70	mA

† V_{DD} refers to any of the following; V_{DD}PA, V_{DD}PD, V_{DD}REF, V_{DD}O, and V_{DD}P
‡ All typical values are at V_{DD} = 3.3 V, T_A = 25°C.

jitter specification over recommended operating free-air temperature range and V_{CC} (unless otherwise noted)

PARAMETER	CLKOUT	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{(jitter)}$ (Multiplication only mode. Phase alignment and programmable delay features are not selected (PA bypass). See Figure 2.)	155 MHz	Period RMS (1Σ jitter, full frequency band)		6.0		ps
		Period p-p		40		
		Phase jitter (accumulated, 12 kHz to 20 MHz)		50		
		Cycle-to-cycle (+)		27		
		Cycle-to-cycle (–)		27		
	200 MHz	Period RMS (1Σ jitter, full frequency band)		5.5		ps
		Period p-p		36		
		Phase jitter (accumulated, 12 kHz to 20 MHz)		36		
		Phase jitter (accumulated, 50 kHz to 80 MHz)		36		
		Cycle-to-cycle (+)		23		
		Cycle-to-cycle (–)		23		
	312 MHz	Period RMS (1Σ jitter, full frequency band)		3.0		ps
		Period p-p		20		
		Phase jitter (accumulated, 12 kHz to 20 MHz)		18		
		Phase jitter (accumulated, 50 kHz to 80 MHz)		18		
		Cycle-to-cycle (+)		17		
		Cycle-to-cycle (–)		17		
	400 MHz	Period RMS (1Σ jitter, full frequency band)		2.3		ps
		Period p-p		17		
		Phase jitter (accumulated, 12 kHz to 20 MHz)		12		
		Phase jitter (accumulated, 50 kHz to 80 MHz)		12		
		Cycle-to-cycle (+)		15		
		Cycle-to-cycle (–)		15		
	500 MHz	Period RMS (1Σ jitter, full frequency band)		2.1		ps
		Period p-p		16		
		Phase jitter (accumulated, 12 kHz to 20 MHz)		8		
		Phase jitter (accumulated, 50 kHz to 80 MHz)		8		
		Cycle-to-cycle (+)		14		
		Cycle-to-cycle (–)		14		
$t_{(jitter)}$ (Multiplication with phase alignment and programmable delay features selected. See Figure 2.)	155 MHz	Period RMS (1Σ jitter, full frequency band)		9.0		ps
		Period p-p		70		
		Phase jitter (accumulated, 12 kHz to 20 MHz)		50		
		Cycle-to-cycle (+)		50		
		Cycle-to-cycle (–)		50		
	200 MHz	Period RMS (1Σ jitter, full frequency band)		7.0		ps
		Period p-p		55		
		Phase jitter (accumulated, 12 kHz to 20 MHz)		36		
		Phase jitter (accumulated, 50 kHz to 80 MHz)		36		
		Cycle-to-cycle (+)		40		
		Cycle-to-cycle (–)		40		
	312 MHz	Period RMS (1Σ jitter, full frequency band)		4.0		ps
		Period p-p		35		
		Phase jitter (accumulated, 12 kHz to 20 MHz)		18		
		Phase jitter (accumulated, 50 kHz to 80 MHz)		18		
		Cycle-to-cycle (+)		30		
		Cycle-to-cycle (–)		30		
	400 MHz	Period RMS (1Σ jitter, full frequency band)		3.1		ps
		Period p-p		27		
		Phase jitter (accumulated, 12 kHz to 20 MHz)		13		
		Phase jitter (accumulated, 50 kHz to 80 MHz)		13		
		Cycle-to-cycle (+)		25		
		Cycle-to-cycle (–)		25		

† All typical values are at V_{DD} = 3.3 V, T_A = 25°C.

jitter specification over recommended operating free-air temperature range and V_{CC} (unless otherwise noted) (continued)

PARAMETER		CLKOUT	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{(jitter)}$ (Multiplication with phase alignment and programmable delay features selected. See Figure 2.)		500 MHz	Period RMS (1Σ jitter, full frequency band) Period p-p Phase jitter (accumulated, 12 kHz to 20 MHz) Phase jitter (accumulated, 50 kHz to 80 MHz) Cycle-to-cycle (+) Cycle-to-cycle (–)		2.9 24 9 9 20 20		ps
$t_{(jitter)}$ (Divider mode with phase aligner not active: DLYCTRL =LEADLAG = 0 or 1. See Figure 2.)	MULT0:1 = 11 (Divider ratio = 4)	12.5 MHz	Period RMS (1Σ jitter, full frequency band) Period p-p Cycle-to-cycle (+) Cycle-to-cycle (–)		12.0 75 55 55		ps
		15.5 MHz	Period RMS (1Σ jitter, full frequency band) Period p-p Cycle-to-cycle (+) Cycle-to-cycle (–)		8.0 50 38 38		ps
	MULT0:1 = 10 (Divider ratio = 3)	25.0 MHz	Period RMS (1Σ jitter, full frequency band) Period p-p Cycle-to-cycle (+) Cycle-to-cycle (–)		7.5 50 35 35		ps
		31.0 MHz	Period RMS (1Σ jitter, full frequency band) Period p-p Cycle-to-cycle (+) Cycle-to-cycle (–)		5.5 30 23 23		ps
	MULT0:1 = 00 (Divider ratio = 2)	50.0 MHz	Period RMS (1Σ jitter, full frequency band) Period p-p Phase jitter (accumulated, 12 kHz to 20 MHz) Cycle-to-cycle (+) Cycle-to-cycle (–)		8.0 40 12 30 30		ps
		62.5 MHz	Period RMS (1Σ jitter, full frequency band) Period p-p Phase jitter (accumulated, 12 kHz to 20 MHz) Cycle-to-cycle (+) Cycle-to-cycle (–)		5.5 28 9 24 24		ps
$t_{(jitter)}$ (Divider mode with phase alignment and programmable delay features selected. See Figure 2.)	MULT0:1 = 11 (Divider ratio = 4)	12.5 MHz	Period RMS (1Σ jitter, full frequency band) Period p-p Cycle-to-cycle (+) Cycle-to-cycle (–)		12.5 80 55 55		ps
		15.5 MHz	Period RMS (1Σ jitter, full frequency band) Period p-p Cycle-to-cycle (+) Cycle-to-cycle (–)		8.5 55 38 38		ps
	MULT0:1 = 10 (Divider ratio = 3)	25.0 MHz	Period RMS (1Σ jitter, full frequency band) Period p-p Cycle-to-cycle (+) Cycle-to-cycle (–)		10.0 60 35 35		ps
		31.0 MHz	Period RMS (1Σ jitter, full frequency band) Period p-p Cycle-to-cycle (+) Cycle-to-cycle (–)		7.0 40 23 23		ps

jitter specification over recommended operating free-air temperature range and V_{CC} (unless otherwise noted) (continued)

PARAMETER		CLKOUT	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{(jitter)}$ (Divider mode with phase alignment and programmable delay features selected. See Figure 2.)	MULT0:1 = 00 (Divider ratio = 2)	50.0 MHz	Period RMS (1Σ jitter, full frequency band)		9.0		ps
			Period p-p		50		
			Phase jitter (accumulated, 12 kHz to 20 MHz)		13		
			Cycle-to-cycle (+)		35		
			Cycle-to-cycle (–)		35		
		62.5 MHz	Period RMS (1Σ jitter, full frequency band)		6.5		ps
			Period p-p		30		
			Phase jitter (accumulated, 12 kHz to 20 MHz)		10		
			Cycle-to-cycle (+)		26		
			Cycle-to-cycle (–)		26		

† All typical values are at V_{DD} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{(DC)}$	Output duty cycle	See Figure 3	45%		55%	
t_r, t_f	Output rise and fall times (measured at 20%–80% of output voltage)	See Figure 5 and Figure 1	150		350	ps

† All typical values are at V_{DD} = 3.3 V, T_A = 25°C.

state transition latency specifications

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{(powerup)}$	Delay time, PWRDNB↑ to CLKOUT/CLKOUTB output settled (excluding $t_{(DISTLOCK)}$)	Powerdown	Normal	See Figure 6			3	ms
	Delay time, PWRDNB↑ to internal PLL and clock are on and settled						3	
$t_{(VDDpowerup)}$	Delay time, power up to CLKOUT/CLKOUTB output settled	V_{DD}	Normal	See Figure 6			3	ms
	Delay time, power up to internal PLL and clock are on and settled						3	
$t_{(MULT)}$	MULT0 and MULT1 change to CLKOUT/CLKOUTB output resettled (excluding $t_{(DISTLOCK)}$)	Normal	Normal	See Figure 7			1	ms
$t_{(CLKON)}$	STOPB↑ to CLKOUT/CLKOUTB glitch-free clock edges	CLK Stop	Normal	See Figure 8			10	ns
$t_{(CLKSETL)}$	STOPB↑ to CLKOUT/CLKOUTB output settled to within 50 ps of the phase before STOPB was disabled	CLK Stop	Normal	See Figure 8			20	cycles
$t_{(CLKOFF)}$	STOPB↓ to CLKOUT/CLKOUTB output disabled	Normal	CLK Stop	See Figure 8			5	ns
$t_{(powerdown)}$	Delay time, PWRDNB↓ to the device in the power-down mode	Normal	Power–down	See Figure 6			1	ms
$t_{(STOP)}$	Maximum time in CLKSTOP (STOPB = 0) before reentering normal mode (STOPB = 1)	STOPB	Normal	See Figure 8			100	µs
$t_{(ON)}$	Minimum time in normal mode (STOPB = 1) before reentering CLKSTOP (STOPB = 0)	Normal	CLK stop	See Figure 8	100			ms

† All typical values are at V_{DD} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

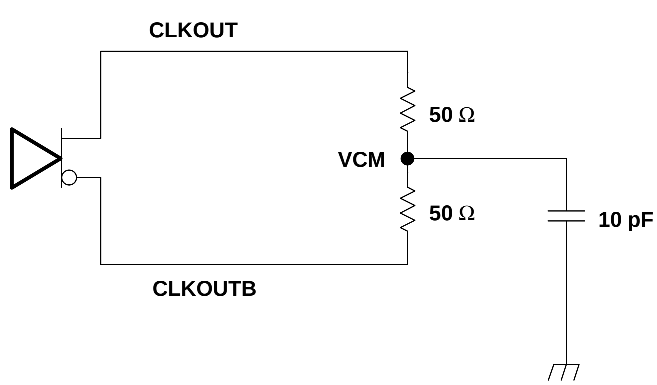
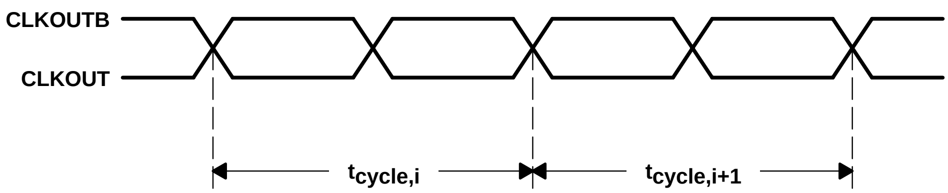


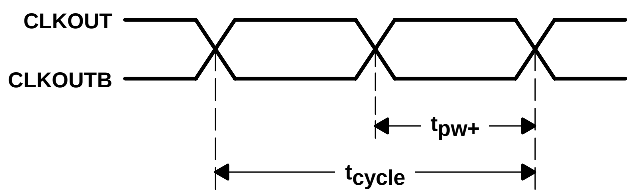
Figure 1. Test Load and Voltage Definitions ($V_{O(STOP)}$, V_{OX}, V_{OH}, V_{OL})

PARAMETER MEASUREMENT INFORMATION



Cycle-to-Cycle Jitter = | $t_{cycle,i}$ – $t_{cycle,i+r}$| Over 1000 Consecutive Cycles

Figure 2. Cycle-to-Cycle Jitter



Duty Cycle = (t_{pw+}/t_{cycle})

Figure 3. Output Duty Cycle

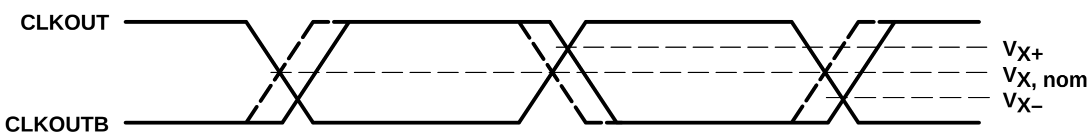


Figure 4. Crossing-Point Voltage

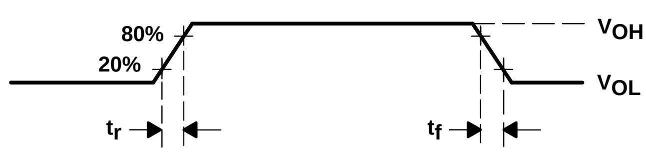


Figure 5. Voltage Waveforms

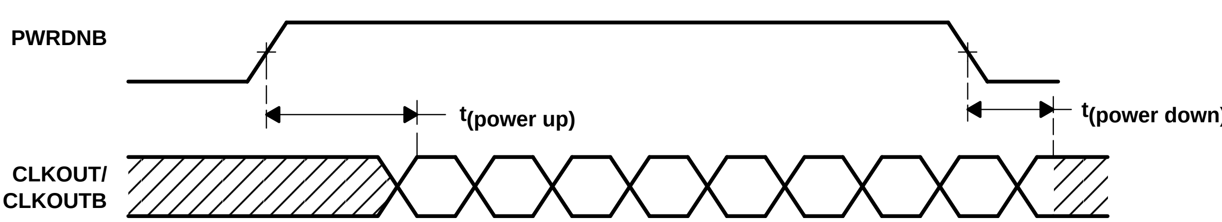


Figure 6. PWRDNB Transition Timings

PARAMETER MEASUREMENT INFORMATION

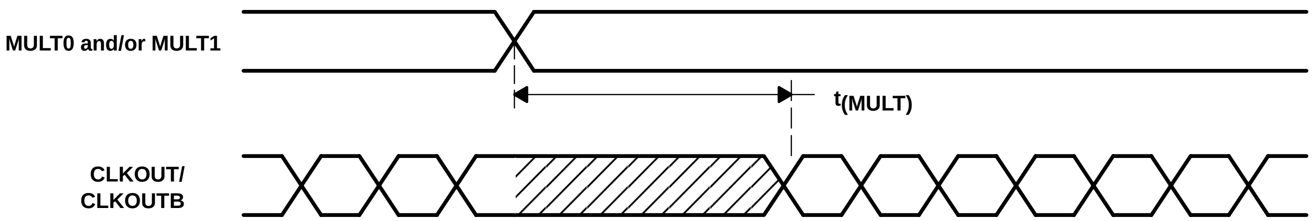
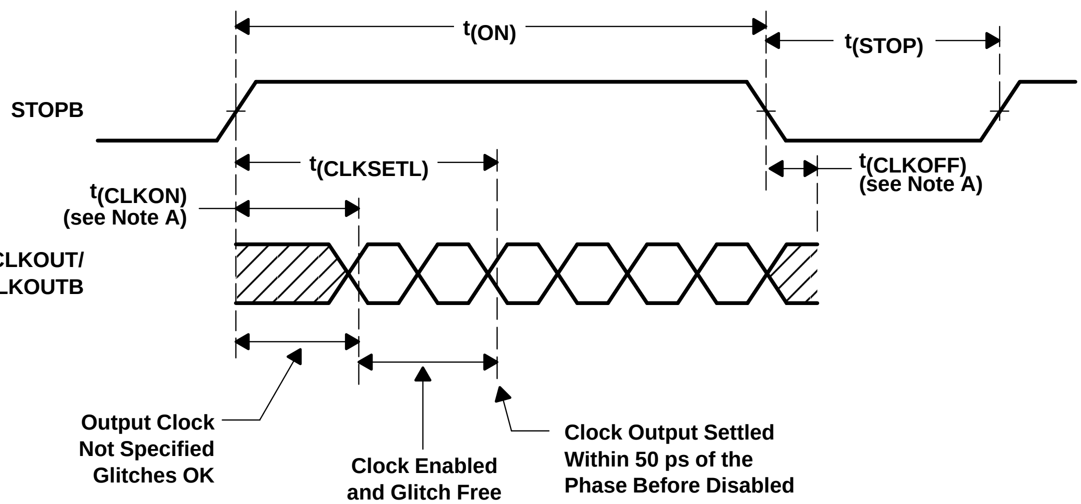


Figure 7. MULT Transition Timings



NOTE A: $V_{ref} = V_O \pm 200$ mV

Figure 8. STOPB Transition Timings

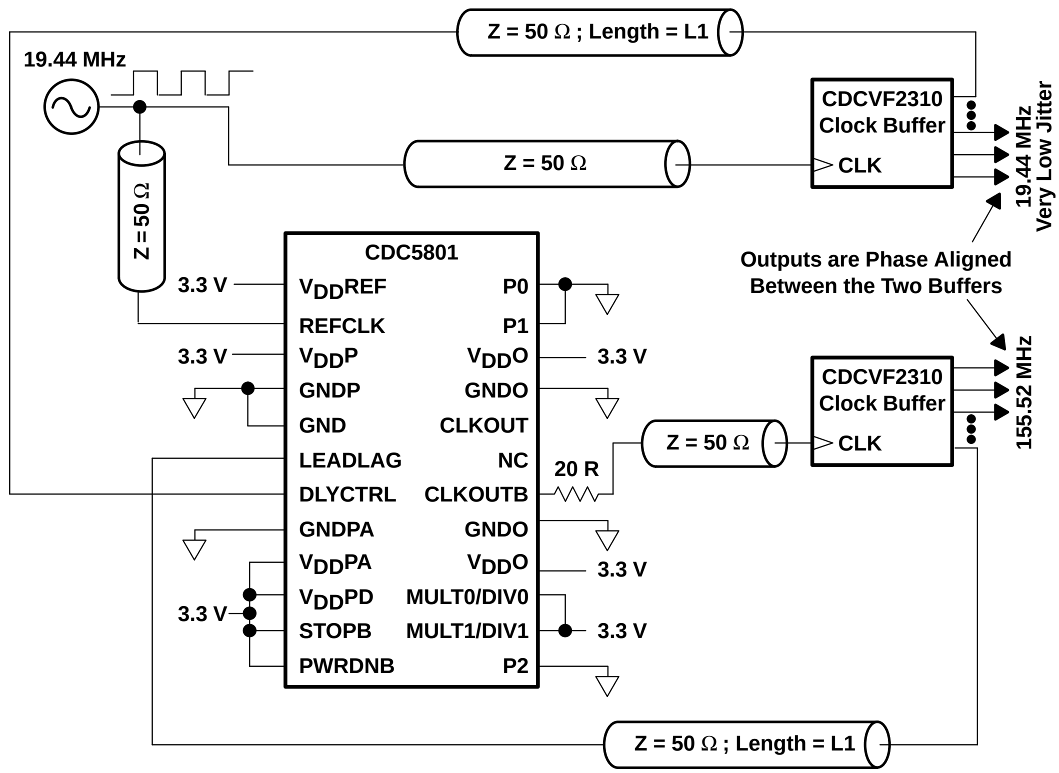
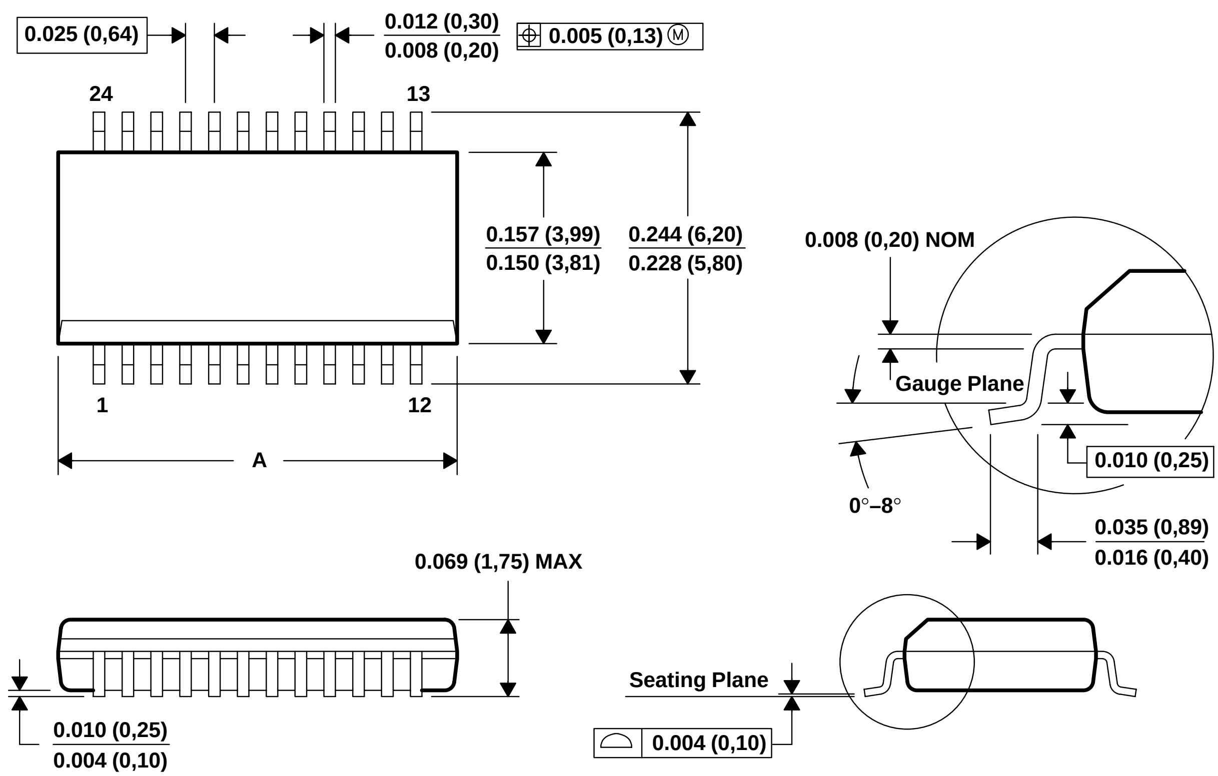


Figure 9. Using the CDC5801 Device as a Multiplier by 8 and Aligning Two Different Clocks

MECHANICAL DATA

DBQ (R–PDSO–G)** **PLASTIC SMALL–OUTLINE PACKAGE**



DIM \ PINS **	16	20	24	28
A MAX	0.197 (5,00)	0.344 (8,74)	0.344 (8,74)	0.394 (10,01)
A MIN	0.189 (4,80)	0.337 (8,56)	0.337 (8,56)	0.386 (9,80)
D M0–137 VARIATION	AB	AD	AE	AF

4073301/F 02/02

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–137.

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