

133-MHz CLOCK SYNTHESIZER/DRIVER FOR PC MOTHERBOARDS WITH 3-STATE OUTPUTS

SCAS633 – JULY 28, 1999

- Supports Pentium III™ Class Motherboards
- Uses a 14.318-MHz Crystal Input to Generate Multiple Output Frequencies
- Includes Spread Spectrum Clocking (SSC), 0.34% Downspread for Reduced EMI Performance
- Power Management Control Terminals
- Low Output Skew and Jitter for Clock Distribution
- 2.5-V and 3.3-V Supplies
- Generates the Following Clocks:
 - 4 CPU (2.5 V, 100/133 MHz)
 - 7 PCI (3.3 V, 33.3 MHz)
 - 1 PCI_F (Free Running, 3.3 V, 33.3 MHz)
 - 2 CPU/2 (2.5 V, 50/66 MHz)
 - 3 APIC (2.5 V, 16.67 MHz)
 - 4 3V66 (3.3 V, 66 MHz)
 - 2 REF (3.3 V, 14.318 MHz)
 - 1 48MHz (3.3 V, 48 MHz)
- Packaged in 56-Pin SSOP Package
- Designed for Use with TI's Direct Rambus™ Clock Generators (CDCR81, CDCR82, CDCR83)

DL PACKAGE (TOP VIEW)

GND	1	56	V _{DD} 2.5V
REF0	2	55	APIC2
REF1	3	54	APIC1
V _{DD} 3.3V	4	53	APIC0
XIN	5	52	GND
XOUT	6	51	V _{DD} 2.5V
GND	7	50	CPU_DIV2(1)
PCI_F	8	49	CPU_DIV2(0)
PCI1	9	48	GND
V _{DD} 3.3V	10	47	V _{DD} 2.5V
PCI2	11	46	CPU3
PCI3	12	45	CPU2
GND	13	44	GND
PCI4	14	43	V _{DD} 2.5V
PCI5	15	42	CPU1
V _{DD} 3.3V	16	41	CPU0
PCI6	17	40	GND
PCI7	18	39	V _{DD} 3.3V
GND	19	38	GND
GND	20	37	PCI_STOP
3V66(0)	21	36	CPU_STOP
3V66(1)	22	35	PWR_DWN
V _{DD} 3.3V	23	34	SPREAD
GND	24	33	SEL1
3V66(2)	25	32	SEL0
3V66(3)	26	31	V _{DD} 3.3V
V _{DD} 3.3V	27	30	48MHz
SEL133/100	28	29	GND

description

The CDC925 is a clock synthesizer/driver that generates system clocks necessary to support Intel Pentium III systems on CPU, CPU_DIV2, 3V66, PCI, APIC, 48MHz, and REF clock signals.

All output frequencies are generated from a 14.318-MHz crystal input. A reference clock input instead of a crystal can be provided at the XIN input. Two phase-locked loops (PLLs) are used, one to generate the host frequencies and the other to generate the 48-MHz clock frequency. On-chip loop filters and internal feedback loops eliminate the need for external components.

The host and PCI clock outputs provide low-skew and low-jitter clock signals for reliable clock operation. All outputs have 3-state capability, which can be selected via control inputs SEL0, SEL1, and SEL133/100.

The outputs are either 3.3-V or 2.5-V single-ended CMOS buffers. With a logic high-level on the PWR_DWN terminal, the device operates normally, but when a logical low-level input is applied, the device powers down completely, with the outputs in a low-level output state. When a high-level is applied to the PCI_STOP or CPU_STOP, the outputs operate normally. With a low-level applied to the PCI_STOP or CPU_STOP terminals, the PCI or CPU and 3V66 outputs, respectively, are held in a low-level state.

The CPU bus can operate at 100 MHz or 133 MHz. Output frequency selection is done with corresponding setting for SEL133/100 control input. The PCI bus frequency is fixed to 33MHz.



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description (continued)

Since the CDC925 is based on PLL circuitry, it requires a stabilization time to achieve phase lock of the PLL. This stabilization time is required after power up or after changes to the SEL inputs are made. With use of an external reference clock, this signal must be fixed-frequency and fixed-phase before the stabilization time starts.

function tables

SELECT FUNCTIONS

INPUTS			OUTPUTS							FUNCTION
SEL133/ 100	SEL1	SEL0	CPU	CPU_DIV2	3V66	PCI, PCI_F	48MHz	REF	APIC	
L	L	L	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	3-state
L	L	H	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
L	H	L	100 MHz	50 MHz	66 MHz	33 MHz	Hi-Z	14.318 MHz	16.67 MHz	48-MHz PLL off
L	H	H	100 MHz	50 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	16.67 MHz	48-MHz PLL on
H	L	L	TCLK/2	TCLK/4	TCLK/4	TCLK/8	TCLK/2	TCLK	TCLK/16	Test
H	L	H	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
H	H	L	133 MHz	66 MHz	66 MHz	33 MHz	Hi-Z	14.318 MHz	16.67 MHz	48-MHz PLL off
H	H	H	133 MHz	66 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	16.67 MHz	48-MHz PLL on

ENABLE FUNCTIONS

INPUTS			OUTPUTS							INTERNAL	
CPU_STOP	PWR_DWN	PCI_STOP	CPU	CPU_DIV2	APIC	3V66	PCI	PCI_F	REF, 48MHz	Crystal	VCOs
X	L	X	L	L	L	L	L	L	L	Off	Off
L	H	L	L	On	On	L	L	On	On	On	On
L	H	H	L	On	On	L	On	On	On	On	On
H	H	L	On	On	On	On	L	On	On	On	On
H	H	H	On	On	On	On	On	On	On	On	On

OUTPUT BUFFER SPECIFICATIONS

BUFFER NAME	V _{DD} RANGE (V)	IMPEDANCE (Ω)	BUFFER TYPE
CPU, CPU_DIV2, APIC	2.375 – 2.625	13.5 – 45	TYPE 1
48MHz, REF	3.135 – 3.465	20 – 60	TYPE 3
PCI, PCI_F, 3V66	3.135 – 3.465	12 – 55	TYPE 5

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Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
3V66 [0–3]	21, 22, 25, 26	O	3.3 V, Type 5, 66-MHz clock outputs
48MHz	30	O	3.3 V, Type 3, 48-MHz clock output
APIC [0–2]	53, 54, 55	O	2.5 V, Type 1, APIC clock outputs
CPU [0–3]	41, 42, 45, 46	O	2.5 V, Type 1, CPU clock outputs
CPU_DIV2 [0–1]	49, 50	O	2.5 V, Type 1, CPU_DIV2 clock outputs
$\overline{\text{CPU_STOP}}$	36	I	Disables CPU clock to low state
GND	1, 7, 13, 19, 20, 24, 29, 38, 40, 44, 48, 52		Ground
PCI [1–7]	9, 11, 12, 14, 15, 17, 18	O	3.3 V, Type 5, 33-MHz PCI clock outputs
$\overline{\text{PCI_F}}$	8	O	Free-running 3.3-V, Type 5, 33-MHz PCI clock output
$\overline{\text{PCI_STOP}}$	37	I	Disables PCI clock to low state
$\overline{\text{PWR_DWN}}$	35	I	Power down for complete device with outputs forced low
REF0, REF1	2, 3	O	3.3 V, Type 3, 14.318-MHz reference clock output
SEL0, SEL1	32, 33	I	LVTTL level logic select terminals for function selection
$\overline{\text{SEL133/100}}$	28	I	LVTTL level logic select pins for enabling 100/133 MHz
$\overline{\text{SPREAD}}$	34	I	Disables SSC function
V _{DD} 3.3V	4, 10, 16, 23, 27, 31, 39		Power for the 3V66, 48MHz, PCI, REF outputs and CORE logic
V _{DD} 2.5V	43, 47, 51, 56		Power for CPU and APIC outputs
XIN	5	I	Crystal input – 14.318 MHz
XOUT	6	O	Crystal output – 14.318 MHz

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spread spectrum clock (SSC) implementation for CDC925

Simultaneously switching at fixed frequency generates a significant power peak at the selected frequency, which in turn will cause EMI disturbance to the environment. The purpose of the internal frequency modulation of the CPU-PLL allows to distribute the energy to many different frequencies which reduces the power peak. A typical characteristic for a single frequency spectrum and a frequency modulated spectrum is shown in Figure 1.

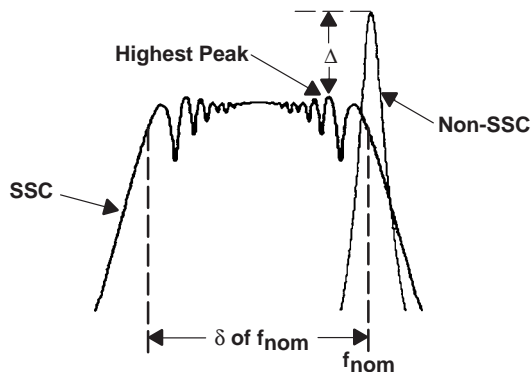


Figure 1. Frequency Power Spectrum With and Without the Use of SSC

The modulated spectrum has its distribution left hand to the single frequency spectrum which indicates a “down-spread modulation”.

The peak reduction depends on the modulation scheme and modulation profile. System performance and timing requirements are the limiting factors for actual design implementations. The implementation was driven to keep the average clock frequency closed to its upper specification limit. The modulation amount was set to approximately -0.34% (compared to -0.5% on the CDC924).

In order to allow a downstream PLL to follow the frequency modulated signal, the bandwidth of the modulation signal is limited in order to minimize SSC induced tracking skew jitter. The ideal modulation profile used for CDC925 is shown in Figure 2.

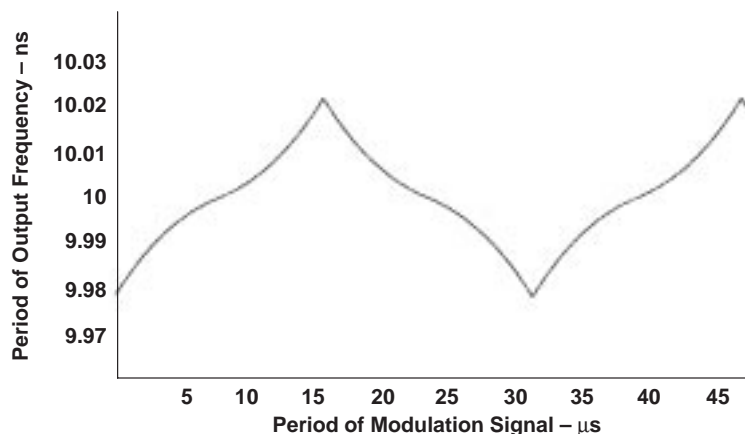


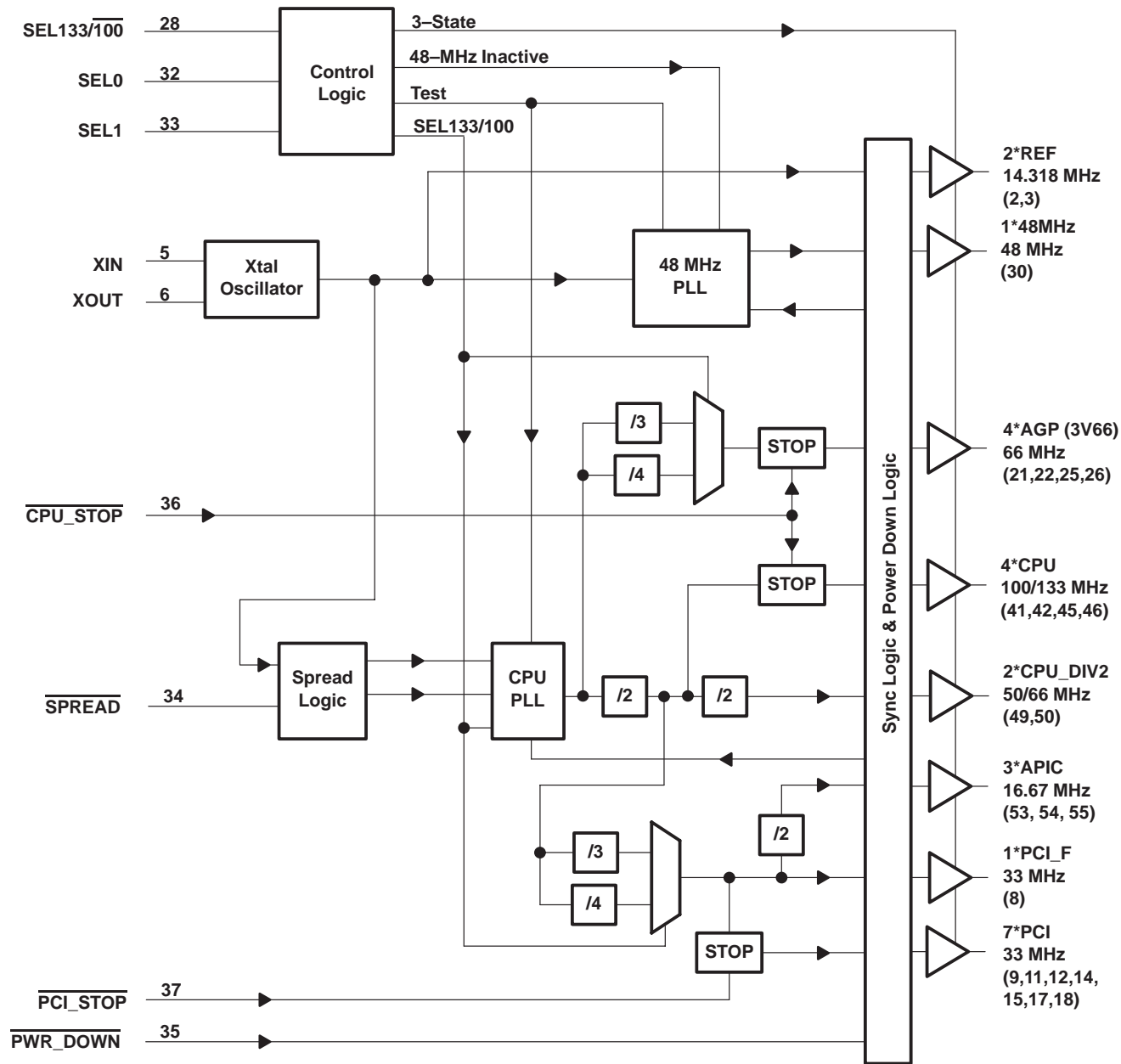
Figure 2. SSC Modulation Profile

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functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance state or power-off state, V_O (see Note 1)	-0.5 V to $V_{DD} + 0.5$ V
Current into any output in the low state, I_O	$2 \times I_{OL}$
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Operating free-air temperature range, T_A	-0°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATNG	DERATING FACTOR† ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DL	1558.6 mW	12.468 mW/°C	997.5 mW	810.52 mW

† This is the inverse of the traditional junction-to-case thermal resistance ($R_{\theta JA}$) and uses a board-mounted device at 80.2°C/W.

recommended operating conditions (see Note 2)

		MIN	NOM†	MAX	UNIT
Supply voltage, V_{DD}	3.3 V	3.135		3.465	V
	2.5 V	2.375		2.625	
High-level input voltage, V_{IH}		2		$V_{DD} + 0.3$ V	V
Low-level input voltage, V_{IL}		GND – 0.3 V		0.8	V
Input voltage, V_I		0		V_{DD}	V
High-level output current, I_{OH}	CPUx, CPU_DIV2x			-12	mA
	APICx			-12	
	48MHz, REFx			-14	
	PCIx, PCI_F, 3V66x			-18	
Low-level output current, I_{OL}	CPUx, CPU_DIV2x			12	mA
	APICx			12	
	48MHz, REFx			9	
	PCIx, PCI_F, 3V66x			12	
Reference frequency, $f_{(XIN)}^\ddagger$	Test mode		130		MHz
Crystal frequency, $f_{(XTAL)}^\S$	Normal mode	13.8	14.318	14.8	MHz
Operating free-air temperature, T_A		0		85	°C

NOTE 2: Unused inputs must be held high or low to prevent them from floating.

† All nominal values are measured at their respective nominal V_{DD} values.

‡ Reference frequency is a test clock driven on the XIN input during the device test mode and normal mode. In test mode, XIN can be driven externally up to $f_{(XIN)} = 130$ MHz. If XIN is driven externally, XOUT is floating.

§ This is a series fundamental crystal with $f_O = 14.31818$ MHz.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}	Input clamp voltage	V _{DD} = 3.135 V, I _I = -18 mA				-1.2	V
R _I	Input resistance	XIN-XOUT	V _{DD} = 3.465 V, V _I = V _{DD} - 0.5 V	80		350	kΩ
I _{IH}	High-level input current	XOUT	V _{DD} = 3.135 V, V _I = V _{DD} - 0.5 V		20	50	mA
		SEL0, SEL1, CPU_STOP, PCI_STOP, SPREAD	V _{DD} = 3.465 V, V _I = V _{DD}		<10	10	μA
		PWR_DWN	V _{DD} = 3.465 V, V _I = V _{DD}		<10	10	μA
		SEL133/100	V _{DD} = 3.465 V, V _I = V _{DD}		<10	10	μA
I _{IL}	Low-level input current	XOUT	V _{DD} = 3.135 V, V _O = 0 V		-2	-5	mA
		SEL0, SEL1, CPU_STOP, PCI_STOP, SPREAD	V _{DD} = 3.465 V, V _I = GND		<10	-10	μA
		PWR_DWN	V _{DD} = 3.465 V, V _I = GND		<10	-10	μA
		SEL133/100	V _{DD} = 3.465 V, V _I = GND		<10	-10	μA
I _{OZ}	High-impedance-state output current	V _{DD} = max, V _O = V _{DD} or GND				±10	μA
I _{DD}	Supply current	V _{DD} = 2.625 V, All outputs = low, PWR_DWN = low,			<20	100	μA
		V _{DD} = 2.625 V, All outputs = high, V _{DDx} = 2.5 V,			<20	100	
		V _{DD} = 3.465 V, All outputs = low, PWR_DWN = low,			<50	200	
		V _{DD} = 3.465 V, All outputs = high			12	35	mA
I _{DD(Z)}	High-impedance-state supply current	V _{DD} = 2.625 V				1.4	mA
		V _{DD} = 3.465 V				28	
Dynamic supply current		C _L = 20 pF, CPU = 133 MHz	V _{DD} = 3.465 V		114	146	mA
			V _{DD} = 2.625 V		52	70	
C _I	Input capacitance	V _{DD} = 3.3 V, V _I = V _{DD} or GND		3.3		5.8	pF
Crystal terminal capacitance		V _{DD} = 3.3 V, V _I = 0.3 V		18	18.5	22.5	pF

† All typical values are measured at their respective nominal V_{DD} values.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

CPUx, CPU_DIV2x, APICx (Type 1)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{OH}	High-level output voltage	V _{DD} = min to max, I _{OH} = -1 mA	V _{DD} - 0.1 V			V
		V _{DD} = 2.375 V, I _{OH} = -12 mA	2			
V _{OL}	Low-level output voltage	V _{DD} = min to max, I _{OL} = 1 mA			0.1	V
		V _{DD} = 2.375 V, I _{OL} = 12 mA	0.18		0.4	
I _{OH}	High-level output current	V _{DD} = 2.375 V, V _O = 1 V	-26	-42		mA
		V _{DD} = 2.5 V, V _O = 1.25 V			-46	
		V _{DD} = 2.625 V, V _O = 2.375 V			-16 -27	
I _{OL}	Low-level output current	V _{DD} = 2.375 V, V _O = 1.2 V	27	57		mA
		V _{DD} = 2.5 V, V _O = 1.25 V			63	
		V _{DD} = 2.625 V, V _O = 0.3 V			23 43	
C _O	Output capacitance	V _{DD} = 3.3 V, V _O = V _{DD} or GND	6		8.5	pF
Z _O	Output impedance	High state V _O = 0.5 V _{DD} , V _O /I _{OH}	13.5	27	45	Ω
		Low state V _O = 0.5 V _{DD} , V _O /I _{OL}	13.5	20	45	

† All typical values are measured at their respective nominal V_{DD} values.

48MHz, REFx (Type 3)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{OH}	High-level output voltage	V _{DD} = min to max, I _{OH} = -1 mA	V _{DD} - 0.1 V			V
		V _{DD} = 3.135 V, I _{OH} = -14 mA	2.4			
V _{OL}	Low-level output voltage	V _{DD} = min to max, I _{OL} = 1 mA			0.1	V
		V _{DD} = 3.135 V, I _{OL} = 9 mA	0.18		0.4	
I _{OH}	High-level output current	V _{DD} = 3.135 V, V _O = 1 V	-27	-41		mA
		V _{DD} = 3.3 V, V _O = 1.65 V			-41	
		V _{DD} = 3.465 V, V _O = 3.135 V			-12 -23	
I _{OL}	Low-level output current	V _{DD} = 3.135 V, V _O = 1.95 V	29	50		mA
		V _{DD} = 3.3 V, V _O = 1.65 V			53	
		V _{DD} = 3.465 V, V _O = 0.4 V			20 37	
C _O	Output capacitance	V _{DD} = 3.3 V, V _O = V _{DD} or GND	4.5		7	pF
Z _O	Output impedance	High state V _O = 0.5 V _{DD} , V _O /I _{OH}	20	40	60	Ω
		Low state V _O = 0.5 V _{DD} , V _O /I _{OL}	20	31	60	

† All typical values are measured at their respective nominal V_{DD} values.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PCIx, PCI_F, 3V66x (Type 5)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{OH}	High-level output voltage	V _{DD} = min to max,	I _{OH} = -1 mA	V _{DD} - 0.1 V			V
		V _{DD} = 3.135 V,	I _{OH} = -18 mA	2.4			
V _{OL}	Low-level output voltage	V _{DD} = min to max,	I _{OL} = 1 mA			0.1	V
		V _{DD} = 3.135 V,	I _{OL} = 12 mA	0.15	0.4		
I _{OH}	High-level output current	V _{DD} = 3.135 V,	V _O = 1 V	-33	-53		mA
		V _{DD} = 3.3 V,	V _O = 1.65 V		-53		
		V _{DD} = 3.465 V,	V _O = 3.135 V		-16	-33	
I _{OL}	Low-level output current	V _{DD} = 3.135 V,	V _O = 1.95 V	30	67		mA
		V _{DD} = 3.3 V,	V _O = 1.65 V		70		
		V _{DD} = 3.465 V,	V _O = 0.4 V		27	49	
C _O	Output capacitance	V _{DD} = 3.3 V,	V _O = V _{DD} or GND	4.5		7.5	pF
Z _O	Output impedance	High state	V _O = 0.5 V _{DD} , V _O /I _{OH}	12	31	55	Ω
		Low state	V _O = 0.5 V _{DD} , V _O /I _{OL}	12	24	55	

† All typical values are measured at their respective nominal V_{DD} values.

switching characteristics, V_{DD} = 3.135 V to 3.465 V, T_A = 0°C to 85°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Overshoot/undershoot				GND - 0.7 V		V _{DD} + 0.7 V	V
Ring back				V _{IL} - 0.1 V		V _{IH} + 0.1 V	V
Stabilization time, PWR_DWN to PCIx		f(CPU) = 133 MHz			0.05	3	ms
t _{dis3}	Disable time, PWR_DWN to PCIx	f(CPU) = 133 MHz			50		ns
Stabilization time, PWR_DWN to CPUx		f(CPU) = 133 MHz			0.03	3	ms
t _{dis4}	Disable time, PWR_DWN to CPUx	f(CPU) = 133 MHz			50		ns
Stabilization time T		After SEL1, SEL0				3	ms
		After power up				3	

† Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at XIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics tables are not applicable. Stabilization time is defined as the time from when V_{DD} achieves its nominal operating level until the output frequency is stable and operating within specification.

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switching characteristics, $V_{DD} = 2.375\text{ V to }2.625\text{ V}$, $T_A = 0^\circ\text{C to }85^\circ\text{C}$ (continued)

CPUx

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{en1}	Output enable time	SEL133/100	CPUx	$f_{(CPU)} = 100\text{ or }133\text{MHz}$		6	10	ns
t_{dis1}	Output disable time	SEL133/100	CPUx	$f_{(CPU)} = 100\text{ or }133\text{MHz}$		8	10	ns
t_c	CPU clock period†			$f_{(CPU)} = 100\text{ MHz}$	10	10.04	10.2	ns
				$f_{(CPU)} = 133\text{ MHz}$	7.5	7.53	7.7	ns
Cycle to cycle jitter				$f_{(CPU)} = 100\text{ or }133\text{MHz}$			250	ps
Duty cycle				$f_{(CPU)} = 100\text{ or }133\text{MHz}$	45		55	%
$t_{sk(o)}$	CPU bus skew	CPUx	CPUx	$f_{(CPU)} = 100\text{ or }133\text{MHz}$		50	175	ps
$t_{sk(p)}$	CPU pulse skew	CPU _n	CPU _n	$f_{(CPU)} = 100\text{ or }133\text{MHz}$			2.2	ns
$t_{(off)}$	CPU clock to APIC clock offset, rising edge				1.5	2.8	4	ns
$t_{(off)}$	CPU clock to 3V66 clock offset, rising edge				0	0.75	1.5	ns
t_{w1}	Pulse duration width, high			$f_{(CPU)} = 100\text{ MHz}$	2.6	4.3		ns
				$f_{(CPU)} = 133\text{ MHz}$	1.4	3.7		
t_{w2}	Pulse duration width, low			$f_{(CPU)} = 100\text{ MHz}$	2.8	4.3		ns
				$f_{(CPU)} = 133\text{ MHz}$	1.7	4		
t_r	Rise time			$V_O = 0.4\text{ V to }2.0\text{ V}$	0.4	1.5	2.2	ns
t_f	Fall time			$V_O = 0.4\text{ V to }2.0\text{ V}$	0.4	1.4	2	ns

† The average over any 1- μs period of time is greater than the minimum specified period.

CPU_DIV2x

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{en1}	Output enable time	SEL133/100	CPU_DIV2x	$f_{(CPU)} = 100\text{ or }133\text{MHz}$		6	10	ns
t_{dis1}	Output disable time	SEL133/100	CPU_DIV2x	$f_{(CPU)} = 100\text{ or }133\text{MHz}$		8	10	ns
t_c	CPU_DIV2 clock period†			$f_{(CPU)} = 100\text{ MHz}$	20	20.08	20.4	ns
				$f_{(CPU)} = 133\text{ MHz}$	15	15.06	15.3	ns
Cycle to cycle jitter				$f_{(CPU)} = 100\text{ or }133\text{MHz}$			250	ps
Duty cycle				$f_{(CPU)} = 100\text{ or }133\text{MHz}$	45		55	%
$t_{sk(o)}$	CPU_DIV2 bus skew	CPU_DIV2x	CPU_DIV2x	$f_{(CPU)} = 100\text{ or }133\text{MHz}$		50	175	ps
$t_{sk(p)}$	CPU_DIV2 pulse skew	CPU_DIV2n	CPU_DIV2n	$f_{(CPU)} = 100\text{ or }133\text{MHz}$			1.6	ns
t_{w1}	Pulse duration width, high			$f_{(CPU)} = 100\text{ MHz}$	7.1			ns
				$f_{(CPU)} = 133\text{ MHz}$	4.7			
t_{w2}	Pulse duration width, low			$f_{(CPU)} = 100\text{ MHz}$	7.3	8.9		ns
				$f_{(CPU)} = 133\text{ MHz}$	5	6.6		
t_r	Rise time			$V_O = 0.4\text{ V to }2.0\text{ V}$	0.4	1.4	2	ns
t_f	Fall time			$V_O = 0.4\text{ V to }2.0\text{ V}$	0.4	1.3	1.8	ns

† The average over any 1- μs period of time is greater than the minimum specified period.

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switching characteristics, $V_{DD} = 2.375\text{ V to }2.625\text{ V}$, $T_A = 0^\circ\text{C to }85^\circ\text{C}$ (continued)

APIC

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{en1}	Output enable time	SEL133/100	APICx	$f_{(APIC)} = 16.67\text{ MHz}$		6	10	ns
t_{dis1}	Output disable time	SEL133/100	APICx	$f_{(APIC)} = 16.67\text{ MHz}$		8	10	ns
t_c	APIC clock period†			$f_{(APIC)} = 16.67\text{ MHz}$	60	60.24	60.6	ns
	Cycle to cycle jitter			$f_{(CPU)} = 100\text{ or }133\text{ MHz}$			400	ps
	Duty cycle			$f_{(APIC)} = 16.67\text{ MHz}$	45		55	%
$t_{sk(o)}$	APIC bus skew	APICx	APICx	$f_{(APIC)} = 16.67\text{ MHz}$		30	100	ps
$t_{sk(p)}$	APIC pulse skew	APICn	APICn	$f_{(APIC)} = 16.67\text{ MHz}$			3	ns
$t_{(off)}$	APIC clock to CPU clock offset, rising edge	APICx	CPUx		-1.5		-4	ns
t_{w1}	Pulse duration width, high			$f_{(APIC)} = 16.67\text{ MHz}$	25.5	28		ns
t_{w2}	Pulse duration width, low			$f_{(APIC)} = 16.67\text{ MHz}$	25.3	29.2		ns
t_r	Rise time			$V_O = 0.4\text{ V to }2\text{ V}$	0.4	1.6	2.1	ns
t_f	Fall time			$V_O = 0.4\text{ V to }2\text{ V}$	0.4	1.2	1.7	ns

† The average over any 1- μs period of time is greater than the minimum specified period.

switching characteristics, $V_{DD} = 3.135\text{ V to }3.465\text{ V}$, $T_A = 0^\circ\text{C to }85^\circ\text{C}$

3V66

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{en1}	Output enable time	SEL133/100	3V66x	$f_{(3V66)} = 66\text{ MHz}$		6	10	ns
t_{dis1}	Output disable time	SEL133/100	3V66x	$f_{(3V66)} = 66\text{ MHz}$		8	10	ns
t_c	3V66 clock period†			$f_{(3V66)} = 66\text{ MHz}$	15	15.06	15.3	ns
	Cycle to cycle jitter			$f_{(CPU)} = 100\text{ or }133\text{ MHz}$			400	ps
	Duty cycle			$f_{(3V66)} = 66\text{ MHz}$	45		55	%
$t_{sk(o)}$	3V66 bus skew	3V66x	3V66x	$f_{(3V66)} = 66\text{ MHz}$		50	150	ps
$t_{sk(p)}$	3V66 pulse skew	3V66n	3V66n	$f_{(3V66)} = 66\text{ MHz}$			2.6	ns
$t_{(off)}$	3V66 clock to CPU clock offset	3V66x	CPUx		0	-0.75	-1.5	ns
$t_{(off)}$	3V66 clock to PCI clock offset, rising edge				1.2	2.1	3	ns
t_{w1}	Pulse duration width, high			$f_{(3V66)} = 66\text{ MHz}$	5.2			ns
t_{w2}	Pulse duration width, low			$f_{(3V66)} = 66\text{ MHz}$	5			ns
t_r	Rise time			$V_O = 0.4\text{ V to }2\text{ V}$	0.5	1.5	2	ns
t_f	Fall time			$V_O = 0.4\text{ V to }2\text{ V}$	0.5	1.5	2	ns

† The average over any 1- μs period of time is greater than the minimum specified period.

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switching characteristics, $V_{DD} = 3.135\text{ V to }3.465\text{ V}$, $T_A = 0^\circ\text{C to }85^\circ\text{C}$ (continued)

48MHz

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{en1}	Output enable time	SEL133/100	48MHz	$f_{(48MHz)} = 48\text{ MHz}$		6 10	ns
t_{dis1}	Output disable time	SEL133/100	48MHz	$f_{(48MHz)} = 48\text{ MHz}$		8 10	ns
t_c	48MHz clock period†			$f_{(48MHz)} = 48\text{ MHz}$		20.5 20.83 21.1	ns
	Cycle to cycle jitter			$f_{(CPU)} = 100\text{ or }133\text{ MHz}$		500	ps
	Duty cycle			$f_{(48MHz)} = 48\text{ MHz}$		45 55	%
$t_{sk(p)}$	48MHz pulse skew	48MHz	48MHz	$f_{(48MHz)} = 48\text{ MHz}$		3	ns
t_{w1}	Pulse duration width, high			$f_{(48MHz)} = 48\text{ MHz}$		7.8	ns
t_{w2}	Pulse duration width, low			$f_{(48MHz)} = 48\text{ MHz}$		7.8	ns
t_r	Rise time			$V_O = 0.4\text{ V to }2\text{ V}$		1 2.1 2.8	ns
t_f	Fall time			$V_O = 0.4\text{ V to }2\text{ V}$		1 1.9 2.8	ns

† The average over any 1- μs period of time is greater than the minimum specified period.

REF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{en1}	Output enable time	SEL133/100	REFx	$f_{(REF)} = 14.318\text{ MHz}$		6 10	ns
t_{dis1}	Output disable time	SEL133/100	REFx	$f_{(REF)} = 14.318\text{ MHz}$		8 10	ns
t_c	REF clock period†			$f_{(REF)} = 14.318\text{ MHz}$		69.84	ns
	Cycle to cycle jitter			$f_{(CPU)} = 100\text{ or }133\text{ MHz}$		700	ps
	Duty cycle			$f_{(REF)} = 14.318\text{ MHz}$		45 55	%
$t_{sk(o)}$	REF bus skew	REFx	REFx	$f_{(REF)} = 14.318\text{ MHz}$		150 250	ps
$t_{sk(p)}$	REF pulse skew	REFn	REFn	$f_{(REF)} = 14.318\text{ MHz}$		2	ns
t_{w1}	Pulse duration width, high			$f_{(REF)} = 14.318\text{ MHz}$		26.2 32.7	ns
t_{w2}	Pulse duration width, low			$f_{(REF)} = 14.318\text{ MHz}$		26.2 31.2	ns
t_r	Rise time			$V_O = 0.4\text{ V to }2\text{ V}$		1 2 2.8	ns
t_f	Fall time			$V_O = 0.4\text{ V to }2\text{ V}$		1 1.9 2.8	ns

† The average over any 1- μs period of time is greater than the minimum specified period.

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switching characteristics, $V_{DD} = 3.135\text{ V to }3.465\text{ V}$, $T_A = 0^\circ\text{C to }85^\circ\text{C}$ (continued)

PCI, PCI_F

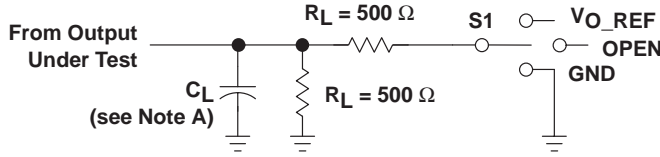
PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{en1}	Output enable time	SEL133/100	PC1x	$f_{(PCI)} = 33\text{ MHz}$		6	10	ns
t_{dis1}	Output disable time	SEL133/100	PC1x	$f_{(PCI)} = 33\text{ MHz}$		8	10	ns
t_c	PC1x clock period [†]			$f_{(PCI)} = 33\text{ MHz}$	30	30.12	30.5	ns
	Cycle to cycle jitter			$f_{(CPU)} = 100\text{ or }133\text{ MHz}$			300	ps
	Duty cycle			$f_{(PCI)} = 33\text{ MHz}$	45		55	%
$t_{sk(o)}$	PC1x bus skew	PC1x	PC1x	$f_{(PCI)} = 33\text{ MHz}$		70	300	ps
$t_{sk(p)}$	PC1x pulse skew	PCIn	PCIn	$f_{(PCI)} = 33\text{ MHz}$			4	ns
$t_{(off)}$	PC1x clock to 3V66 clock offset				-1.2		-3	ns
t_{w1}	Pulse duration width, high			$f_{(PCI)} = 33\text{ MHz}$	12			ns
t_{w2}	Pulse duration width, low			$f_{(PCI)} = 33\text{ MHz}$	12			ns
t_r	Rise time			$V_O = 0.4\text{ V to }2\text{ V}$	0.5	1.6	2	ns
t_f	Fall time			$V_O = 0.4\text{ V to }2\text{ V}$	0.5	1.5	2	ns

[†] The average over any 1- μs period of time is greater than the minimum specified period.

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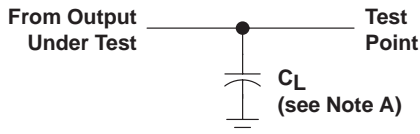
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PARAMETER MEASUREMENT INFORMATION

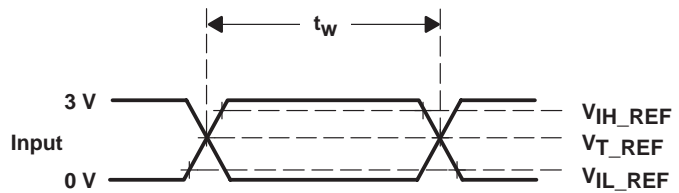


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{O_REF}
t_{PHZ}/t_{PZH}	GND

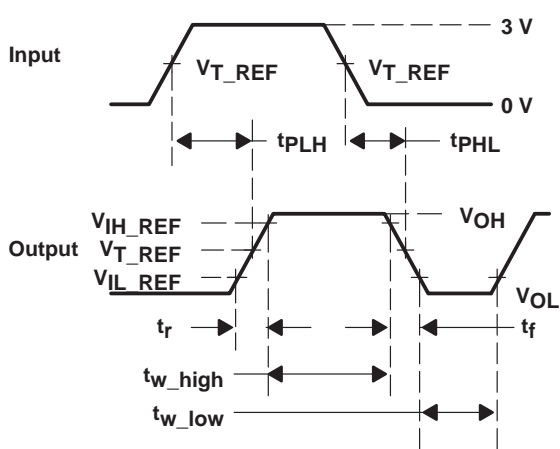
LOAD CIRCUIT for t_{pd} and t_{sk}



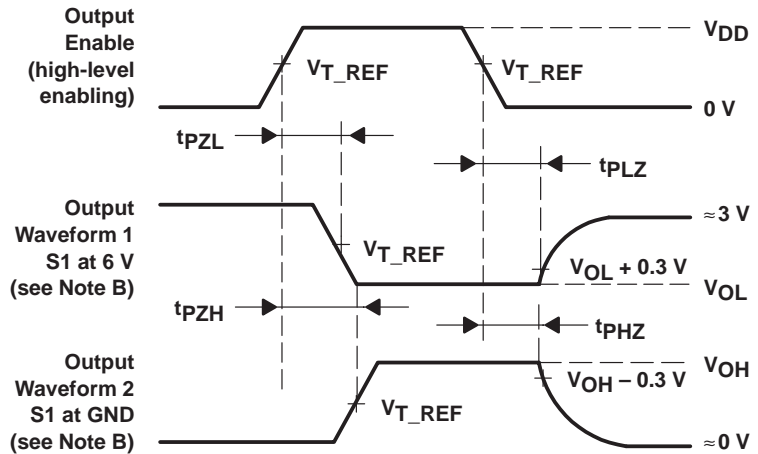
LOAD CIRCUIT FOR t_r and t_f



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance. $C_L = 20$ pF (CPUx, APICx, 48MHz, REF), $C_L = 30$ pF (PC1x, 3V66)
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 14.318$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

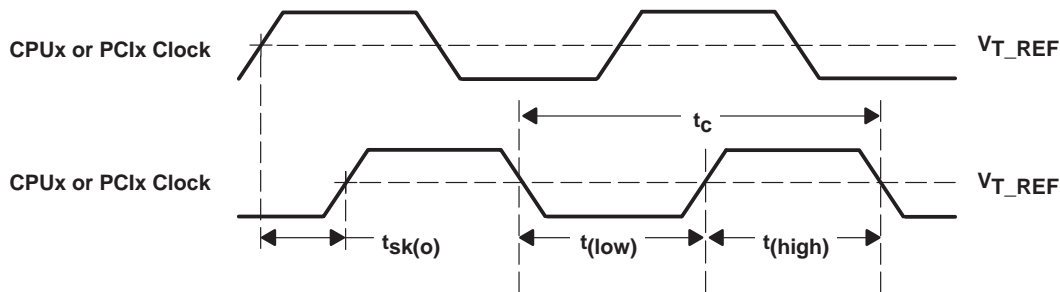
PARAMETER		3.3-V INTERFACE	2.5-V INTERFACE	UNIT
V_{IH_REF}	High-level reference voltage	2.4	2	V
V_{IL_REF}	Low-level reference voltage	0.4	0.4	V
V_{T_REF}	Input Threshold reference voltage	1.5	1.25	V
V_{O_REF}	Off-state reference voltage	6	4.6	V

Figure 3. Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION



$$t_{sk(p)} = |t_{PLH} - t_{PHL}|$$

$$\text{Duty Cycle} = \frac{t_{(low \text{ or } high)}}{t_c} \times 100$$

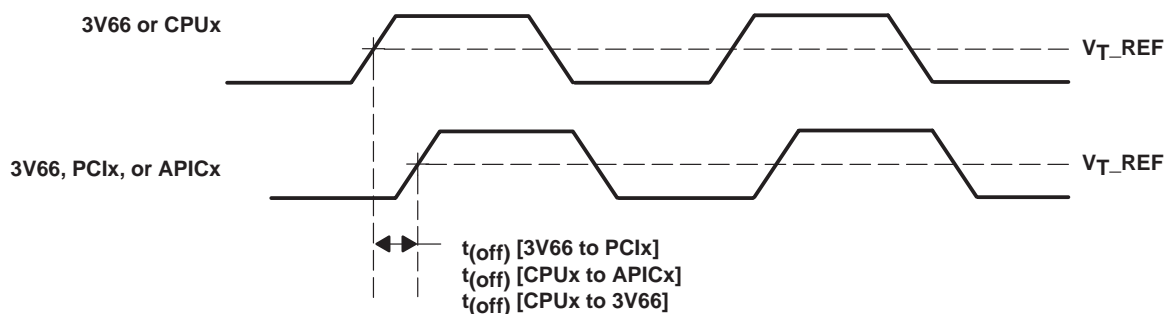


Figure 4. Waveforms for Calculation of Skew, Offset, and Jitter

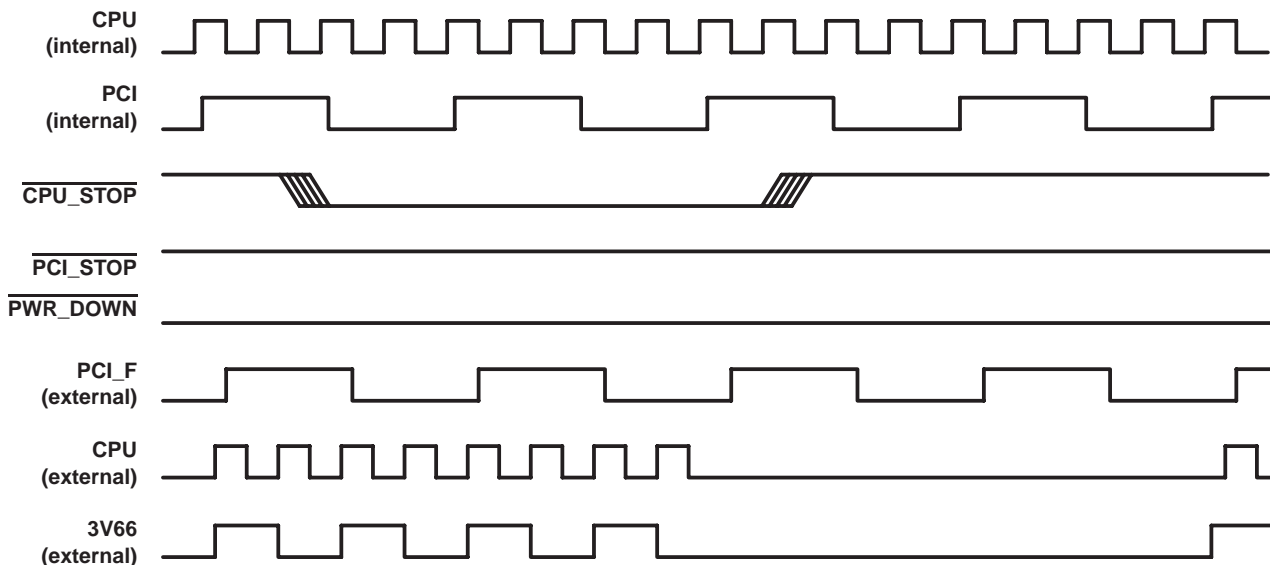


Figure 5. CPU_STOP Timing

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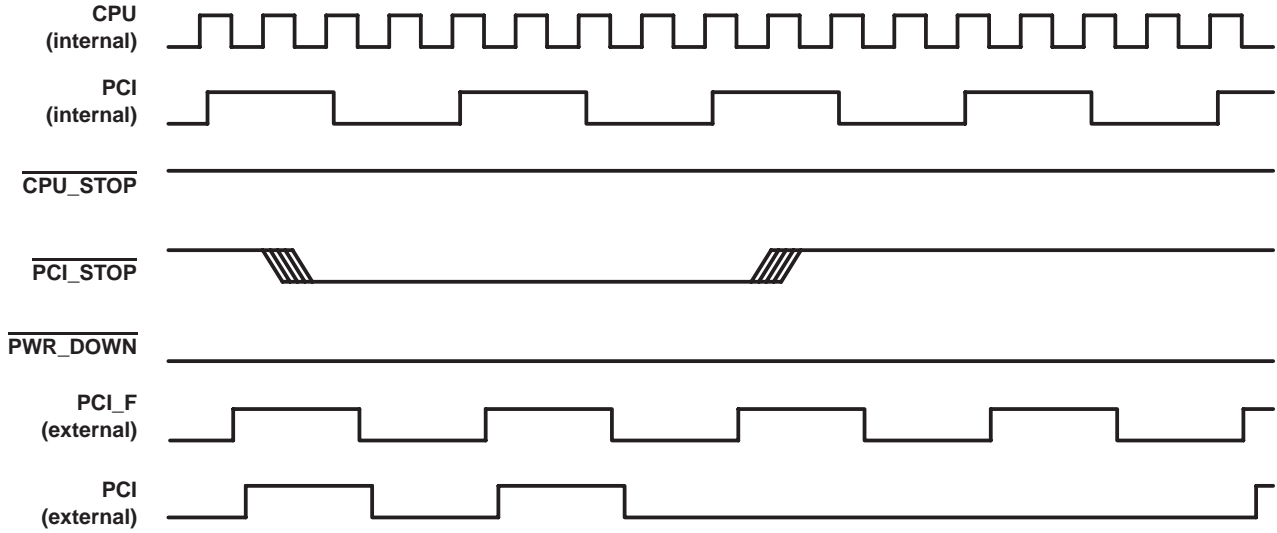
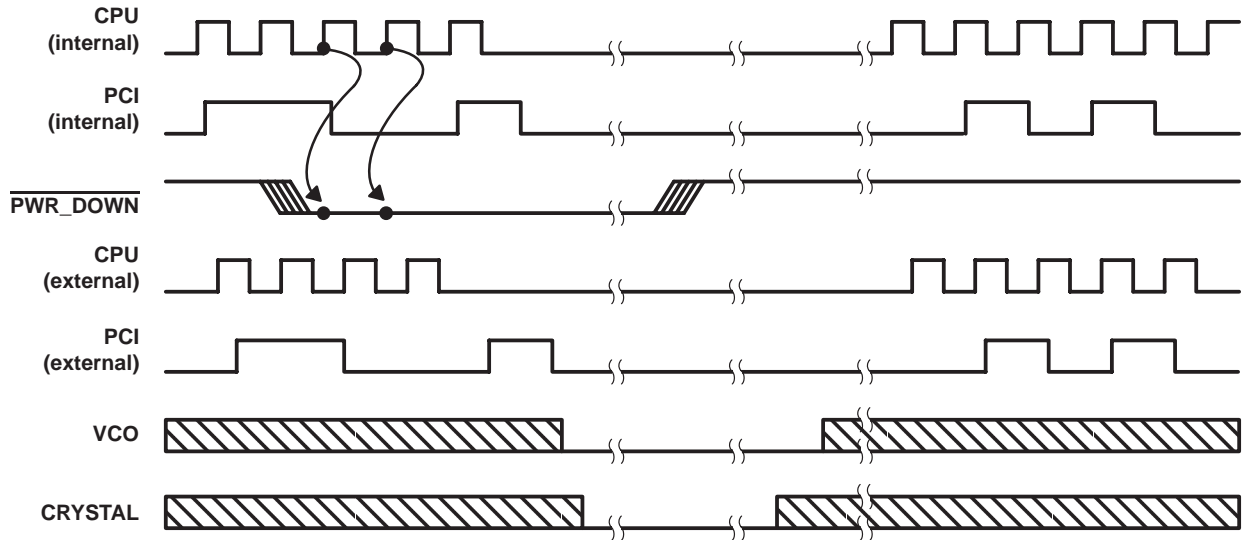


Figure 6. PCI_STOP Timing



NOTE A: Shaded sections on the VCO and Crystal waveforms indicate that the VCO and crystal oscillators are active and there is a valid clock.

Figure 7. Power-Down Timing

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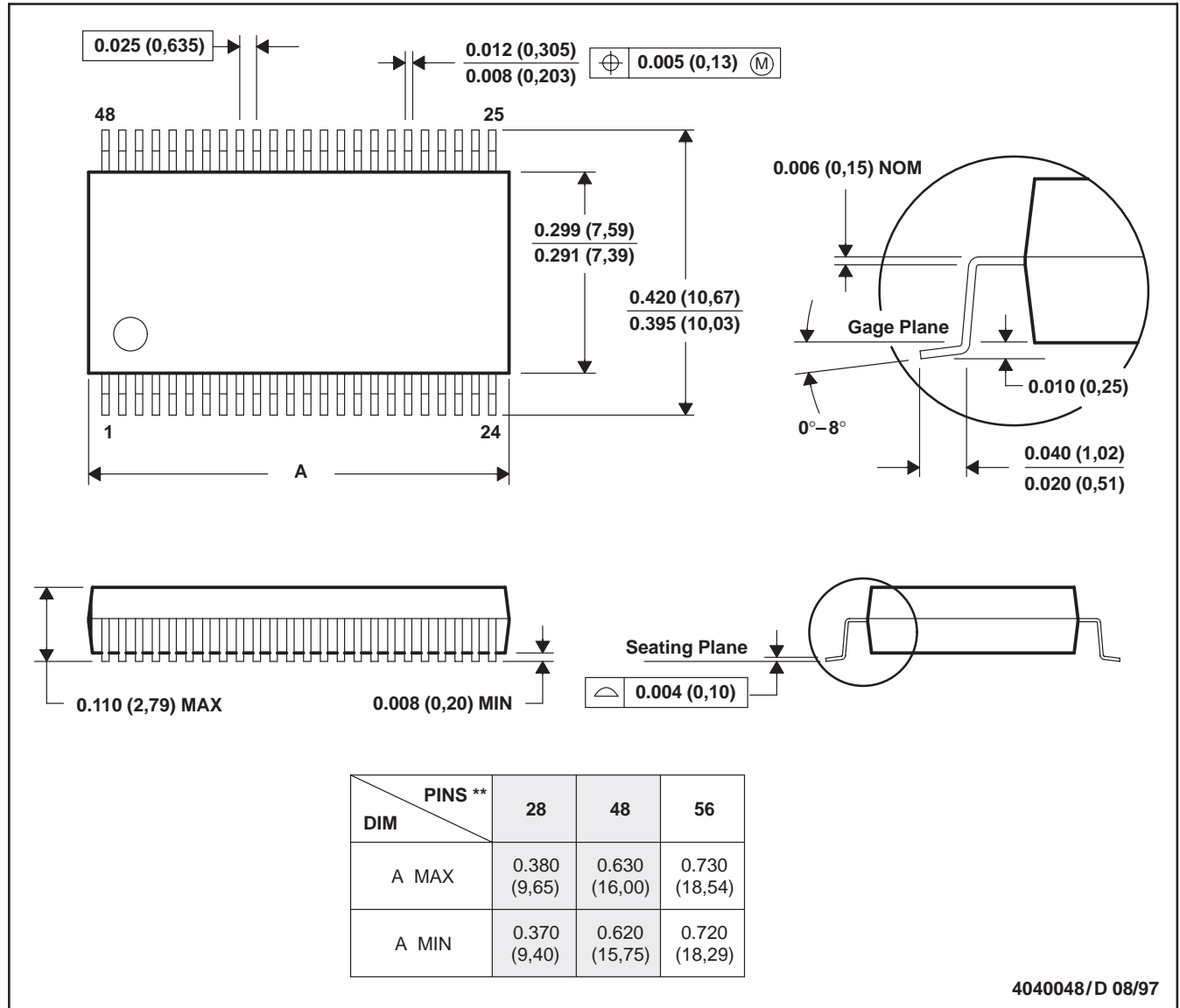
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MECHANICAL DATA

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48-PIN SHOWN



- NOTES: B. All linear dimensions are in inches (millimeters).
 C. This drawing is subject to change without notice.
 D. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 E. Falls within JEDEC MO-118

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