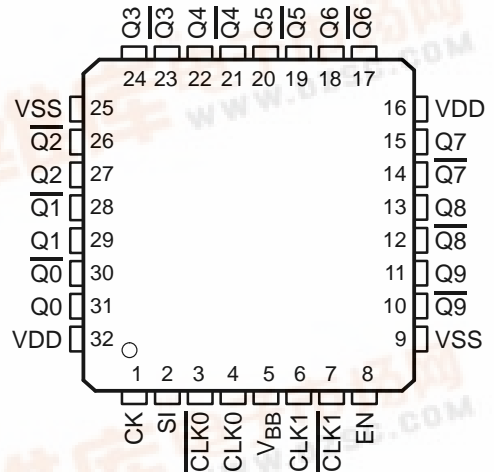


CDCLVD110 PROGRAMMABLE LOW-VOLTAGE 1:10 LVDS CLOCK DRIVER

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- **Low-Output Skew <30 ps (Typical) for Clock-Distribution applications**
- **Distributes One Differential Clock Input to 10 LVDS Differential Clock Outputs**
- **V_{CC} range 2.5 V ±5%**
- **Typical Signaling Rate Capability of Up to 1.1 GHz**
- **Configurable Register (SI/CK) Individually Enables Disables Outputs, Selectable CLK0, $\overline{\text{CLK0}}$ or CLK1, $\overline{\text{CLK1}}$ Inputs**
- **Full Rail-to-Rail Common-Mode Input Range**
- **Receiver Input Threshold ±100 mV**
- **Available in 32-Pin TQFP Package**
- **Fail-Safe I/O-Pins for V_{DD} = 0 V (Power Down)**

TQFP PACKAGE
(TOP VIEW)



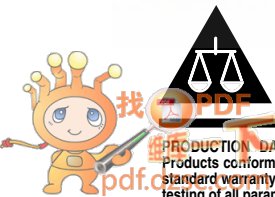
description

The CDCLVD110 clock driver distributes one pair of differential LVDS clock inputs (either CLK0 or CLK1) to 10 pairs of differential clock outputs (Q0, Q9) with minimum skew for clock distribution. The CDCLVD110 is specifically designed for driving 50-Ω transmission lines.

When the control enable is high (EN = 1), the 10 differential outputs are programmable in that each output can be individually enabled/disabled (3-stated) according to the first 10 bits loaded into the shift register. Once the shift register is loaded, the last bit selects either CLK0 or CLK1 as the clock input. However, when EN = 0, the outputs are not programmable and all outputs are enabled.

The CDCLVD110 is characterized for operation from -40°C to 85°C.

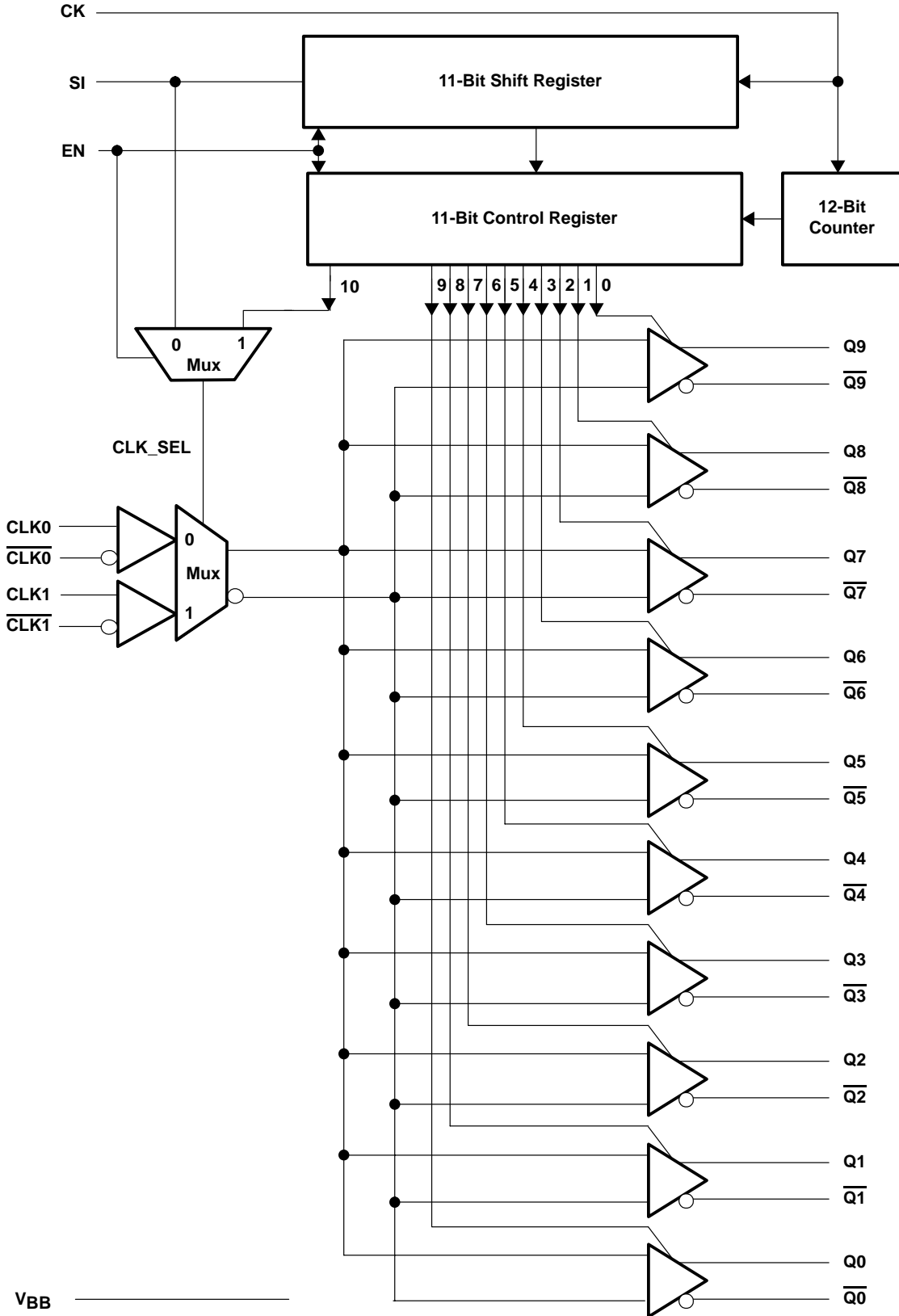
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functional block diagram



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Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|----------------------------|--|-----|---|
| CK | 1 | I | Control register input clock, features a 120-kΩ pullup resistor |
| SI | 2 | I | Control register serial input/CLK Select, features a 120-kΩ pulldown resistor |
| $\overline{\text{CLK0}}$ | 3 | I | Complementary differential input, LVDS |
| CLK0 | 4 | I | True differential input, LVDS |
| V _{BB} | 5 | O | Reference voltage output |
| CLK1 | 6 | I | Complementary differential input, LVDS |
| $\overline{\text{CLK1}}$ | 7 | I | True differential input, LVDS |
| EN | 8 | I | Control enable (for programmability), features a 120-kΩ pulldown resistor, input |
| V _{SS} | 9, 25 | | Device ground |
| V _{DD} | 16, 32 | | Supply voltage |
| Q [9:0] | 11, 13, 15, 18, 20, 22, 24, 27, 29, 31 | O | Clock outputs, these outputs provide low-skew copies of CLKIN |
| $\overline{\text{Q}}[9:0]$ | 10, 12, 14, 17, 19, 21, 23, 26, 28, 30 | O | Complementary clock outputs, these outputs provide low-skew copies of $\overline{\text{CLKIN}}$ |

absolute maximum ratings†

| | |
|---|-----------------------------------|
| Supply voltage, V _{DD} | –0.3 V to 2.8 V |
| Input voltage, V _I | –0.2 V to (V _{DD} + 0.2) |
| Output voltage, V _O | –0.2 V to (V _{DD} + 0.2) |
| Driver short circuit current, Q _n , $\overline{\text{Q}}_n$, I _{OSD} | Continuous |
| Electrostatic discharge (HBM 1.5 kΩ, 100 pF), ESD | >2000 V |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|---------------------|-----|---------------------------------------|------|
| Supply voltage, V _{DD} | 2.375 | 2.5 | 2.625 | V |
| Receiver common-mode input voltage, V _{IC} | 0.5 V _{ID} | | V _{DD} – 0.5 V _{ID} | V |
| Operating free-air temperature, T _A | –40 | | 85 | °C |

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driver electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|----------------------------------|--|------|------|------|------|
| V _{OD} | Differential output voltage | R _L = 100 Ω | 250 | 450 | 600 | mV |
| ΔV _{OD} | V _{OD} magnitude change | | | | 50 | mV |
| V _{OS} | Offset voltage | –40°C to 85°C | 0.95 | 1.2 | 1.45 | V |
| ΔV _{OS} | V _{OS} magnitude change | | | | 350 | mV |
| I _{OS} | Output short circuit current | V _O = 0 V | | | –20 | mA |
| | | V _{OD} = 0 V | | | 20 | |
| V _{BB} | Reference output voltage | V _{DD} = 2.5 V, I _{BB} = –100 μA | 1.15 | 1.25 | 1.35 | V |
| C _O | Output capacitance | V _O = V _{DD} or GND | | 3 | | pF |

receiver electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|---|------|-----|-----|------|
| V _{IDH} | Input threshold high | | | | 100 | mV |
| V _{IDL} | Input threshold low | | –100 | | | mV |
| V _{ID} | Input differential voltage | | 200 | | | mV |
| I _{IH} | Input current, CLK0/ $\overline{\text{CLK0}}$, CLK1/ $\overline{\text{CLK1}}$ | V _I = V _{DD} | –5 | | 5 | μA |
| I _{IL} | | V _I = 0 V | | | | |
| C _I | Input capacitance | V _I = V _{DD} or GND | | 3 | | pF |

supply current electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------|----------------|-----------------|--|-----|-----|-----|------|
| I _{DD} | Supply current | Full loaded | All outputs enabled and loaded, R _L = 100 Ω, f = 0 Hz | | | 130 | mA |
| | | No load | Outputs enabled, no output load, f = 0 Hz | | | 35 | |
| | | 3-State | All outputs 3-state by control logic, f = 0 Hz | | | 35 | |
| I _{DDZ} | | | | | | | |

LVDS—switching characteristics over recommended operating free-air temperature range, V_{DD} = 2.5 V ±5%

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | MIN | TYP | MAX | UNIT |
|---------------------|---|--|---|-----|------|-----|------|
| t _{PLH} | Propagation delay low-to-high | CLK0, $\overline{\text{CLK0}}$ CLK1, $\overline{\text{CLK1}}$ | Q _n , $\overline{\text{Qn}}$ | | 2 | 3 | ns |
| t _{PHL} | Propagation delay high-to-low | CLK0, $\overline{\text{CLK0}}$ CLK1, $\overline{\text{CLK1}}$ | Q _n , $\overline{\text{Qn}}$ | | 2 | 3 | ns |
| t _{duty} | Duty cycle | CLK0, $\overline{\text{CLK0}}$ CLK1, $\overline{\text{CLK1}}$ | Q _n , $\overline{\text{Qn}}$ | 45% | | 55% | |
| t _{sk(o)} | Output skew | | Any Q _n , $\overline{\text{Qn}}$ | | 30 | | ps |
| t _{sk(p)} | Pulse skew | | Any Q _n , $\overline{\text{Qn}}$ | | | 50 | ps |
| t _{sk(pp)} | Part-to-part skew | | Any Q _n , $\overline{\text{Qn}}$ | | | 600 | ps |
| t _r | Output rise time, 20% to 80%, R _L = 100 Ω, C _L = 5 pF | | Any Q _n , $\overline{\text{Qn}}$ | | | 350 | ps |
| t _f | Output fall time, 20% to 80%, R _L = 100 Ω, C _L = 5 pF | | Any Q _n , $\overline{\text{Qn}}$ | | | 350 | ps |
| f _{clk} | Max input frequency | CLK0, $\overline{\text{CLK0}}$ CLK1, $\overline{\text{CLK1}}$ | Any Q _n , $\overline{\text{Qn}}$ | 900 | 1100 | | MHz |

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**control register characteristics over recommended operating free-air temperature range,
 $V_{DD} = 2.5\text{ V} \pm 5\%$**

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------|-------------------------------------|-------------------------|-----|-----|-----|---------------|
| f_{MAX} | Maximum frequency of shift register | | 100 | 150 | | MHz |
| t_{su} | Setup time, clock to SI | | | | 2 | ns |
| t_h | Hold time, clock to SI | | | | 1.5 | ns |
| $t_{removal}$ | Removal time, enable to clock | | | | 1.5 | ns |
| t_w | Clock pulse width, minimum | | 3 | | | ns |
| V_{IH} | Logic input high | $V_{DD} = 2.5\text{ V}$ | 2 | | | V |
| V_{IL} | Logic input low | $V_{DD} = 2.5\text{ V}$ | | | 0.8 | V |
| I_{IH} | Input current, CK pin | $V_I = V_{DD}$ | -5 | | 5 | μA |
| | Input current, SI and EN pins | | 10 | | 30 | |
| I_{IL} | Input current, CK pin | $V_I = \text{GND}$ | -10 | | -30 | μA |
| | Input current, SI and EN pins | | -5 | | 5 | |

specification of control register

The CDCLVD110 is provided with an 11-bit, serial-in shift register and an 11-bit control register. The control Register enables/disables each output clock and selects either CLK0 or CLK1 as the input clock. The CDCLVD110 has two modes of operation:

Programmable Mode (EN=1)

The shift register utilizes a serial input (SI) and a clock input (CK). Once the shift register is loaded with 11 clock pulses, the twelfth clock pulse loads the control register. The first bit (bit 0) on SI enables the Q9, $\overline{Q9}$ output pair, and the tenth bit (bit 9) enables the Q0, $\overline{Q0}$ pair. The eleventh bit (bit 10) on SI selects either CLK0 or CLK1 as the input clock; a bit value of 0 selects CLK0, whereas a bit value of 1 selects CLK1. To restart the control register configuration, a reset of the state machine must be done with a clock pulse on CK (shift register clock input) and EN set to low. The control register can be configured only once after each reset.

Standard Mode (EN=0)

In this mode, the CDCLVD110 is not programmable and all the clock outputs are enabled. The clock input (CLK0 or CLK1) is selected with the SI pin, as is shown in the table entitled control register.

state-machine inputs

| EN | SI | CK | OUTPUT |
|----|----|----|--|
| L | L | X | All outputs enabled, CLK0 selected, control register disabled, default state |
| L | H | X | All outputs enabled, CLK1 selected, control register disabled |
| H | L | ↑ | First stage stores L, other stage stores data of previous stage |
| H | H | | First stage stores H, other stage stores data of previous stage |
| L | X | | Reset of state machine, shift and control registers |

control register

| BIT 10 | BITS [0-9] | $Q_N[0-9]$ |
|--------|------------|------------------|
| L | H | CLK0 |
| H | H | CLK1 |
| X | L | Outputs disabled |

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serial input (SI) sequence

| BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| CLK_SEL | Q0 | Q1 | Q2 | Q3 | Q4 | Q5 | Q6 | Q7 | Q8 | Q9 |

truth table for control logic

| CK | EN | SI | CLK0 | $\overline{\text{CLK0}}$ | CLK1 | $\overline{\text{CLK1}}$ | Q (0–9) | $\overline{\text{Q(0–9)}}$ | |
|---------------------|----|----------------|------|--------------------------|------|--------------------------|---------|----------------------------|--|
| L | L | L | L | H | X | X | L | H | |
| L | L | L | H | L | X | X | H | L | |
| L | L | L | Open | Open | X | X | L | H | |
| L | L | H | X | X | L | H | L | H | |
| L | L | H | X | X | H | L | H | L | |
| L | L | H | X | X | Open | Open | L | H | |
| All outputs enabled | | X = Don't care | | | | | | | |

APPLICATION INFORMATION

Fail-Safe information:

For $V_{DD} = 0$ V (power-down mode) the CDCLVD110 has fail-safe input and output pins. In power-on mode, fail-safe biasing at input pins can be accomplished with a 10-k Ω pullup resistor from CLK0/CLK1 to VDD and a 10-k Ω pulldown resistor from $\overline{\text{CLK0}}/\overline{\text{CLK1}}$ to GND.

LVDS Receiver Input termination:

The LVDS receiver inputs need to have 100- Ω termination resistors placed as close as possible across the input pins.

Control Inputs termination:

No external termination is required. The CK control input has an internal 120-k Ω pullup resistor while SI– and EN– control inputs each have an internal 120-k Ω pulldown resistor. If the control pins are left open per the default, all outputs are enabled, CLK0, $\overline{\text{CLK0}}$ is selected, and the control register is disabled.

PARAMETER MEASUREMENT INFORMATION

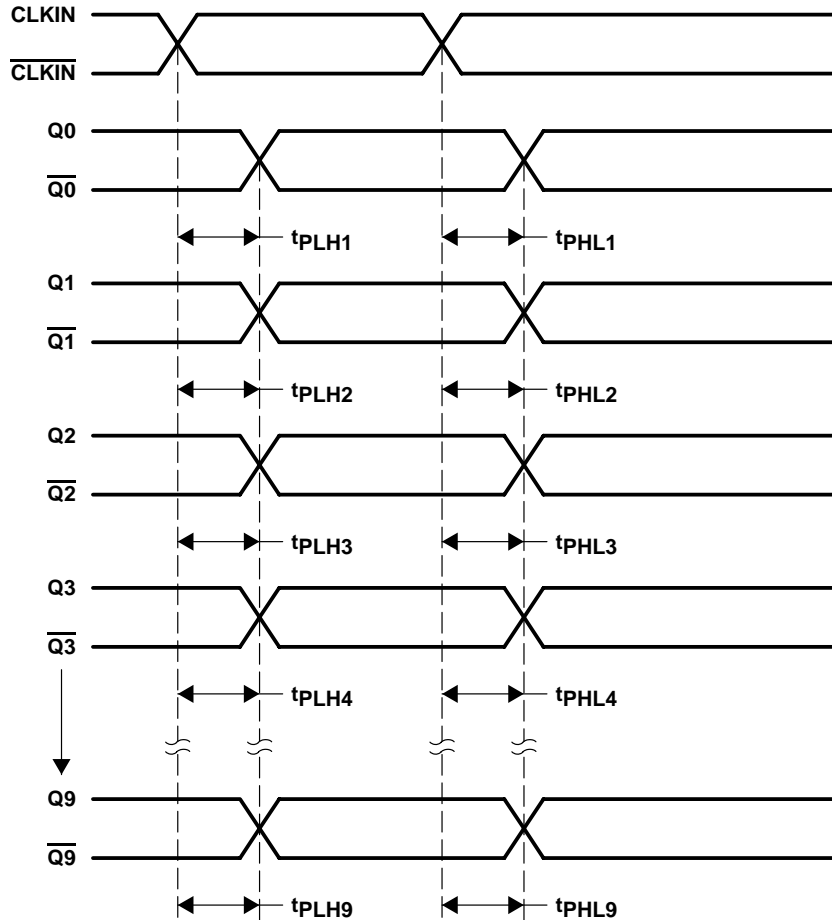


Figure 1. Waveforms for Calculation of $t_{sk(o)}$ and $t_{sk(pp)}$

- NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and the slowest t_{PLHn} ($n = 1, 2, \dots, 10$)
 - The difference between the fastest and the slowest t_{PHLn} ($n = 1, 2, \dots, 10$)
- B. Part-to-part skew, $t_{sk(pp)}$, is calculated as the greater of:
- The difference between the fastest and the slowest t_{PLHn} ($n = 1, 2, \dots, 10$) across multiple devices
 - The difference between the fastest and the slowest t_{PHLn} ($n = 1, 2, \dots, 10$) across multiple devices
- C. Pulse skew, $t_{sk(p)}$, is calculated as the magnitude of the absolute time difference between the high-to-low (t_{PHL}) and the low-to-high (t_{PLH}) propagation delays when a single switching input causes one or more outputs to switch, $t_{sk(p)} = |t_{PHL} - t_{PLH}|$. Pulse skew is sometimes referred to as pulse width distortion or duty cycle skew.

PARAMETER MEASUREMENT INFORMATION

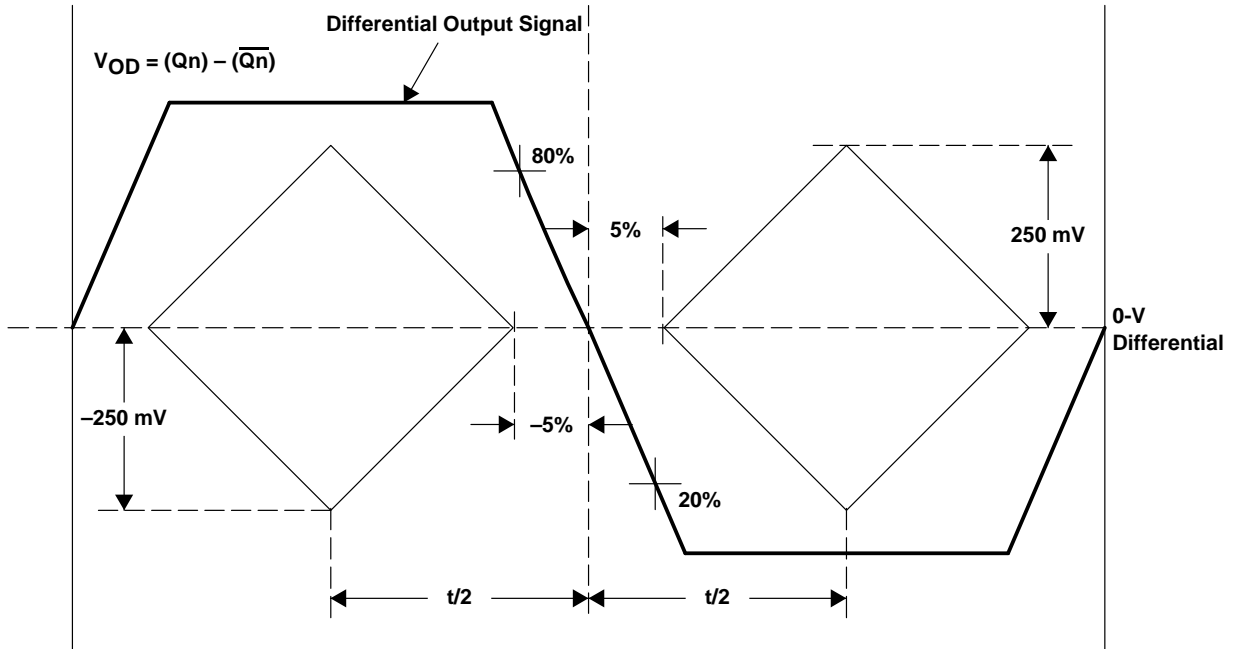


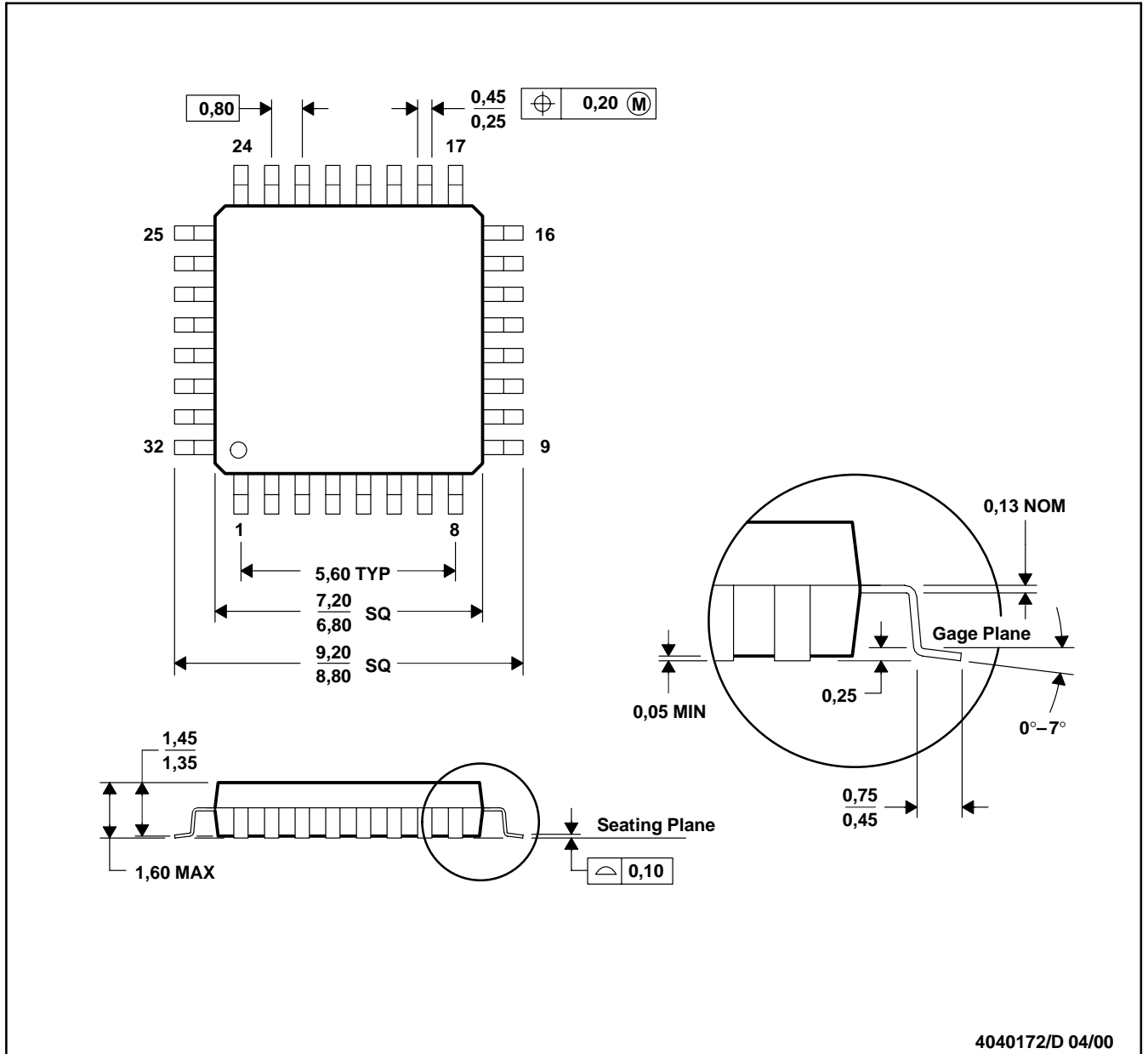
Figure 2. Test Criteria for f_{clk} , Duty Cycle, t_r , t_f , V_{OD}

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MECHANICAL DATA

VF (S-PQFP-G32)

PLASTIC QUAD FLATPACK



4040172/D 04/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265