

- Phase-Lock Loop Clock Driver for Double Data-Rate Synchronous DRAM Applications
- Spread Spectrum Clock Compatible
- Operating Frequency: 60 MHz to 200 MHz
- Low Jitter (cycle-cycle): ± 50 ps
- Low Static Phase Offset: ± 50 ps
- Low Jitter (Period): ± 35 ps
- Distributes One Differential Clock Input to 10 Differential Outputs
- Enters Low-Power Mode When No CLK Input Signal Is Applied or PWRDWN Is Low
- Operates From Dual 2.5-V Supplies
- Available in a 48-Pin TSSOP Package or 56-Ball MicroStar Junior™ BGA Package
- Consumes $< 100\text{-}\mu\text{A}$ Quiescent Current
- External Feedback Pins (FBIN, $\overline{\text{FBIN}}$) Are Used to Synchronize the Outputs to the Input Clocks
- Meets/Exceeds the Latest DDR JEDEC Spec JESD82-1

description

The CDCV857B is a high-performance, low-skew, low-jitter zero delay buffer that distributes a differential clock input pair (CLK, $\overline{\text{CLK}}$) to 10 differential pairs of clock outputs (Y[0:9], $\overline{\text{Y}}[0:9]$) and one differential pair of feedback clock outputs (FBOUR, $\overline{\text{FBOUR}}$). The clock outputs are controlled by the clock inputs (CLK, $\overline{\text{CLK}}$), the feedback clocks (FBIN, $\overline{\text{FBIN}}$), and the analog power input (AV_{DD}). When PWRDWN is high, the outputs switch in phase and frequency with CLK. When PWRDWN is low, all outputs are disabled to a high-impedance state (3-state) and the PLL is shut down (low-power mode). The device also enters this low-power mode when the input frequency falls below a suggested detection frequency that is below 20 MHz (typical 10 MHz). An input frequency detection circuit detects the low frequency condition and, after applying a $>20\text{-MHz}$ input signal, this detection circuit turns the PLL on and enables the outputs.

When AV_{DD} is strapped low, the PLL is turned off and bypassed for test purposes. The CDCV857B is also able to track spread spectrum clocking for reduced EMI.

Since the CDCV857B is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up. The CDCV857B is characterized for both commercial and industrial temperature ranges.

AVAILABLE OPTIONS

| T_A | TSSOP (DGG) | MicroStar Junior™ BGA (GQL) |
|---------------|-------------|-----------------------------|
| 0°C to 85°C | CDCV857BDGG | CDCV857BGQL |
| -40°C to 85°C | CDCV857BIGG | — |

FUNCTION TABLE (Select Functions)

| INPUTS | | | | OUTPUTS | | | | PLL |
|-------------------------|--------|-----------|-------------------------|---------|----------------------------|-------|---------------------------|--------------|
| AV_{DD} | PWRDWN | CLK | $\overline{\text{CLK}}$ | Y[0:9] | $\overline{\text{Y}}[0:9]$ | FBOUR | $\overline{\text{FBOUR}}$ | |
| GND | H | L | H | L | H | L | H | Bypassed/Off |
| GND | H | H | L | H | L | H | L | Bypassed/Off |
| X | L | L | H | Z | Z | Z | Z | Off |
| X | L | H | L | Z | Z | Z | Z | Off |
| 2.5 V (nom) | H | L | H | L | H | L | H | On |
| 2.5 V (nom) | H | H | L | H | L | H | L | On |
| 2.5 V (nom) | X | <20 MHz | <20 MHz | Z | Z | Z | Z | Off |

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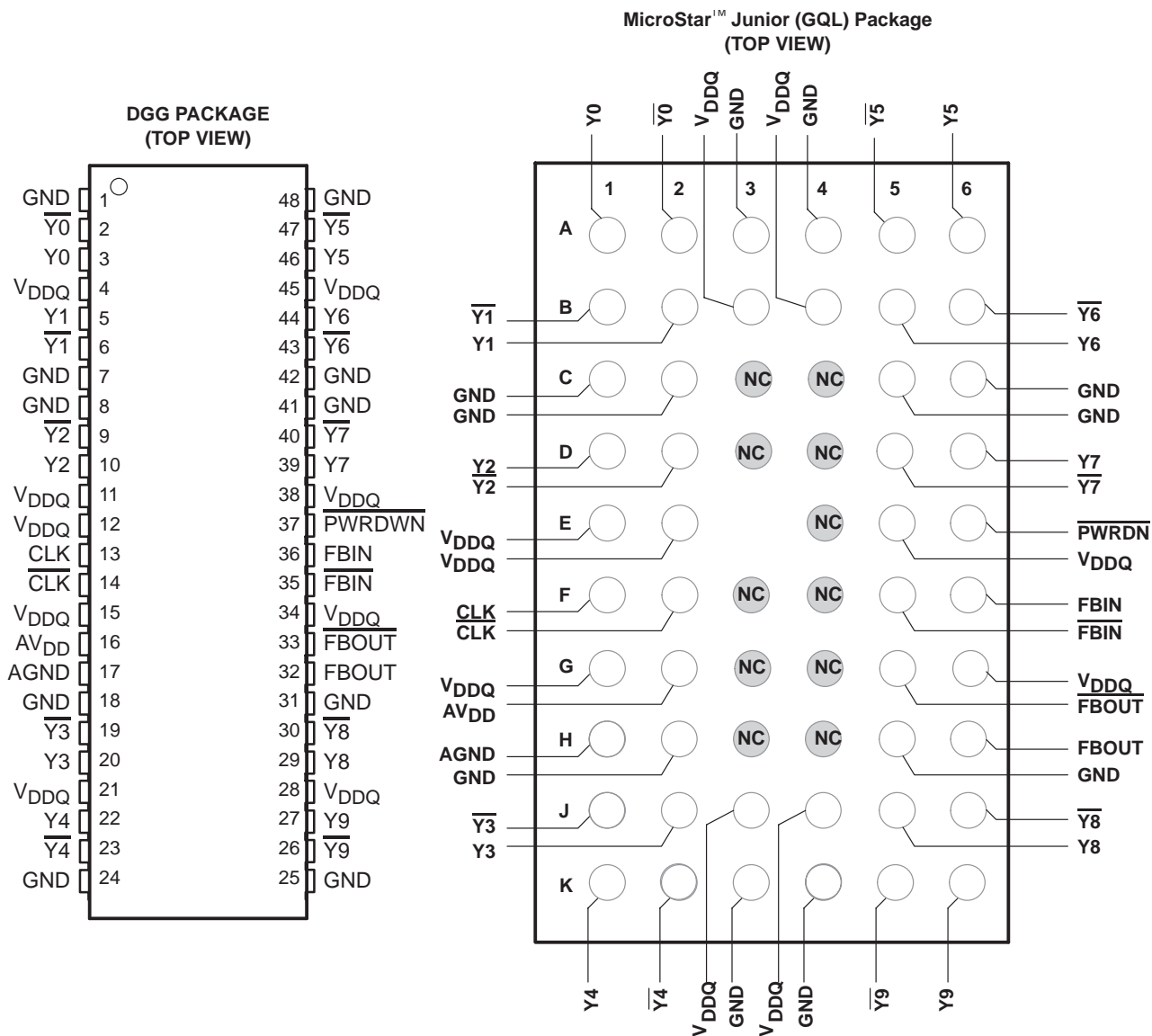
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



CDCV857B, CDCV857BI

2.5-V PHASE-LOCK LOOP CLOCK DRIVER

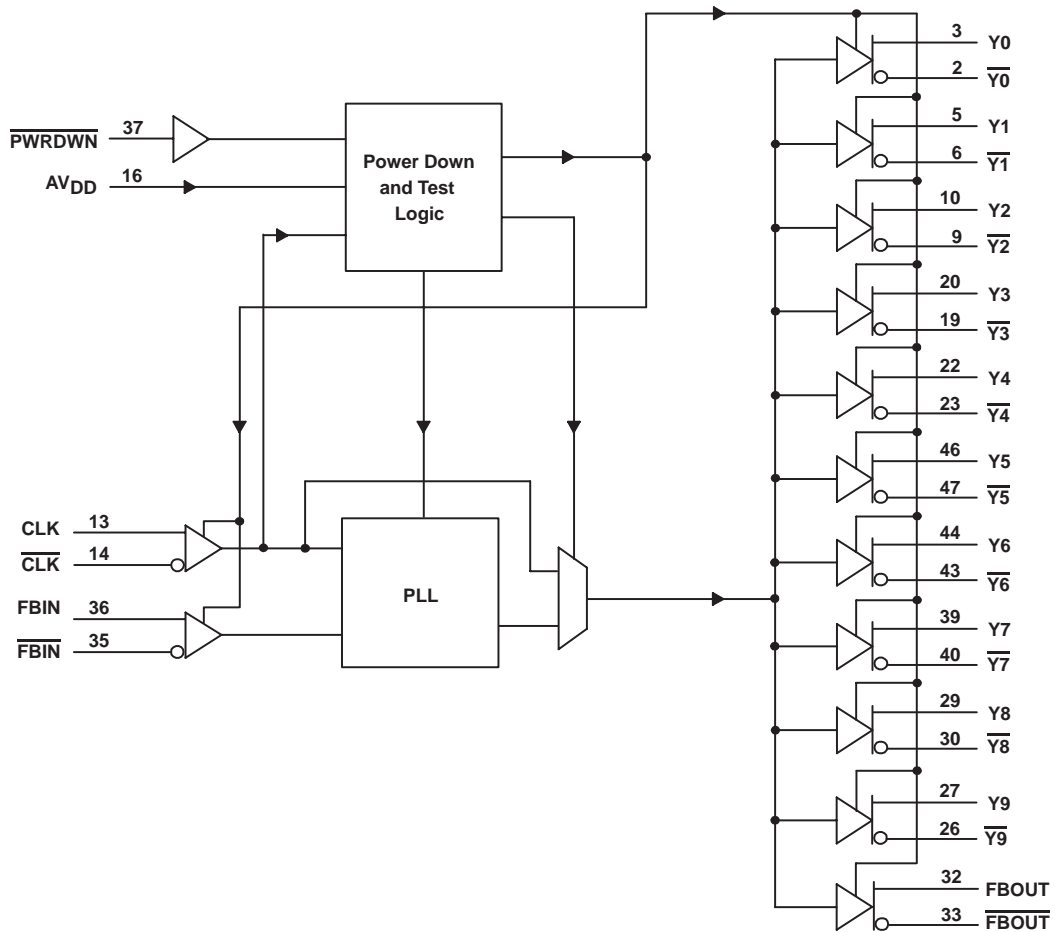
SCAS689 – FEBRUARY 2003



CDCV857B, CDCV857BI 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS689 – FEBRUARY 2003

functional block diagram



CDCV857B, CDCV857BI

2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS689 – FEBRUARY 2003

Terminal Functions

| TERMINAL | | | | DESCRIPTION |
|--------------------------------|---|--|---|--|
| NAME | DGG | GQL | | |
| AGND | 17 | H1 | | Ground for 2.5-V analog supply |
| AVDD | 16 | G2 | | 2.5-V Analog supply |
| CLK, $\overline{\text{CLK}}$ | 13, 14 | F1, F2 | I | Differential clock input |
| FBIN, FBIN | 35, 36 | F5, F6 | I | Feedback differential clock input |
| FBOU, $\overline{\text{FBOU}}$ | 32, 33 | H6, G5 | O | Feedback differential clock output |
| GND | 1, 7, 8, 18, 24, 25, 31, 41, 42, 48 | A3, A4, C1, C2, C5, C6, H2, H5, K3, K4 | | Ground |
| $\overline{\text{PWRDWN}}$ | 37 | E6 | I | Output enable for Y and $\overline{\text{Y}}$ |
| VDDQ | 4, 11, 12, 15, 21, 28, 34, 38, 45 | B3, B4, E1, E2, E5, G1, G6, J3, J4 | | 2.5-V Supply |
| Y[0:9] | 3, 5, 10, 20, 22, 27, 29, 39, 44, 46 | A1, B2, D1, J2, K1, A6, B5, D6, J5, K6 | O | Buffered output copies of input clock, CLK |
| $\overline{\text{Y}}[0:9]$ | 2, 6, 9, 19, 23, 26, 30, 40, 43, 47 | A2, B1, D2, J1, K2, A5, B6, D5, J6, K5 | O | Buffered output copies of input clock, $\overline{\text{CLK}}$ |

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

| | |
|--|------------------------|
| Supply voltage range, VDDQ, AVDD | 0.5 V to 3.6 V |
| Input voltage range, VI (see Notes 1 and 2) | -0.5 V to VDDQ + 0.5 V |
| Output voltage range, VO (see Notes 1 and 2) | -0.5 V to VDDQ + 0.5 V |
| Input clamp current, I _{IK} (VI < 0 or VI > VDDQ) | ±50 mA |
| Output clamp current, I _{OK} (VO < 0 or VO > VDDQ) | ±50 mA |
| Continuous output current, IO (VO = 0 to VDDQ) | ±50 mA |
| Continuous current to GND or VDDQ | ±100 mA |
| Package thermal impedance, θ_{JA} (see Note 3): GQL package | 137.6°C/W |
| Storage temperature range T _{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
 2. This value is limited to 3.6 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

CDCV857B, CDCV857BI

2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS689 – FEBRUARY 2003

recommended operating conditions (see Note 4)

| | | | MIN | TYP | MAX | UNIT |
|---|------------------------|-----------|----------------------------|-----|---------------------------|------|
| Supply voltage | V _{DDQ} | | 2.3 | | 2.7 | V |
| | AV _{DD} | | V _{DDQ} - 0.12 | | 2.7 | V |
| Low-level input voltage, V _{IL} | CLK, CLK̄, FBIN, FBIN̄ | | V _{DDQ} /2 - 0.18 | | | V |
| | PWRDWN | | -0.3 | | 0.7 | |
| High-level input voltage, V _{IH} | CLK, CLK̄, FBIN, FBIN̄ | | V _{DDQ} /2 + 0.18 | | | V |
| | PWRDWN | | 1.7 | | V _{DDQ} + 0.3 | |
| DC input signal voltage (see Note 5) | | | -0.3 | | V _{DDQ} + 0.3 | V |
| Differential input signal voltage, V _{ID} (see Note 6) | dc | CLK, FBIN | 0.36 | | V _{DDQ} + 0.6 | V |
| | ac | CLK, FBIN | 0.7 | | V _{DDQ} + 0.6 | |
| Input differential pair cross voltage, V _{IX} (see Note 7) | | | V _{DDQ} /2 - 0.2 | | V _{DDQ} /2 + 0.2 | V |
| High-level output current, I _{OH} | | | | | -12 | mA |
| Low-level output current, I _{OL} | | | | | 12 | mA |
| Input slew rate, SR | | | 1 | | 4 | V/ns |
| Operating free-air temperature, T _A | Commercial | | 0 | | 85 | °C |
| | Industrial | | -40 | | 85 | |

- NOTES:
- The unused inputs must be held high or low to prevent them from floating.
 - The dc input signal voltage specifies the allowable dc execution of the differential input.
 - The differential input signal voltage specifies the differential voltage |V_{TR} - V_{CP}| required for switching, where V_{TR} is the true input level and V_{CP} is the complementary input level.
 - The differential cross-point voltage is expected to track variations of V_{CC} and is the voltage at which the differential signals must be crossing.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|-------------------|---|------------|---|----------------------------|---------------------|----------------------------|------|
| V _{IK} | Input voltage | All inputs | V _{DDQ} = 2.3 V, I _I = -18 mA | | | -1.2 | V |
| V _{OH} | High-level output voltage | | V _{DDQ} = min to max, I _{OH} = -1 mA | V _{DDQ} - 0.1 | | | V |
| | | | V _{DDQ} = 2.3 V, I _{OH} = -12 mA | 1.7 | | | |
| V _{OL} | Low-level output voltage | | V _{DDQ} = min to max, I _{OL} = 1 mA | | | 0.1 | V |
| | | | V _{DDQ} = 2.3 V, I _{OL} = 12 mA | | | 0.6 | |
| V _{OD} | Output voltage swing [‡] | | Differential outputs are terminated with 120 Ω /CL = 14 pF (See Figure 3) | 1.1 | | V _{DDQ} - 0.4 | V |
| V _{OX} | Output differential cross-voltage [§] | | | V _{DDQ} /2 - 0.15 | V _{DDQ} /2 | V _{DDQ} /2 + 0.15 | |
| I _I | Input current | | V _{DDQ} = 2.7 V, V _I = 0 V to 2.7 V | | | ±10 | μA |
| I _{OZ} | High-impedance state output current | | V _{DDQ} = 2.7 V, V _O = V _{DDQ} or GND | | | ±10 | μA |
| I _{DDPD} | Power-down current on V _{DDQ} + AV _{DD} | | CLK and CLK̄ = 0 MHz; PWRDWN = Low; Σ of I _{DD} and AI _{DD} | | 20 | 100 | μA |
| AI _{DD} | Supply current on AV _{DD} | | f _O = 170 MHz | | 7 | 10 | mA |
| | | | f _O = 200 MHz | | 9 | 12 | |
| C _I | Input capacitance | | V _{DDQ} = 2.5 V, V _I = V _{DDQ} or GND | 2 | 2.5 | 3.5 | pF |

[†] All typical values are at a respective nominal V_{DDQ}.

[‡] The differential output signal voltage specifies the differential voltage |V_{TR} - V_{CP}|, where V_{TR} is the true output level and V_{CP} is the complementary output level.

[§] The differential cross-point voltage is expected to track variations of V_{DDQ} and is the voltage at which the differential signals must be crossing. The frequency range is 100 MHz to 200 MHz.

CDCV857B, CDCV857BI

2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS689 – FEBRUARY 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|-------------------|--|--|--------------------------|------|------|------|
| I _{DD} | Dynamic current on V _{DDQ} | Without load | f _O = 170 MHz | 100 | 110 | mA |
| | | | f _O = 200 MHz | 105 | 120 | |
| | | Differential outputs terminated with 120 Ω/CL = 0 pF | f _O = 170 MHz | 200 | 240 | |
| | | | f _O = 200 MHz | 210 | 250 | |
| | | Differential outputs terminated with 120 Ω/CL = 14 pF | f _O = 170 MHz | 260 | 300 | |
| | | | f _O = 200 MHz | 280 | 320 | |
| ΔC | Part-to-part input capacitance variation | V _{DDQ} = 2.5 V, V _I = V _{DDQ} or GND | | | 1 | pF |
| C _{I(Δ)} | Input capacitance difference between CLK and CLKB, FBIN, and FBINB | V _{DDQ} = 2.5 V, V _I = V _{DDQ} or GND | | | 0.25 | pF |
| C _O | Output capacitance | V _{DDQ} = 2.5 V, V _O = V _{DDQ} or GND | 2.5 | 3 | 3.5 | pF |

† All typical values are at a respective nominal V_{DDQ}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

| | | MIN | MAX | UNIT |
|-----------------------------------|-----------------------------|-----|-----|------|
| f _{CLK} | Operating clock frequency | 60 | 200 | MHz |
| | Application clock frequency | | | |
| Input clock duty cycle | | 40% | 60% | |
| Stabilization time† (PLL mode) | | | 10 | μs |
| Stabilization time‡ (Bypass mode) | | | 30 | ns |

† The time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK and V_{DD} must be applied. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

‡ A recovery time is required when the device goes from power-down mode into bypass mode (AVDD at GND).

switching characteristics

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|--|-----------------------------|------|-----|-----|------|
| t _{PLH} § | Low to high level propagation delay time | Test mode/CLK to any output | | 3.5 | | ns |
| t _{PHL} § | High-to low level propagation delay time | Test mode/CLK to any output | | 3.5 | | ns |
| t _{jit(per)} ¶ | Jitter (period), See Figure 7 | 66 MHz | -60 | | 60 | ps |
| | | 100/133/167/200 MHz | -35 | | 35 | ps |
| t _{jit(cc)} ¶ | Jitter (cycle-to-cycle), See Figure 4 | 66 MHz | -75 | | 75 | ps |
| | | 100/133/167/200 MHz | -50 | | 50 | |
| t _{jit(hper)} ¶ | Half-period jitter, See Figure 8 | 66 MHz | -100 | | 100 | ps |
| | | 100/133/167/200 MHz | -75 | | 75 | |
| t _{slr(o)} | Output clock slew rate, See Figure 9 | Load: 120 Ω/14 pF | 1 | | 2 | V/ns |
| t(∅) | Static phase offset, See Figure 5 | 66 MHz | -100 | | 100 | ps |
| | | 100/133/167/200 MHz | -50 | | 50 | |
| t _{sk(o)} | Output skew, See Figure 6 | Load: 120 Ω/14 pF | | 70 | 100 | ps |
| t _r , t _f | Output rise and fall times (20% – 80%) | Load: 120 Ω/14 pF | 600 | | 900 | ps |

§ Refers to the transition of the noninverting output.

¶ This parameter is assured by design but can not be 100% production tested.

PARAMETER MEASUREMENT INFORMATION

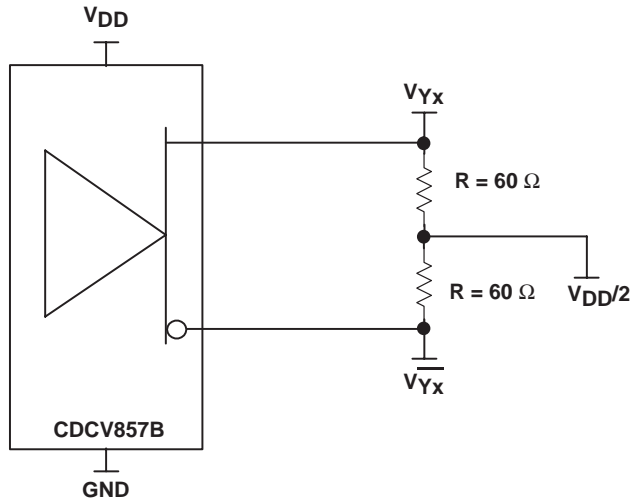


Figure 1. IBIS Model Output Load

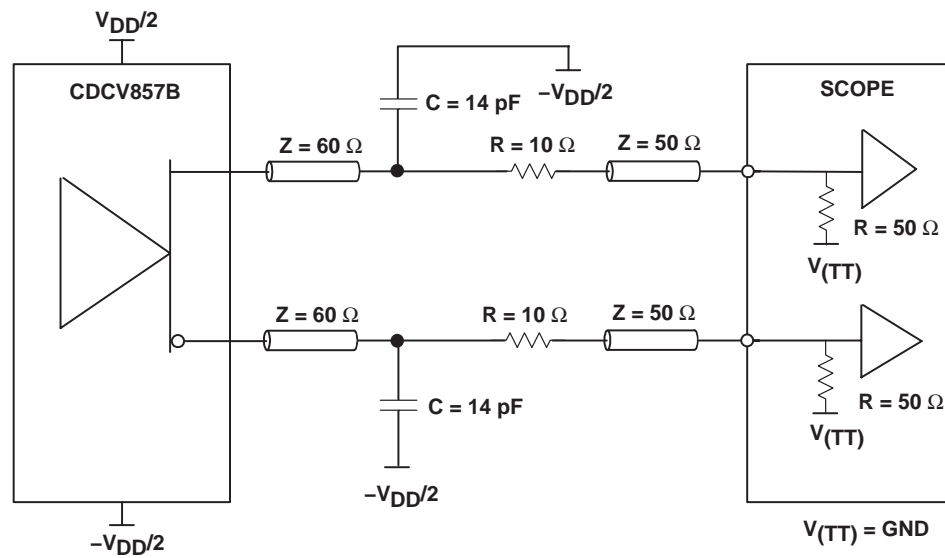


Figure 2. Output Load Test Circuit

CDCV857B, CDCV857BI

2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS689 – FEBRUARY 2003

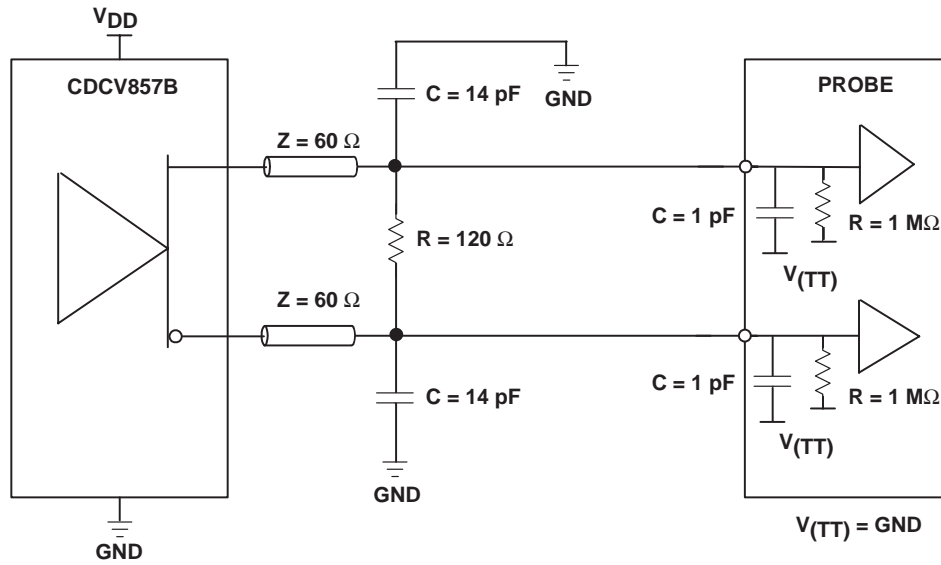


Figure 3. Output Load Test Circuit for Crossing Point

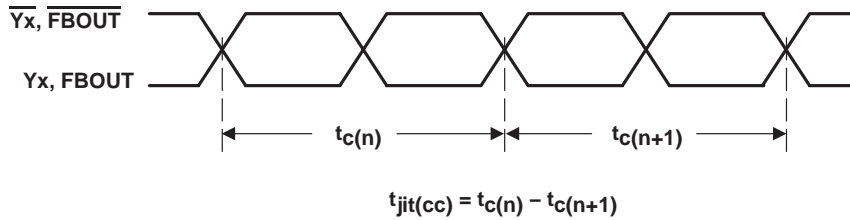


Figure 4. Cycle-to-Cycle Jitter

PARAMETER MEASUREMENT INFORMATION

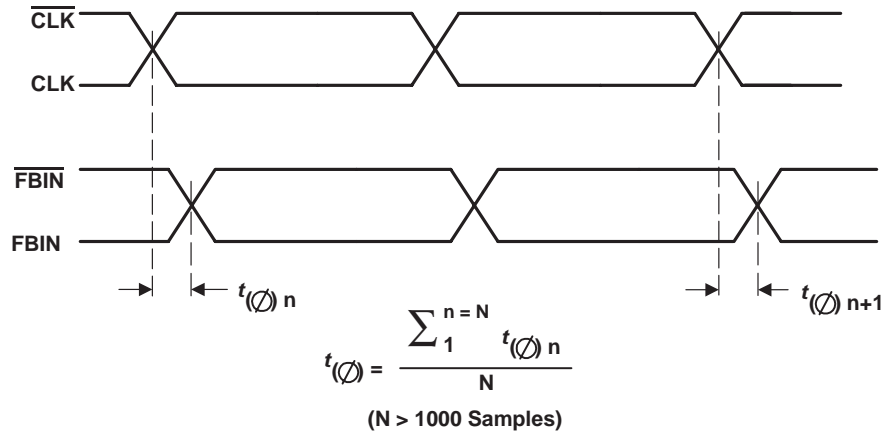


Figure 5. Phase Offset

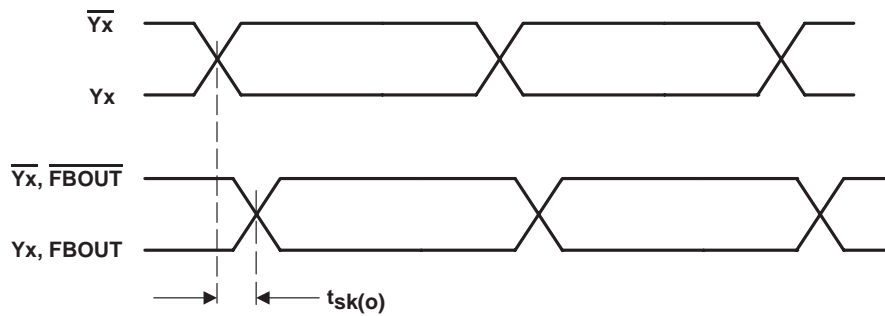


Figure 6. Output Skew

CDCV857B, CDCV857BI

2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS689 – FEBRUARY 2003

PARAMETER MEASUREMENT INFORMATION

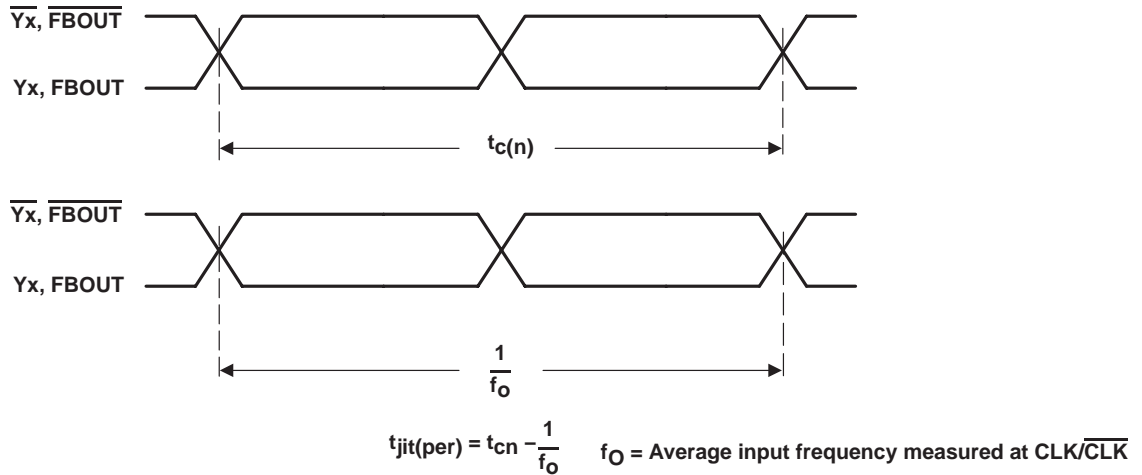


Figure 7. Period Jitter

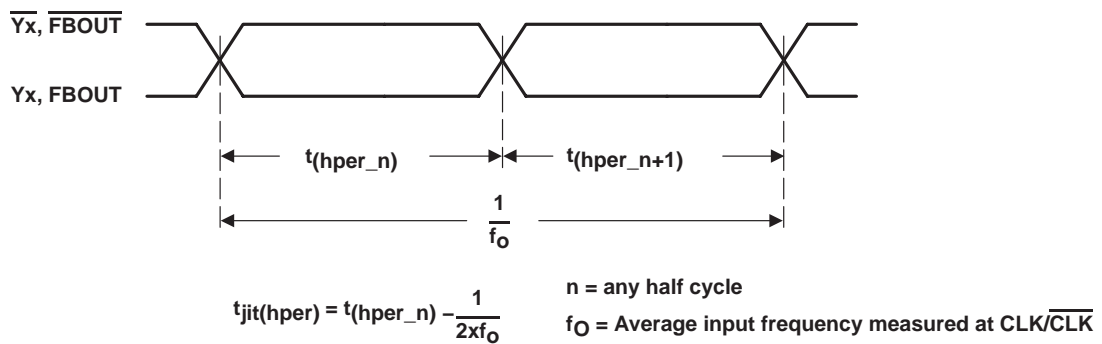


Figure 8. Half-Period Jitter

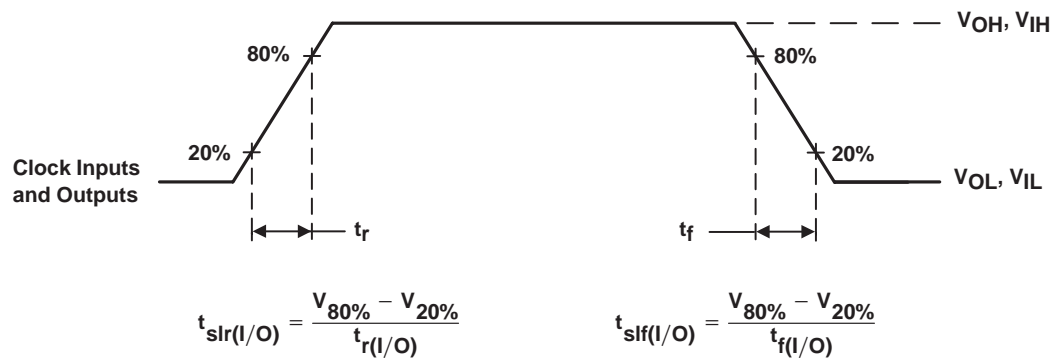


Figure 9. Input and Output Slew Rates

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CDCV857BDGGR | ACTIVE | TSSOP | DGG | 48 | 40 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| CDCV857BDGGR | ACTIVE | TSSOP | DGG | 48 | 2000 | None | Call TI | Call TI |
| CDCV857BGQLR | ACTIVE | VFBGA | GQL | 56 | 1000 | None | Call TI | Level-2A-220C-4 WKS |
| CDCV857BDGGR | ACTIVE | TSSOP | DGG | 48 | 40 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| CDCV857BDGGR | ACTIVE | TSSOP | DGG | 48 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

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Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

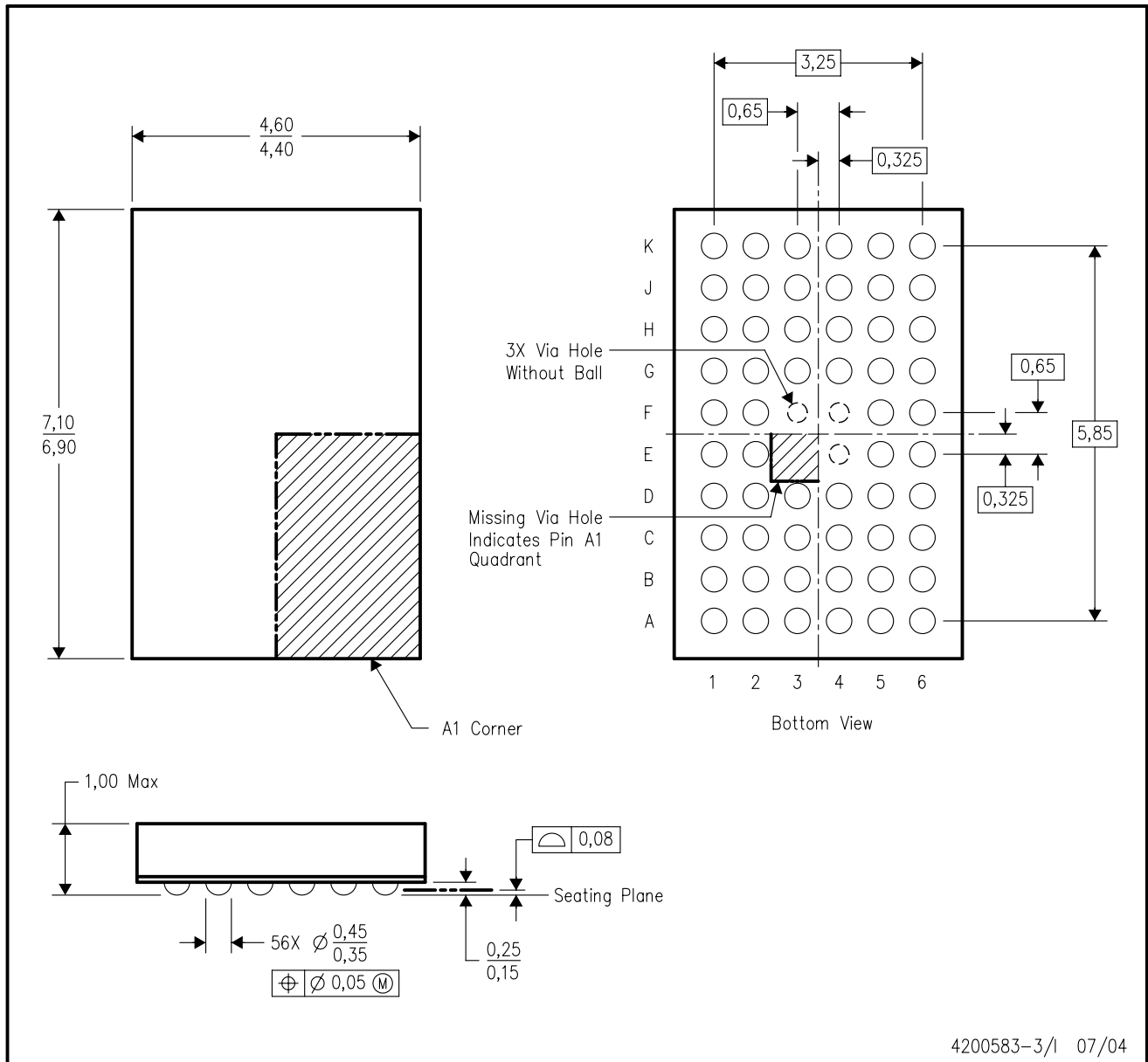
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MECHANICAL DATA

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225 variation BA.
 - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

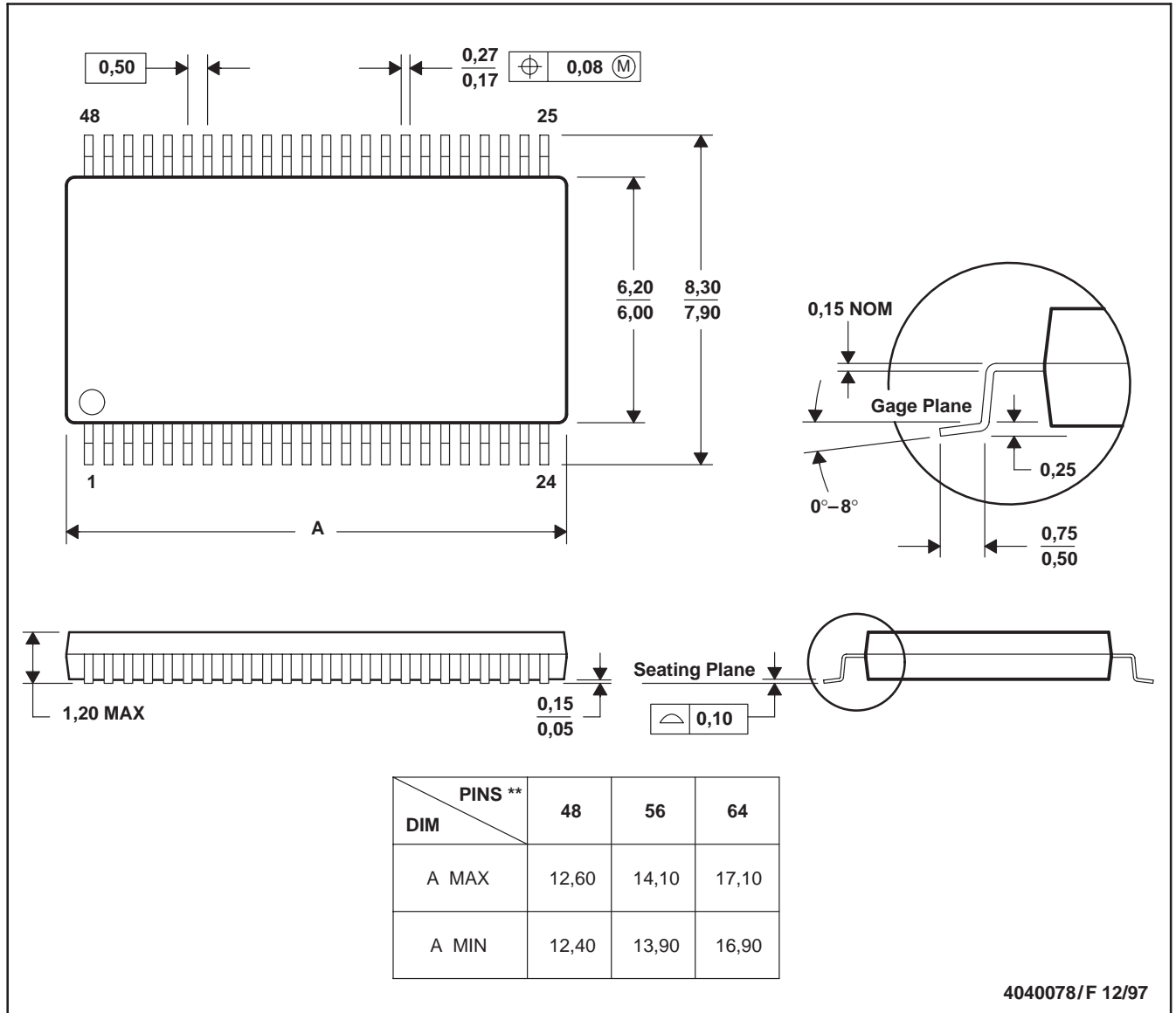
MECHANICAL DATA

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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