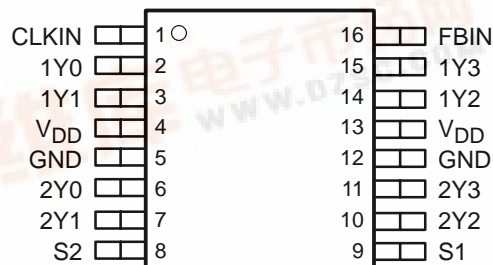


- **Phase-Locked Loop-Based Zero-Delay Buffer**
- **Operating Frequency: 8 MHz to 200 MHz**
- **Low Jitter (Cycle-Cycle):  $\pm 100$  ps Over the Range 66 MHz to 200 MHz**
- **Distributes One Clock Input to Two Banks of Four Outputs**
- **Auto Frequency Detection to Disable Device (Power Down Mode)**
- **Consumes Less Than 20  $\mu$ A in Power Down Mode**
- **Operates From Single 3.3-V Supply**
- **Industrial Temperature Range  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$**
- **25- $\Omega$  On-Chip Series Damping Resistors**
- **No External RC Network Required**
- **Spread Spectrum Clock Compatible (SSC)**
- **Available in 16-Pin TSSOP or 16-Pin SOIC Packages**

**D PACKAGE (SOIC)  
PW PACKAGE (TSSOP)  
(TOP VIEW)**



## description

The CDCVF25081 is a high-performance, low-skew, low-jitter, phase-lock loop clock driver. It uses a PLL to precisely align, in both frequency and phase, the output clocks to the input clock signal. The CDCVF25081 operates from a nominal supply voltage of 3.3 V. The device also includes integrated series-damping resistors in the output drivers that make it ideal for driving point-to-point loads.

Two banks of four outputs each provide low-skew, low-jitter copies of CLKIN. All outputs operate at the same frequency. Output duty cycles are adjusted to 50%, independent of duty cycle at CLKIN. The device automatically goes into power-down mode when no input signal is applied to CLKIN and the outputs go into a low state. Unlike many products containing PLLs, the CDCVF25081 does not require an external RC network. The loop filter for the PLL is included on-chip, minimizing component count, space, and cost.

Because it is based on a PLL circuitry, the CDCVF25081 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization is required following power up and application of a fixed-frequency signal at CLKIN and any following changes to the PLL reference.

The CDCVF25081 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**FUNCTION TABLE**

S2	S1	1Y0–1Y3	2Y0–2Y3	OUTPUT SOURCE	PLL SHUTDOWN
0	0	Hi-Z	Hi-Z	N/A.	Yes
0	1	Active	Hi-Z	PLL <sup>†</sup>	No
1	0	Active	Active	Input clock (PLL bypass)	Yes
1	1	Active	Active	PLL <sup>†</sup>	No

<sup>†</sup> CLK input frequency < 2 MHz switches the outputs to low level

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# CDCVF25081

## 3.3-V PHASED-LOCK LOOP CLOCK DRIVER

SCAS671A – OCTOBER 2001 – REVISED FEBRUARY 2003

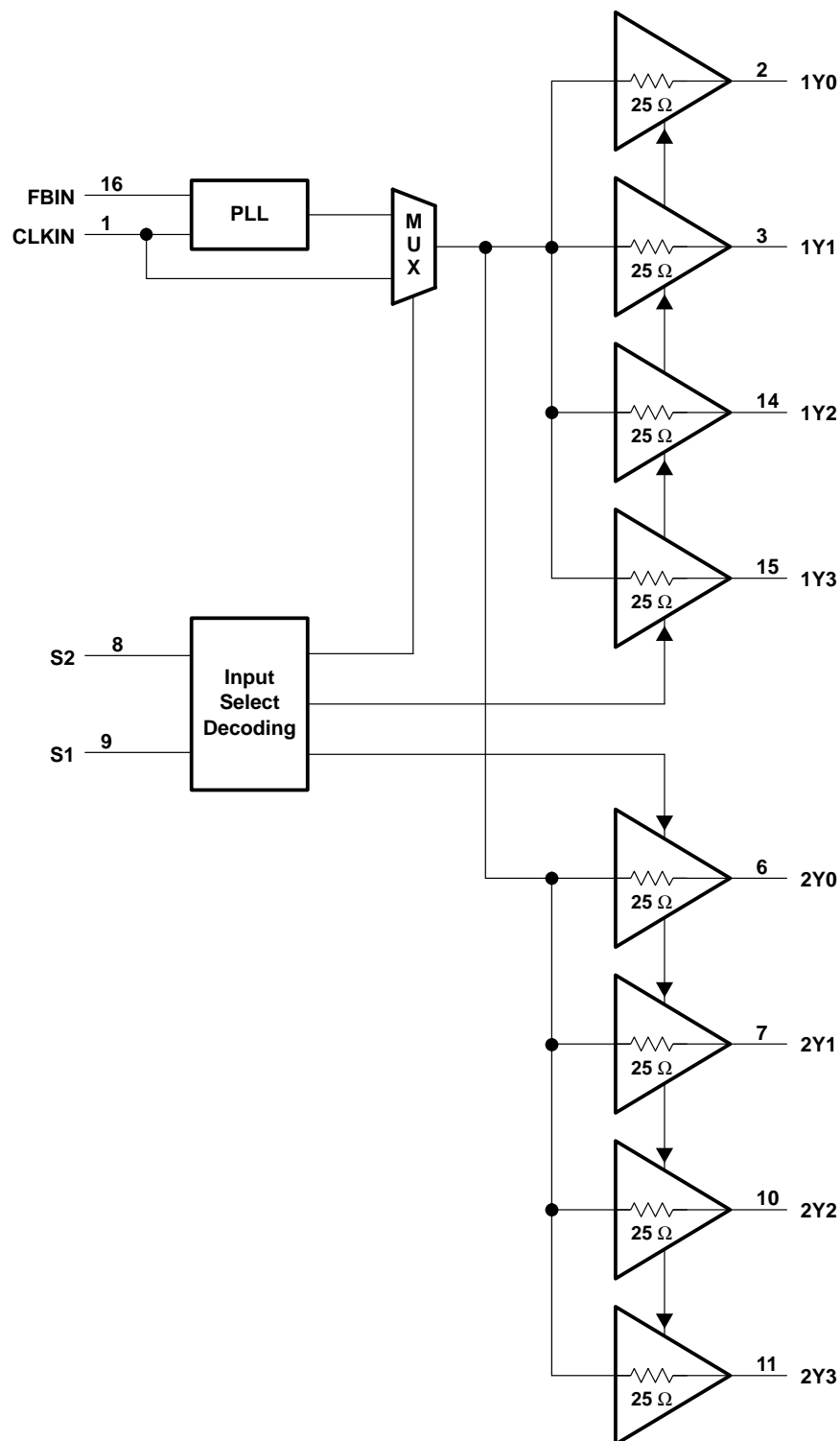
### Terminal Functions

TERMINAL		TYPE	DESCRIPTION
NAME	PIN NO.		
1Y[0:3]	2, 3, 14, 15	O	Bank 1Yn clock outputs. These outputs are low-skew copies of CLKIN. Each output has an integrated 25- $\Omega$ series-damping resistor.
2Y[0:3]	6, 7, 10, 11	O	Bank 2Yn clock outputs. These outputs are low-skew copies of CLKIN. Each output has an integrated 25- $\Omega$ series-damping resistor.
CLKIN	1	I	Clock input. CLKIN provides the clock signal to be distributed by the CDCVF25081 clock driver. CLKIN is used to provide the reference signal to the integrated PLL that generates the output signal. CLKIN must have a fixed frequency and phase in order for the PLL to acquire lock. Once the circuit is powered up and a valid signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to CLKIN.
FBIN	16	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be wired to one of the outputs to complete the feedback loop of the internal PLL. The integrated PLL synchronizes the FBIN and output signal so there is nominally zero-delay from input clock to output clock.
GND	5, 12	Ground	Ground
S1, S2	9, 8	I	Select pins to determine mode of operation. See the <i>FUNCTION TABLE</i> for mode selection options.
VDD	4, 13	Power	Supply voltage. The supply voltage range is 3 V to 3.6 V

CDCVF25081  
3.3-V PHASED-LOCK LOOP CLOCK DRIVER

SCAS671A – OCTOBER 2001 – REVISED FEBRUARY 2003

functional block diagram



# CDCVF25081

## 3.3-V PHASED-LOCK LOOP CLOCK DRIVER

SCAS671A – OCTOBER 2001 – REVISED FEBRUARY 2003

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{DD}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Notes 1 and 2)	–0.5 V to 4.6 V
Output voltage range, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{DD} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Continuous total output current, $I_O$ ( $V_O = 0$ to $V_{DD}$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): PW package	147°C/W
D package	112°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

3. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{DD}$	3	3.3	3.6	V
Low level input voltage, $V_{IL}$			0.8	V
High level input voltage, $V_{IH}$	2			V
Input voltage, $V_I$	0		3.6	V
High-level output current, $I_{OH}$			–12	mA
Low-level output current, $I_{OL}$			12	mA
Operating free-air temperature, $T_A$	–40		85	°C

### timing requirements over recommended ranges of supply voltage, load and operating free-air temperature

		MIN	NOM	MAX	UNIT
Clock frequency, $f_{clk}$	$C_L = 25$ pF	8		100	MHz
	$C_L = 15$ pF	66		200	

**CDCVF25081**  
**3.3-V PHASED-LOCK LOOP CLOCK DRIVER**

SCAS671A – OCTOBER 2001 – REVISED FEBRUARY 2003

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V <sub>IK</sub>	Input voltage	V <sub>DD</sub> = 3 V, I <sub>I</sub> = -18 mA			-1.2	V
I <sub>I</sub>	Input current	V <sub>I</sub> = 0 V or V <sub>DD</sub>			±5	μA
I <sub>PD</sub> ‡	Power down current	f <sub>CLKIN</sub> = 0 MHz, V <sub>DD</sub> = 3.3 V			20	μA
I <sub>OZ</sub>	Output 3-state	V <sub>O</sub> = 0 V or V <sub>DD</sub> , V <sub>DD</sub> = 3.6 V			±5	μA
C <sub>I</sub>	Input capacitance at FBIN, CLKIN	V <sub>I</sub> = 0 V or V <sub>DD</sub>		4		pF
C <sub>I</sub>	Input capacitance at S1, S2	V <sub>I</sub> = 0 V or V <sub>DD</sub>		2.2		pF
C <sub>O</sub>	Output capacitance	V <sub>I</sub> = 0 V or V <sub>DD</sub>		3		pF
V <sub>OH</sub>	High-level output voltage	V <sub>DD</sub> = min to max, I <sub>OH</sub> = -100 μA	V <sub>DD</sub> - 0.2			V
		V <sub>DD</sub> = 3 V, I <sub>OH</sub> = -12 mA	2.1			
		V <sub>DD</sub> = 3 V, I <sub>OH</sub> = -6 mA	2.4			
V <sub>OL</sub>	Low-level output voltage	V <sub>DD</sub> = min to max, I <sub>OL</sub> = 100 μA	0.2			V
		V <sub>DD</sub> = 3 V, I <sub>OL</sub> = 12 mA	0.8			
		V <sub>DD</sub> = 3 V, I <sub>OL</sub> = 6 mA	0.55			
I <sub>OH</sub>	High-level output current	V <sub>DD</sub> = 3 V, V <sub>O</sub> = 1 V	-24			mA
		V <sub>DD</sub> = 3.3 V, V <sub>O</sub> = 1.65 V	-30			
		V <sub>DD</sub> = 3.6 V, V <sub>O</sub> = 3.135 V	-15			
I <sub>OL</sub>	Low-level output current	V <sub>DD</sub> = 3 V, V <sub>O</sub> = 1.95 V	26			mA
		V <sub>DD</sub> = 3.3 V, V <sub>O</sub> = 1.65 V	33			
		V <sub>DD</sub> = 3.6 V, V <sub>O</sub> = 0.4 V	14			

† All typical values are at respective nominal V<sub>DD</sub>.

‡ For I<sub>DD</sub> over frequency see Figure 7.

# CDCVF25081

## 3.3-V PHASED-LOCK LOOP CLOCK DRIVER

SCAS671A – OCTOBER 2001 – REVISED FEBRUARY 2003

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted)**

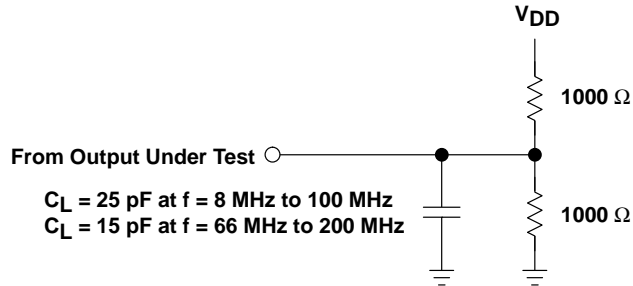
PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{\text{(lock)}}$ PLL lock time	$f = 100 \text{ MHz}$		10		$\mu\text{s}$
$t_{\text{(phoffset)}}$ Phase offset (CLKIN to FBIN)	$f = 8 \text{ MHz to } 66 \text{ MHz},$ $V_{\text{th}} = V_{\text{DD}}/2$ (see Note 5)	-200		200	ps
	$f = 66 \text{ MHz to } 200 \text{ MHz},$ $V_{\text{th}} = V_{\text{DD}}/2$ (see Note 5)	-150		150	
$t_{\text{PLH}}$ Low-to-high level output propagation delay	$S2 = \text{High},$ $S1 = \text{Low (PLL bypass)}$	2.5		6	ns
$t_{\text{PHL}}$ High-to-low level output propagation delay	$f = 1 \text{ MHz},$ $C_L = 25 \text{ pF}$				
$t_{\text{sk(o)}}$ Output skew ( $Y_n$ to $Y_n$ ) (see Note 4)				150	ps
$t_{\text{sk(pp)}}$ Part-to-part skew	$S2 = \text{high},$ $S1 = \text{high (PLL mode)}$			600	ps
	$S2 = \text{high},$ $S1 = \text{low (PLL bypass)}$			700	
$t_{\text{jit(cc)}}$ Jitter (cycle-to-cycle)	$f = 66 \text{ MHz to } 200 \text{ MHz}, C_L = 15 \text{ pF}$			$\pm 100$	ps
	$f = 66 \text{ MHz to } 100 \text{ MHz}, C_L = 25 \text{ pF}$			$\pm 150$	
	$f = 8 \text{ MHz to } 66 \text{ MHz (see Figure 6)}$			$\pm 150$	
odc Output duty cycle	$f = 8 \text{ MHz to } 200 \text{ MHz}$	43%		57%	
$t_{\text{sk(p)}}$ Pulse skew	$S2 = \text{High},$ $S1 = \text{low (PLL bypass)}$ $f = 1 \text{ MHz},$ $C_L = 25 \text{ pF}$			0.7	ns
$t_r$ Rise time rate	$C_L = 15 \text{ pF},$ See Figure 4	0.8		3.3	V/ns
	$C_L = 25 \text{ pF},$ See Figure 4	0.5		2	
$t_f$ Fall time rate	$C_L = 15 \text{ pF},$ See Figure 4	0.8		3.3	V/ns
	$C_L = 25 \text{ pF},$ See Figure 4	0.5		2	

† All typical values are at respective nominal  $V_{\text{DD}}$ .

NOTES: 4. The  $t_{\text{sk(o)}}$  specification is only valid for equal loading of all outputs.

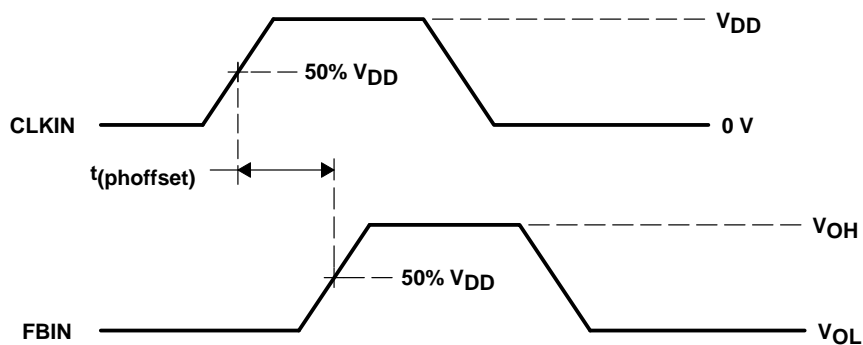
5. Similar waveform at CLKIN and FBIN are required. For phase displacement between CLKIN and Y-outputs see Figure 5.

### PARAMETER MEASUREMENT INFORMATION

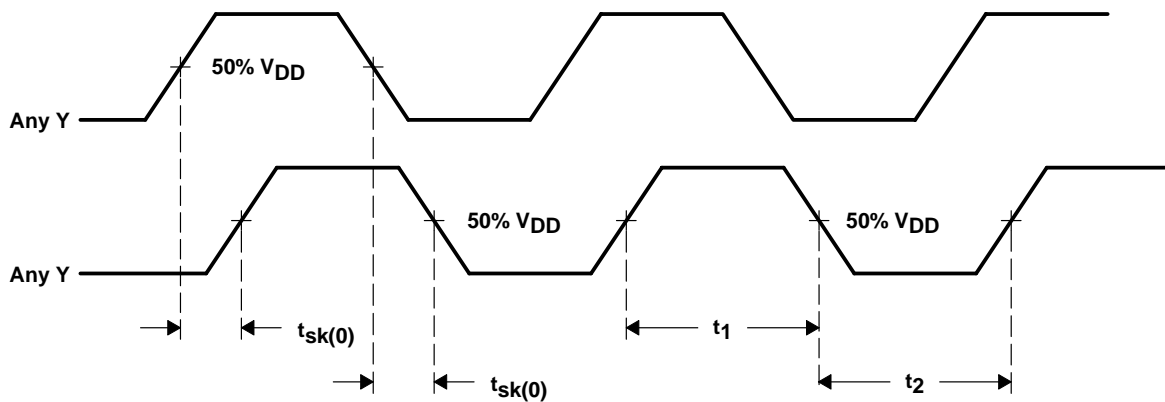


- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $Z_O = 50 \Omega$ ,  $t_r < 1.2 \text{ ns}$ ,  $t_f < 1.2 \text{ ns}$ .  
 C. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Test Load Circuit**



**Figure 2. Voltage Thresholds for Measurements, Phase Offset (PLL Mode)**



NOTE:  $odc = t_1 / (t_1 + t_2) \times 100\%$

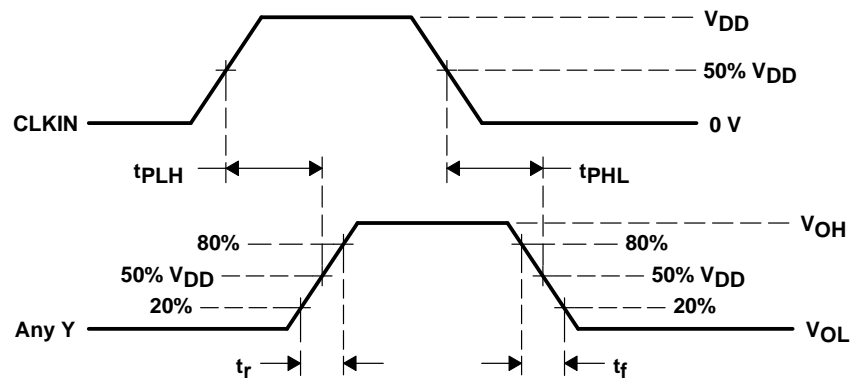
**Figure 3. Output Skew and Output Duty Cycle (PLL Mode)**

# CDCVF25081

## 3.3-V PHASED-LOCK LOOP CLOCK DRIVER

SCAS671A – OCTOBER 2001 – REVISED FEBRUARY 2003

### PARAMETER MEASUREMENT INFORMATION



NOTE:  $t_{sk(p)} = |t_{PLH} - t_{PHL}|$

Figure 4. Propagation Delay and Pulse Skew (Non-PLL Mode)

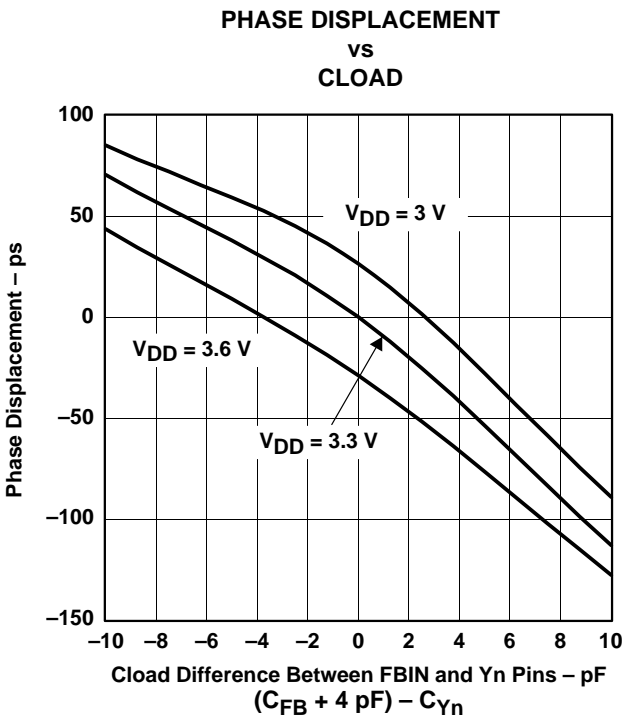


Figure 5

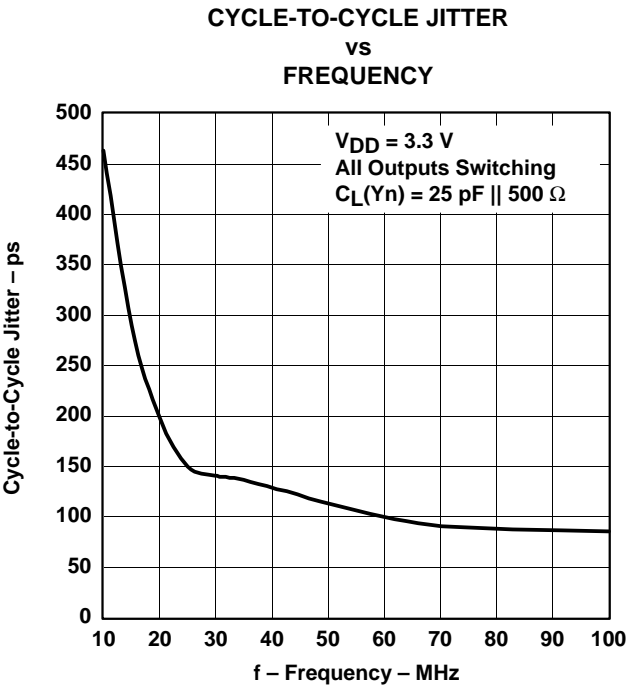


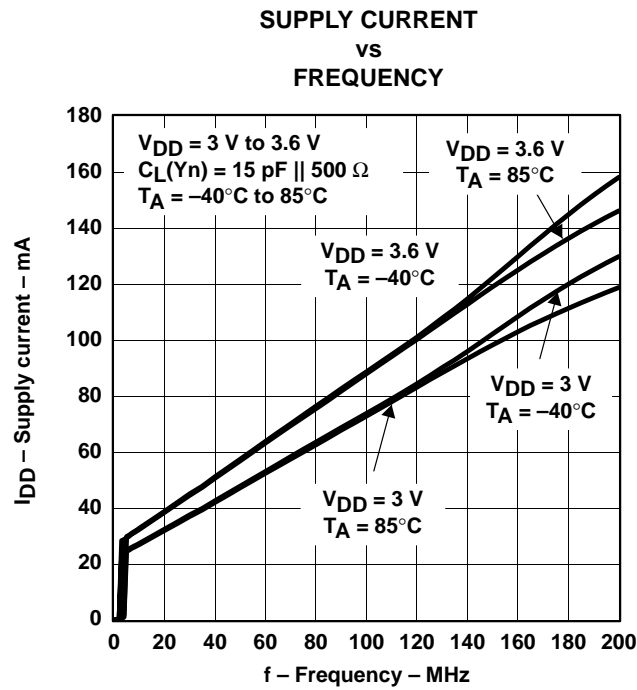
Figure 6



**CDCVF25081**  
**3.3-V PHASED-LOCK LOOP CLOCK DRIVER**

SCAS671A – OCTOBER 2001 – REVISED FEBRUARY 2003

**PARAMETER MEASUREMENT INFORMATION**



**Figure 7**

# CDCVF25081

## 3.3-V PHASED-LOCK LOOP CLOCK DRIVER

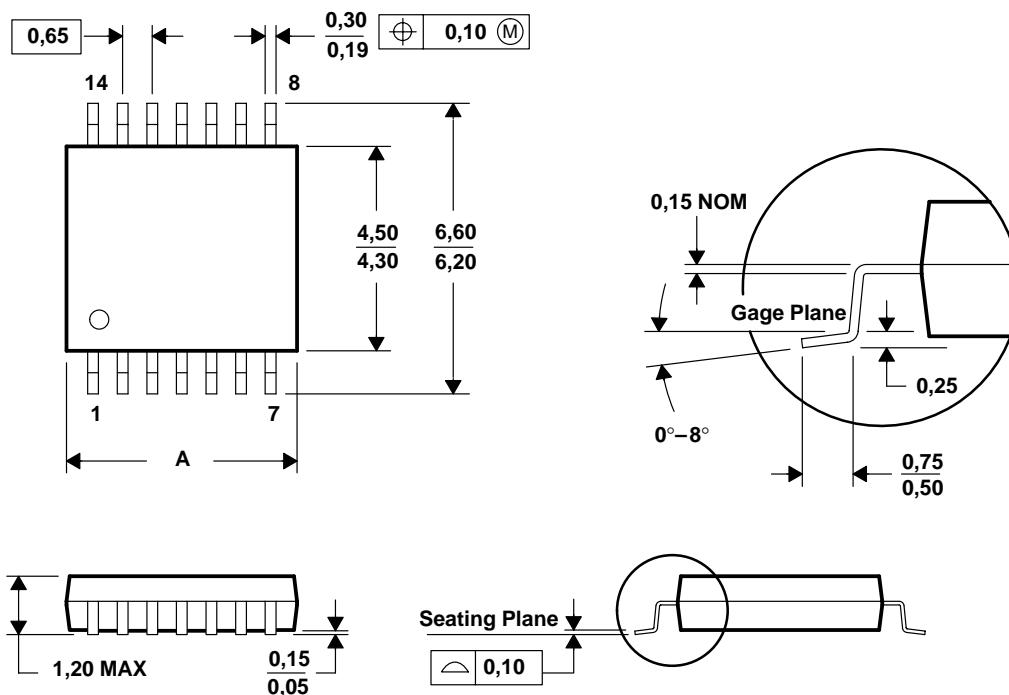
SCAS671A – OCTOBER 2001 – REVISED FEBRUARY 2003

### MECHANICAL DATA

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

**CDCVF25081**  
**3.3-V PHASED-LOCK LOOP CLOCK DRIVER**

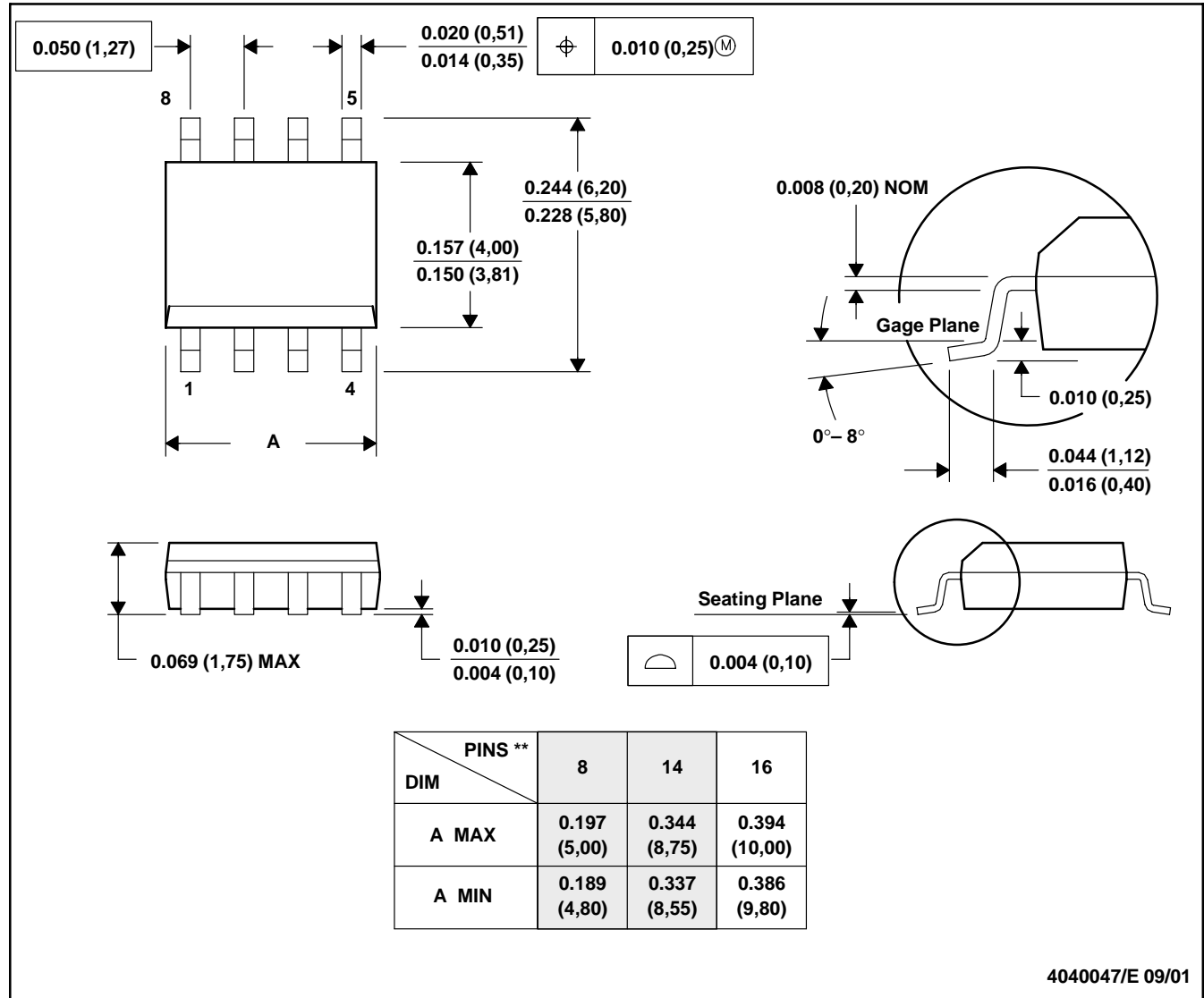
SCAS671A – OCTOBER 2001 – REVISED FEBRUARY 2003

**MECHANICAL DATA**

**D (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**8 PINS SHOWN**



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012

## **IMPORTANT NOTICE**

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

### **Mailing Address:**

Texas Instruments  
Post Office Box 655303  
Dallas, Texas 75265