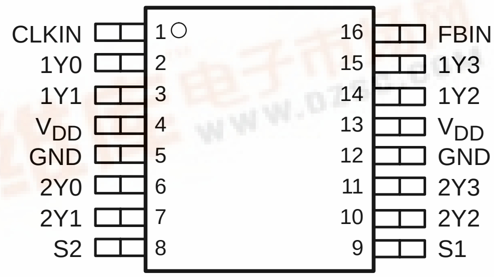
# CDCVF25084
# 3.3-V 1:8 ZERO DELAY (PLL) x4 CLOCK MULTIPLIER

SCAS690A – APRIL 2003 – REVISED MAY 2003

- **Phase-Locked Loop-Based Multiplier by Four**
- **Input Frequency Range: 2.5 MHz to 45 MHz**
- **Output Frequency Range: 10 MHz to 180 MHz**
- **LVCMOS/LVTTL I/O Compatible**
- **Low Jitter (Cycle-Cycle): ±120 ps Over the Range 75 MHz to 180 MHz**
- **Distributes One Clock Input to Two Banks of Four Outputs**
- **Auto Frequency Detection to Disable Device (Power-Down Mode)**
- **Operates From Single 3.3-V Supply**
- **Industrial Temperature Range –40°C to 85°C**
- **25-Ω On-Chip Series Damping Resistors**
- **No External RC Network Required**
- **Spread Spectrum Clock Compatible (SSC)**
- **Available in 16-Pin TSSOP Package**

**PW PACKAGE (TSSOP)**
**(TOP VIEW)**




## description

The CDCVF25084 is a high-performance, low-skew, low-jitter, phase-lock loop clock multiplier. It uses a PLL to precisely align, in both frequency and phase, the output clocks to the input clock signal including a multiplication factor of four. The CDCVF25084 operates from a nominal supply voltage of 3.3 V. The device also includes integrated series-damping resistors in the output drivers that make it ideal for driving point-to-point loads.

Two banks of four outputs each provide low-skew, low-jitter copies of CLKIN x four. All outputs operate at the same frequency. Output duty cycles are adjusted to 50%, independent of duty cycle at CLKIN. The device automatically goes into power-down mode when no input signal is applied to CLKIN and the outputs go into a low state. Unlike many products containing PLLs, the CDCVF25084 does not require an external RC network. The loop filter for the PLL is included on-chip, minimizing component count, space, and cost.

Because it is based on a PLL circuitry, the CDCVF25084 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization is required following power up and application of a fixed-frequency signal at CLKIN and any following changes to the PLL reference.

The CDCVF25084 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| S2 | S1 | 1Y0–1Y3 | 2Y0–2Y3 | OUTPUT SOURCE | PLL SHUTDOWN |
|---|---|---|---|---|---|
| 0 | 0 | Hi-Z | Hi-Z | N/A | Yes |
| 0 | 1 | Active | Hi-Z | PLL† | No |
| 1 | 0 | Active | Active | Input clock (PLL bypass) | Yes |
| 1 | 1 | Active | Active | PLL† | No |

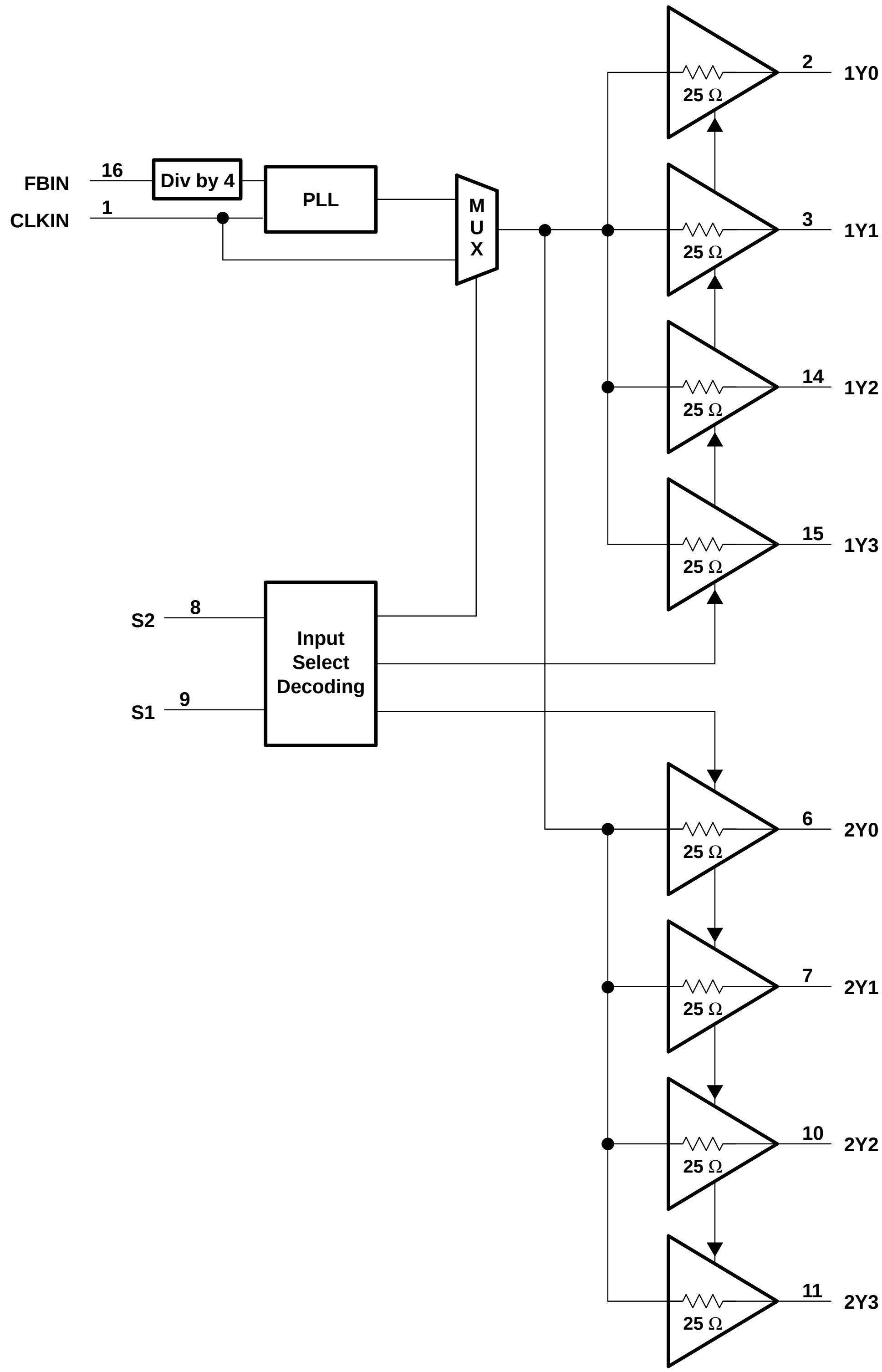
† A CLK input frequency < 2 MHz switches the outputs to low level.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## Terminal Functions

| TERMINAL NAME | TERMINAL PIN NO. | TYPE | DESCRIPTION |
|---|---|---|---|
| 1Y[0:3] | 2, 3, 14, 15 | O | Bank 1Yn clock outputs. These outputs are low-skew copies of CLKIN. Each output has an integrated 25-Ω series-damping resistor. |
| 2Y[0:3] | 6, 7, 10, 11 | O | Bank 2Yn clock outputs. These outputs are low-skew copies of CLKIN. Each output has an integrated 25-Ω series-damping resistor. |
| CLKIN | 1 | I | Clock input. CLKIN provides the clock signal to be distributed by the CDCVF25084 clock driver. CLKIN is used to provide the reference signal to the integrated PLL that generates the output signal. CLKIN must have a fixed frequency and phase in order for the PLL to acquire lock. Once the circuit is powered up and a valid signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to CLKIN. |
| FBIN | 16 | I | Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be wired to one of the outputs to complete the feedback loop of the internal PLL. The integrated PLL synchronizes the FBIN and output signal so there is nominally zero-delay from input clock to output clock. |
| GND | 5, 12 | Ground | Ground |
| S1, S2 | 9, 8 | I | Select pins to determine mode of operation. See the *FUNCTION TABLE* for mode selection options. |
| $V_{DD}$ | 4, 13 | Power | Supply voltage. The supply voltage range is 3 V to 3.6 V |

## functional block diagram



## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, $V_{DD}$ . . . . . . . . . . –0.5 V to 4.6 V
Input voltage range, $V_I$ (see Notes 1 and 2) . . . . . . . . . . –0.5 V to 4.6 V
Output voltage range, $V_O$ (see Notes 1 and 2) . . . . . . . . . . –0.5 V to $V_{DD}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . . . . . . –50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . . . . . . –50 mA
Continuous total output current, $I_O$ ($V_O$ = 0 to $V_{DD}$) . . . . . . . . . . ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): PW package . . . . . . . . . . 147°C/W
Storage temperature range, $T_{stg}$ . . . . . . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{DD}$ | 3 | 3.3 | 3.6 | V |
| Low level input voltage, $V_{IL}$ | | | 0.8 | V |
| High level input voltage, $V_{IH}$ | 2 | | | V |
| Input voltage, $V_I$ | 0 | | 3.6 | V |
| High-level output current, $I_{OH}$ | | | –12 | mA |
| Low-level output current, $I_{OL}$ | | | 12 | mA |
| Operating free-air temperature, $T_A$ | –40 | | 85 | °C |

## timing requirements over recommended ranges of supply voltage, load and operating free-air temperature

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input clock frequency, $f_{CLKIN}$ | | 2.5 | | 45 | MHz |
| Input clock duty cycle | | 40% | | 60% | |
| Clock frequency, $f_{clkout}$ | $C_L$ = 15 pF | 10 | | 180 | MHz |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input voltage | $V_{DD}$ = 3 V, | $I_I$ = –18 mA | | | –1.2 | V |
| $I_I$ | Input current | $V_I$ = 0 V or $V_{DD}$ | | | | ±5 | µA |
| $I_{PD}$ | Power-down current | $f_{CLKIN}$ = 0 MHz, | $V_{DD}$ = 3.3 V | | | 100 | µA |
| $I_{DD}$‡ | Dynamic current | $f_{out}$ = 80 MHz, | $C_L$ = 15 pF | | 60 | 80 | mA |
| $I_{OZ}$ | Output 3-state | $V_o$ = 0 V or $V_{DD}$, | $V_{DD}$ = 3.6 V | | | ±5 | µA |
| $C_I$ | Input capacitance at FBIN, CLKIN | $V_I$ = 0 V or $V_{DD}$ | | | 4 | | pF |
| $C_I$ | Input capacitance at S1, S2 | $V_I$ = 0 V or $V_{DD}$ | | | 2.2 | | pF |
| $C_O$ | Output capacitance | $V_I$ = 0 V or $V_{DD}$ | | | 3 | | pF |
| $V_{OH}$ | High-level output voltage | $V_{DD}$ = min to max, | $I_{OH}$ = –100 µA | $V_{DD}$ – 0.2 | | | V |
| | | $V_{DD}$ = 3 V, | $I_{OH}$ = –12 mA | 2.1 | | | |
| | | $V_{DD}$ = 3 V, | $I_{OH}$ = –6 mA | 2.4 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{DD}$ = min to max, | $I_{OL}$ = 100 µA | | | 0.2 | V |
| | | $V_{DD}$ = 3 V, | $I_{OL}$ = 12 mA | | | 0.8 | |
| | | $V_{DD}$ = 3 V, | $I_{OL}$ = 6 mA | | | 0.55 | |
| $I_{OH}$ | High-level output current | $V_{DD}$ = 3 V, | $V_O$ = 1 V | –24 | | | mA |
| | | $V_{DD}$ = 3.3 V, | $V_O$ = 1.65 V | | –30 | | |
| | | $V_{DD}$ = 3.6 V, | $V_O$ = 3.135 V | | | -15 | |
| $I_{OL}$ | Low-level output current | $V_{DD}$ = 3 V, | $V_O$ = 1.95 V | 26 | | | mA |
| | | $V_{DD}$ = 3.3 V, | $V_O$ = 1.65 V | | 33 | | |
| | | $V_{DD}$ = 3.6 V, | $V_O$ = 0.4 V | | | 14 | |

† All typical values are at respective nominal $V_{DD}$.
‡ All outputs are switching; for $I_{DD}$ over frequency see Figure 9.

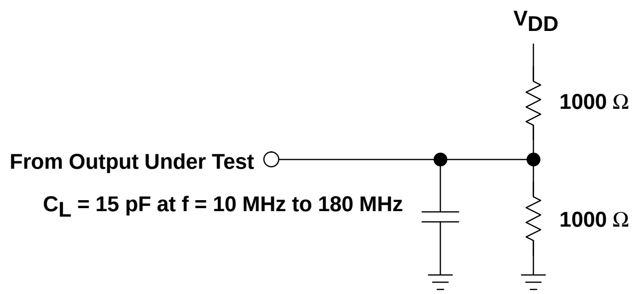
## switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{(lock)}$ | PLL lock time | $f_{out}$ = 100 MHz | | 2 | | µs |
| $t_{(phoffset)}$ | Phase offset (CLKIN to FBIN), (see Note 5) | $f_{out}$ = 40 MHz to 75 MHz, Vth = $V_{DD}$/2 | | | ±200 | ps |
| | | $f_{out}$ = 75 MHz to 180 MHz, Vth = $V_{DD}$/2 | | | ±100 | |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | S2 = High, S1 = Low (PLL bypass mode) | 2.3 | | 4.5 | ns |
| $t_{sk(o)}$ | Output skew (Yn to Yn) (see Note 4) | See Figure 3 | | 75 | 150 | ps |
| $t_{sk(pp)}$ | Part-to-part skew (low-to-high transition) | PLL bypass mode | | | 900 | ps |
| | | PLL mode, $f_{out}$ = 40 MHz to 75 MHz | | | 350 | |
| | | PLL mode, $f_{out}$ = 75 MHz to 180 MHz | | | 300 | |
| $t_{jit(cc)}$ | Jitter (cycle-to-cycle) | $f_{out}$ = 40 MHz to 75 MHz | | | ±220 | ps |
| | | $f_{out}$ = 75 MHz to 180 MHz | | | ±120 | ps |
| $t_{jit(per)}$ | Period jitter | $f_{out}$ = 40 MHz to 75 MHz | | | 260 | ps |
| | | $f_{out}$ = 75 MHz to 180 MHz | | | 140 | ps |
| $t_{jit(\theta)}$ | Phase jitter | $f_{out}$ = 75 MHz to 180 MHz, peak-to-peak (see Note 6) | | | ±110 | ps |
| | | $f_{out}$ = 75 MHz to 180 MHz, RMS (see Note 6) | | | 26 | ps |
| odc | Output duty cycle | $f_{out}$ = 10 MHz to 180 MHz | 45% | | 55% | |
| $t_{sk(p)}$ | Pulse skew | S2 = High, S1 = low (PLL bypass mode) | | | 0.3 | ns |
| $t_r$, $t_f$ | Rise / fall time rate | See Figure 4 | 1 | | 3 | V/ns |

† All typical values are at respective nominal $V_{DD}$.

NOTES: 4. The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.
5. Similar waveform at CLKIN and FBIN are required. Output 1Y3 is used as a feedback to FBIN loaded with 11 pF and all other outputs have 15 pF. For phase displacement between CLKIN and Y-outputs, see Figure 5.
6. Input phase jitter < ±50 ps; output sample size is 20000 cycles.

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: $Z_O$ = 50 Ω, $t_r$ < 1.2 ns, $t_f$ < 1.2 ns
C. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Test Load Circuit**

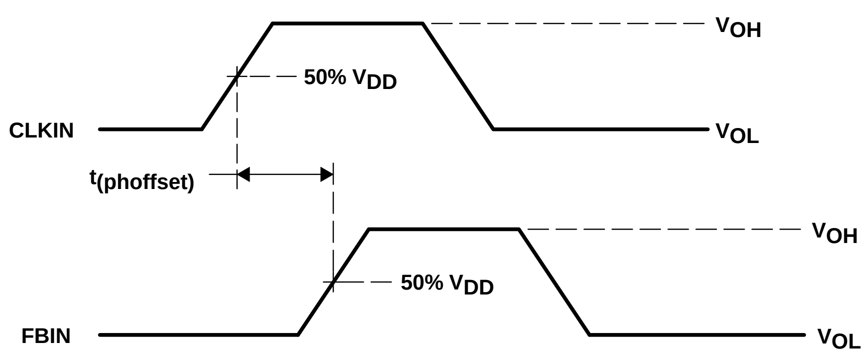
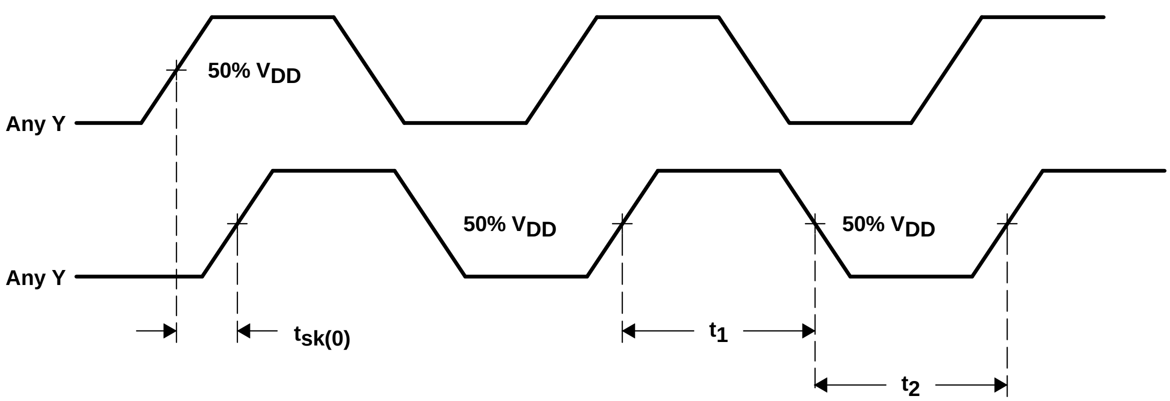


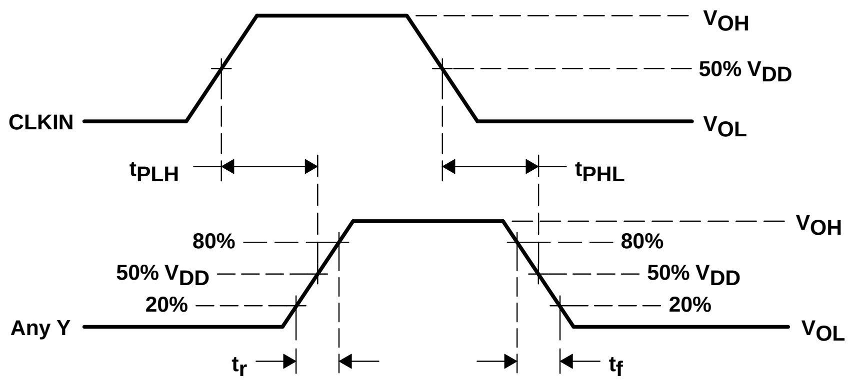

**Figure 2. Voltage Thresholds for Measurements, Phase Offset (PLL Mode)**




NOTE: odc = $t_1/(t_1 + t_2)$ x 100%

**Figure 3. Output Skew and Output Duty Cycle (PLL Mode)**

## PARAMETER MEASUREMENT INFORMATION




NOTE: $t_{sk(p)}=|t_{PLH}–t_{PHL}|$

**Figure 4. Propagation Delay and Pulse Skew (Non-PLL Mode)**

**PHASE DISPLACEMENT vs CLOAD**

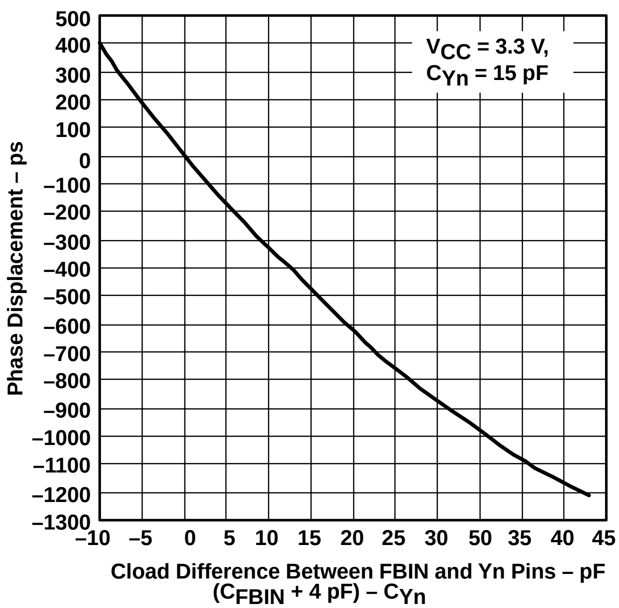



**Figure 5**

**PHASE OFFSET vs FREQUENCY**

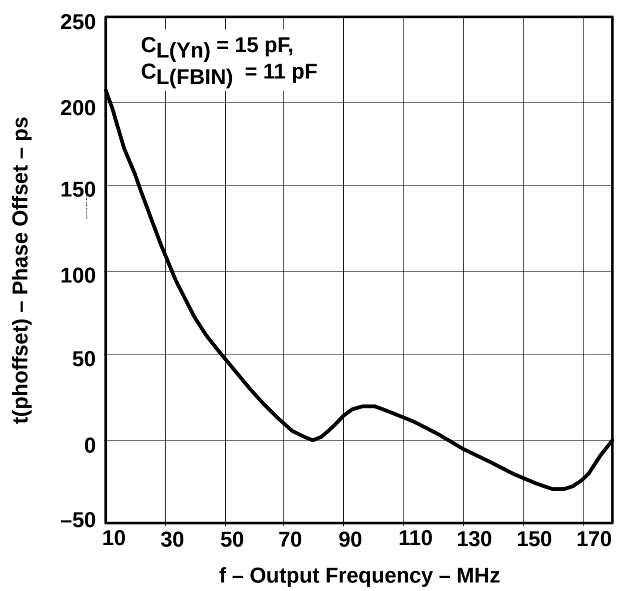



**Figure 6**

## PARAMETER MEASUREMENT INFORMATION

**CYCLE-TO-CYCLE / PERIOD JITTER vs FREQUENCY**

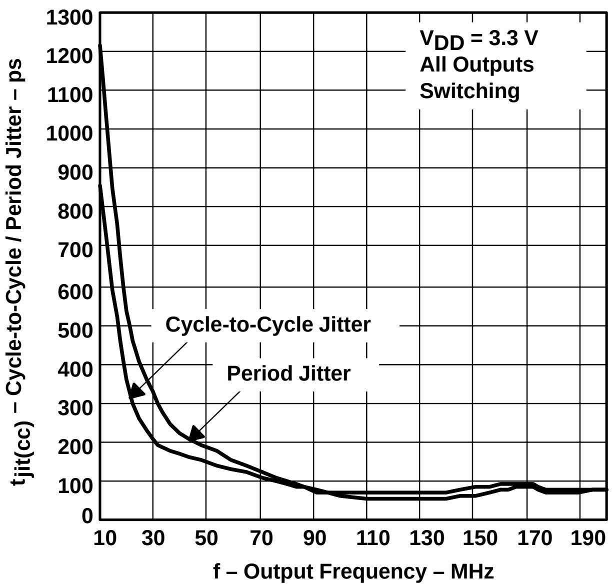



**Figure 7**

**TRANSFER CHARACTERISTIC FROM CLKIN TO Yn**

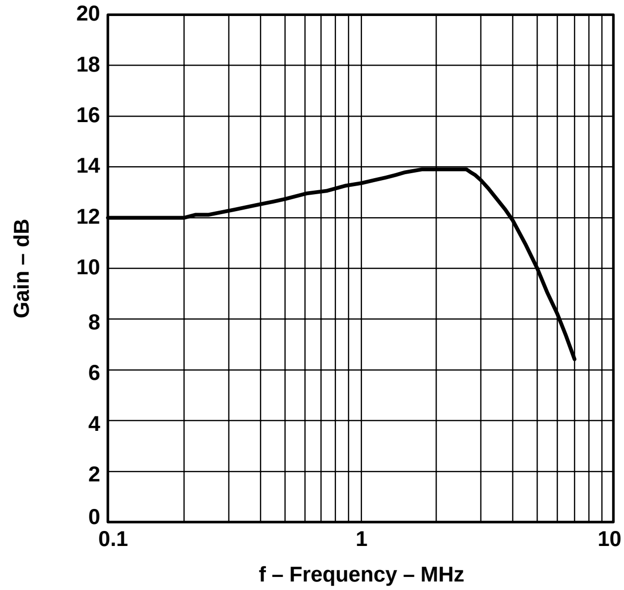



**Figure 8**

**SUPPLY CURRENT vs FREQUENCY**

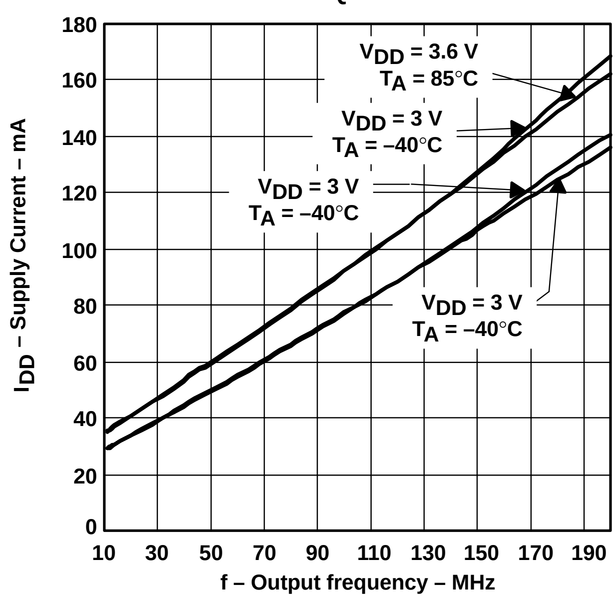
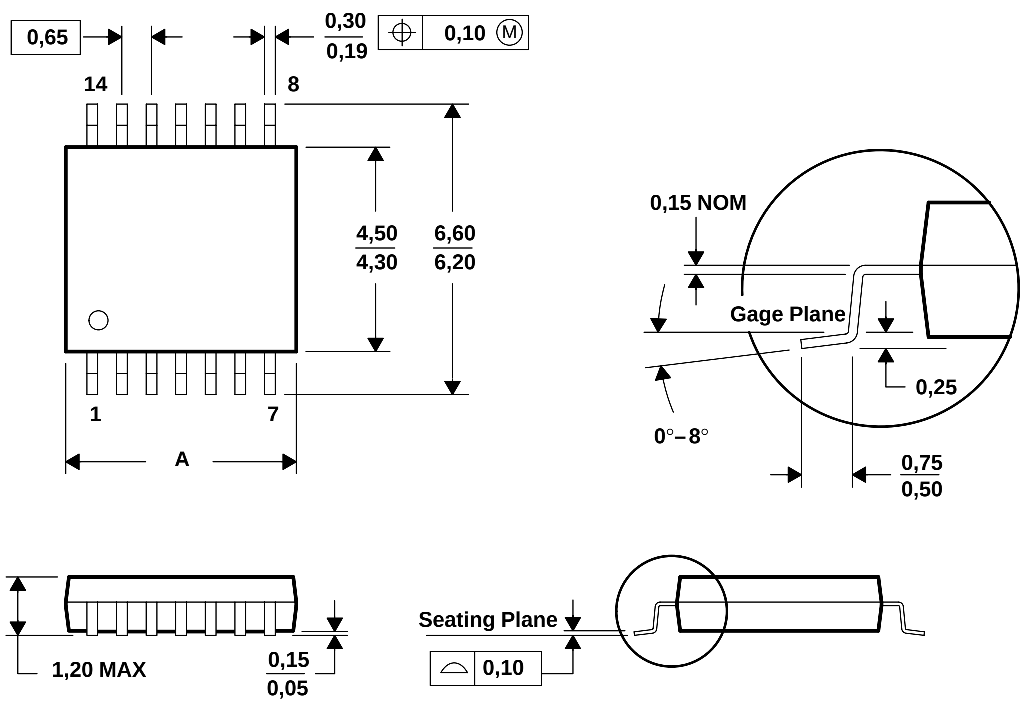



**Figure 9**

## MECHANICAL DATA

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**




| PINS ** / DIM | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

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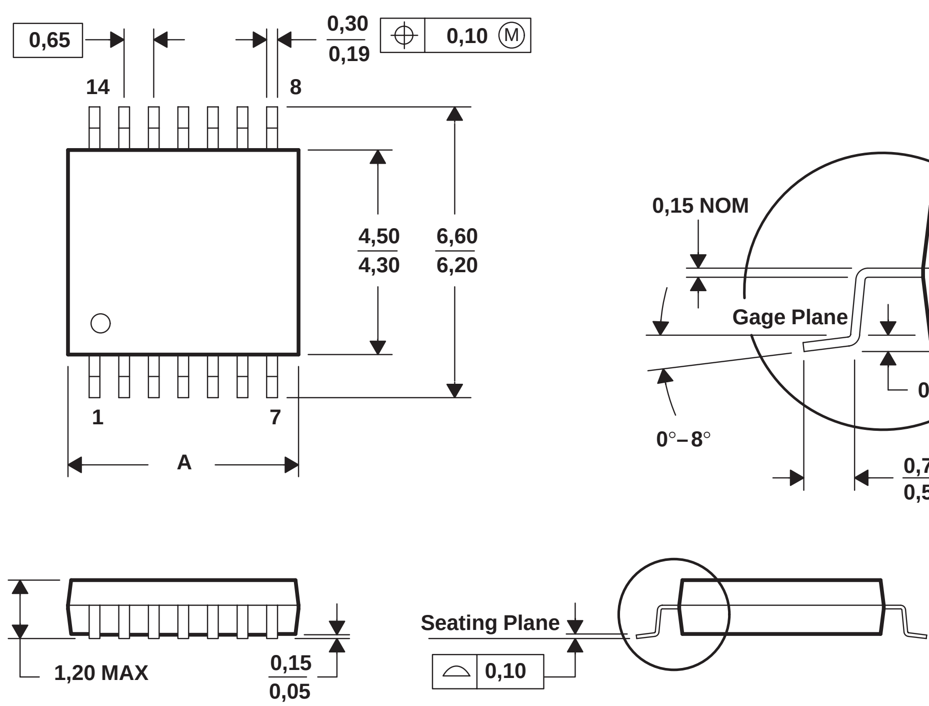


| PINS ** / DIM | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
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**IMPORTANT NOTICE**



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