- **General-Purpose and PCI-X 1:4 Clock Buffer**
- **Operating Frequency: 0 MHz to 140 MHz**
- **Low Output Skew: <100 ps**
- **Distributes One Clock Input to One Bank of Four Outputs**
- **Output Enable Control That Drives Outputs Low When OE Is Low**
- **Operates From Single 3.3-V Supply**
- **8-Pin TSSOP Package**

TSSOP
PW PACKAGE
(TOP VIEW)

description

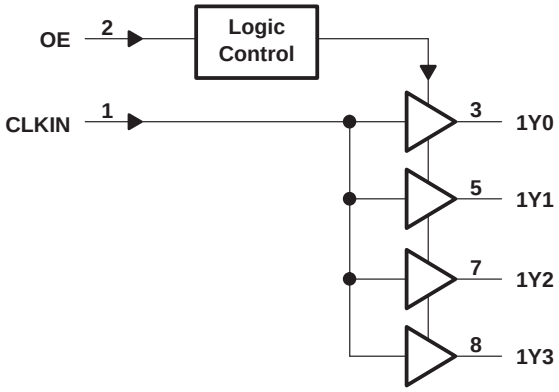
The CDCV304 is a high-performance, low-skew, general-purpose and PCI-X clock buffer. It distributes one input clock signal (CLKIN) to the output clocks (1Y[0:3]). It is specifically designed for use with PCI-X applications. The CDCV304 operates at 3.3 V.

The CDCV304 is characterized for operation from −40°C to 85°C for automotive and industrial applications.

FUNCTION TABLE

INPUTS		OUTPUT
CLKIN	**OE**	**1Y (0:3)**
L	L	L
H	L	L
L	H	L
H	H	H

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
1Y[0−3]	3, 5, 7, 8	O	Buffered output clocks
CLKIN	1	I	Input reference frequency
GND	4	Power	Ground
OE	2	I	Outputs enable control
V_{DD}3.3V	6	Power	3.3-V supply

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD} . . . . . −0.5 V to 4.3 V
Input voltage range, V_I (see Notes 1 and 2) . . . . . −0.5 V to V_{DD} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . −0.5 V to V_{DD} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) . . . . . ±50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) . . . . . ±50 mA
Continuous total output current, I_O (V_O = 0 to V_{DD}) . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 3): PW package . . . . . 230.5°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	3.3	3.6	V
High-level input voltage, V_{IH}	0.7×V_{DD}			V
Low-level input voltage, V_{IL}			0.3×V_{DD}	V
Input voltage, V_I	0		V_{DD}	V
High-level output current, I_{OH}			−24	mA
Low-level output current, I_{OL}			24	mA
Operating free-air temperature, T_A	−40		85	°C

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	NOM	MAX	UNIT
f_{clk}	Clock frequency	0		140	MHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input voltage	V_{DD} = 3 V,	I_I = −18 mA			−1.2	V
V_{OH}	High-level output voltage	V_{DD} = min to max,	I_{OH} = −1 mA	V_{DD}−0.2			V
		V_{DD} = 3 V,	I_{OH} = −24 mA	2			
		V_{DD} = 3 V,	I_{OH} = −12 mA	2.4			
V_{OL}	Low-level output voltage	V_{DD} = min to max,	I_{OL} = 1 mA			0.2	V
		V_{DD} = 3 V,	I_{OL} = 24 mA			0.8	
		V_{DD} = 3 V,	I_{OL} = 12 mA			0.55	
I_{OH}	High-level output current	V_{DD} = 3 V,	V_O = 1 V	−50			mA
		V_{DD} = 3.3 V,	V_O = 1.65 V		−55		
I_{OL}	Low-level output current	V_{DD} = 3 V,	V_O = 2 V	60			mA
		V_{DD} = 3.3 V,	V_O = 1.65 V		70		
I_I	Input current	V_I = V_O or V_{DD}				±5	µA
I_{DD}	Dynamic current, See Figure 5	f = 67 MHz				37	mA
C_i	Input capacitance	V_{DD} = 3.3 V,	V_I = 0 V or V_{DD}		3		pF
C_o	Output capacitance	V_{DD} = 3.3 V,	V_I = 0 V or V_{DD}		3.2		pF

† All typical values are at respective nominal V_{DD} and 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 10 pF, V_{DD} = 3.3 V ± 0.3 V (see Note 6 and Figures 1 and 2)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	High-to-low propagation delay	See Figures 1 and 2	1.8	2.5	3	ns
t_{PHL}	Low-to-high propagation delay		1.8	2.4	3	ns
$t_{sk(o)}$	Output skew (see Note 4)			50	100	ps
$t_{sk(p)}$	Pulse skew	V_{IH} = V_{DD}, V_{IL} = 0 V			150	ps
$t_{sk(pr)}$	Process skew			0.2	0.3	ns
$t_{sk(pp)}$	Part-to-part skew			0.25	0.4	ns
T_{high}	CLK high time, See Figure 4	66 MHz	6			ns
		140 MHz	3			
T_{low}	CLK low time, See Figure 4	66 MHz	6			ns
		140 MHz	3			
t_r	Output rise slew rate‡	0.2V_{DD} to 0.6V_{DD}	1.5	2.7	4	V/ns
t_f	Output fall slew rate‡	0.6V_{DD} to 0.2V_{DD}	1.5	2.7	4	V/ns

† All typical values are at respective nominal V_{DD}.
‡ This symbol is according to PCI-X terminology.
NOTE 4: The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

PARAMETER MEASUREMENT INFORMATION

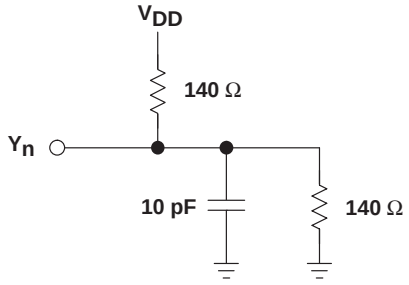


Figure 1. Test Load Circuit

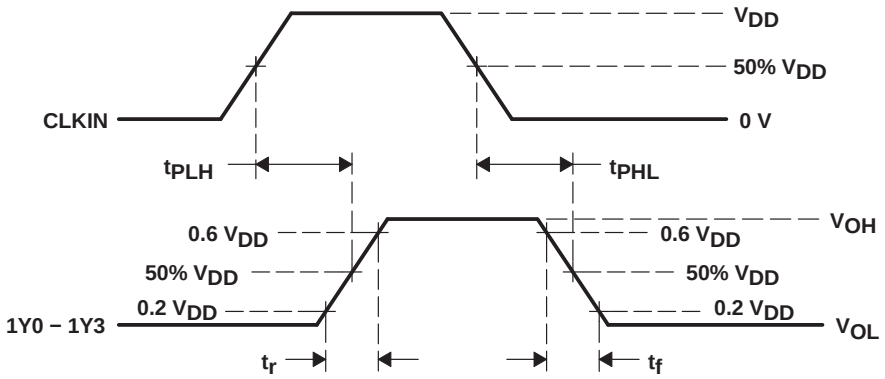


Figure 2. Voltage Thresholds for Propagation Delay (t_{pd}) Measurements

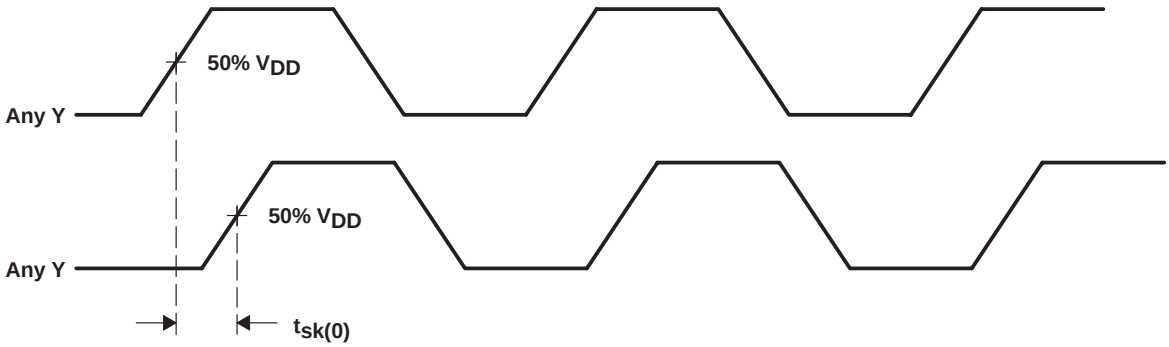
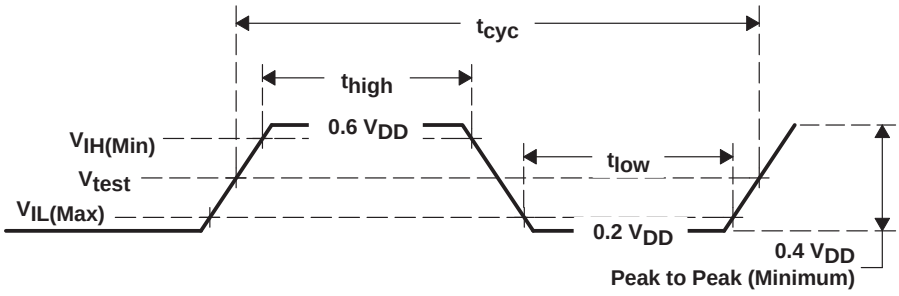


Figure 3. Output Skew

PARAMETER	VALUE	UNIT
$V_{IH(Min)}$	0.5 V_{DD}	V
$V_{IL(Max)}$	0.35 V_{DD}	V
V_{test}	0.4 V_{DD}	V



NOTE: All parameters in Figure 4 are according to PCI-X 1.0 specifications.

Figure 4. Clock Waveform

PARAMETER MEASUREMENT INFORMATION

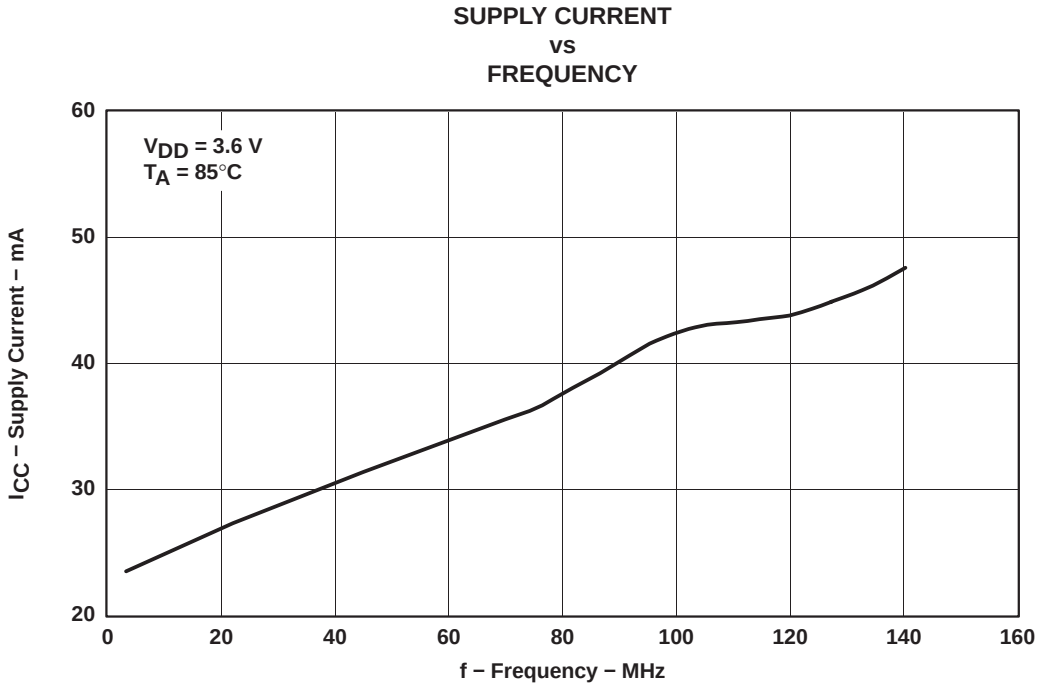


Figure 5

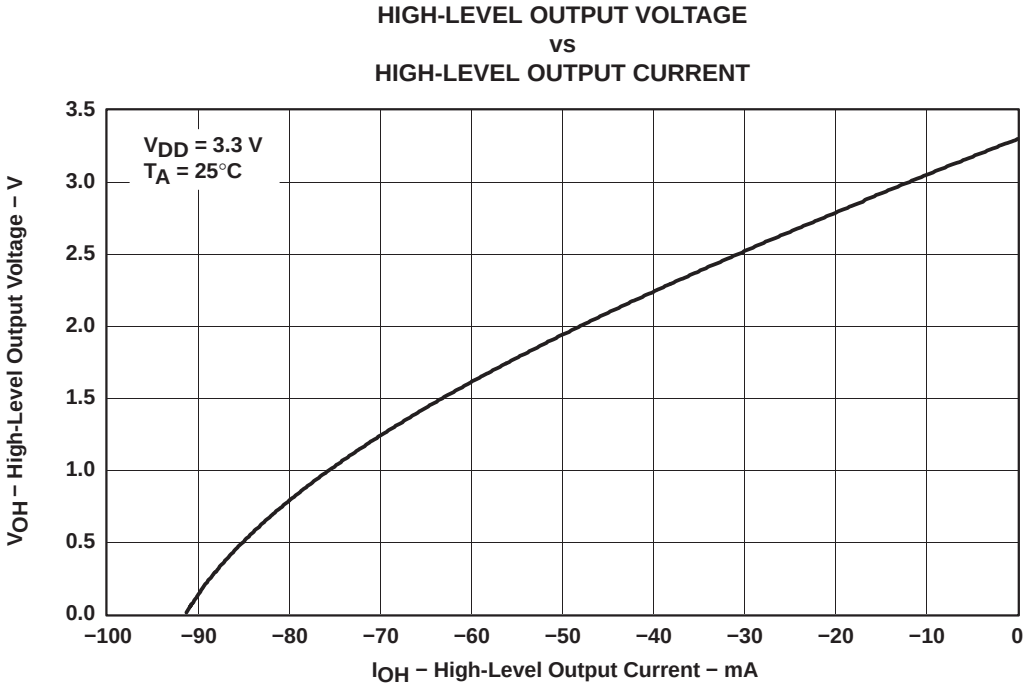


Figure 6

PARAMETER MEASUREMENT INFORMATION

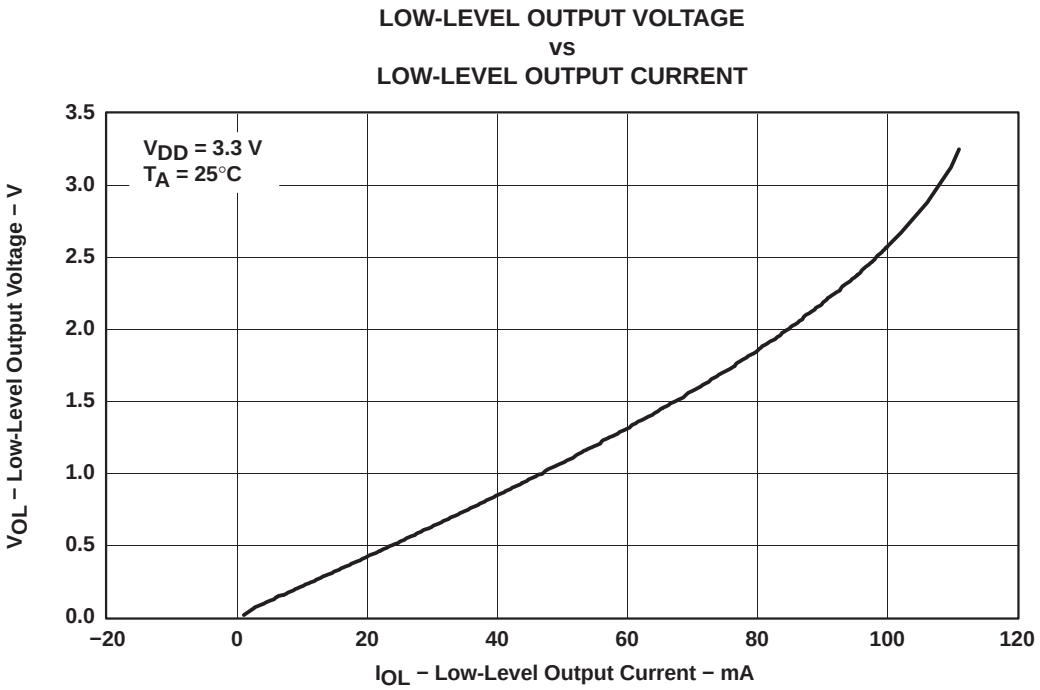


Figure 7

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
8/23/06	A	5	Parameter Measurement Information	Changed Figure 5 deleting the first 2 MHz line from the drawing.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CDCV304PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCV304PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCV304PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCV304PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

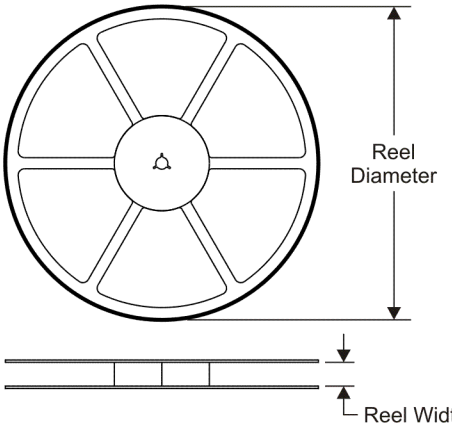
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

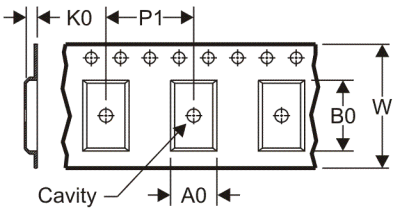
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

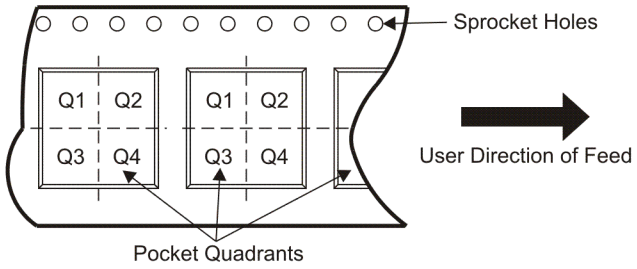


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

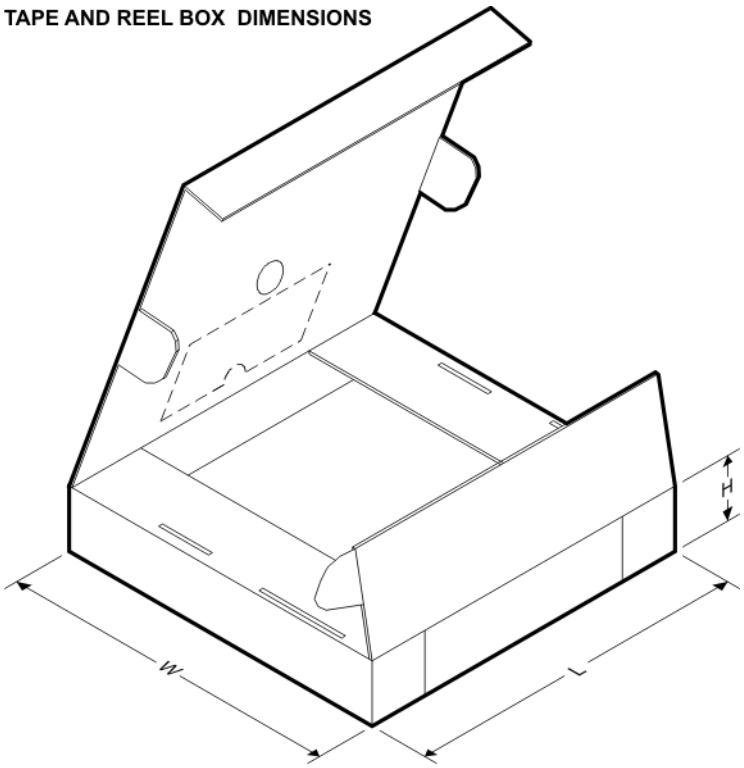
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCV304PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

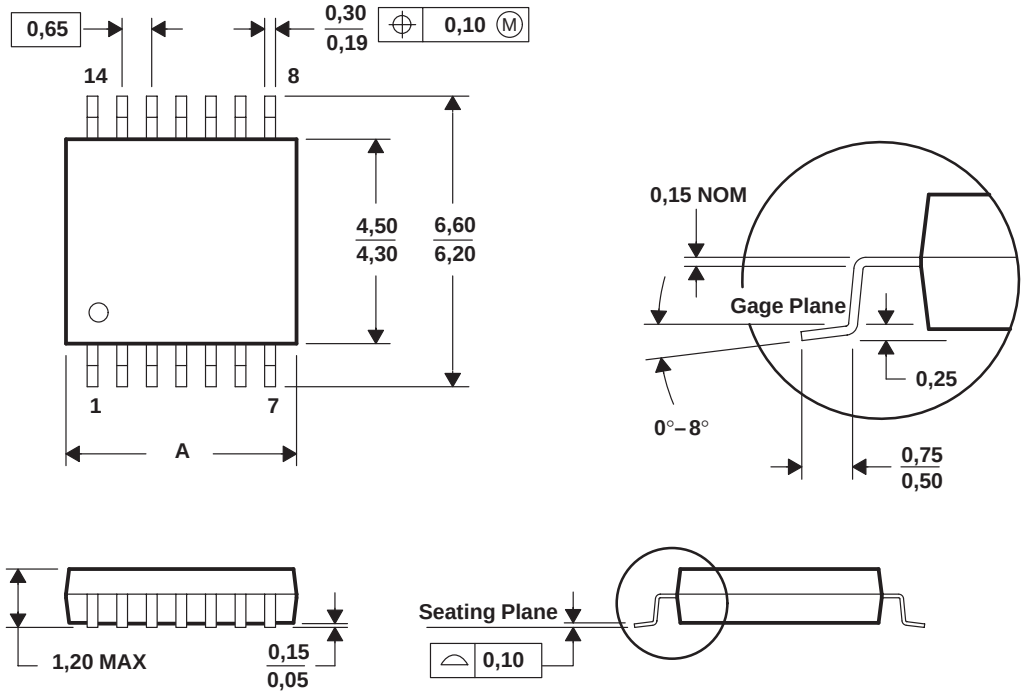


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCV304PWR	TSSOP	PW	8	2000	346.0	346.0	29.0

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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