intersil

CDP1802AC/3

March 1997

High-Reliability CMOS 8-Bit Microprocessor

Features

- **For Use In Aerospace, Military, and Critical Industrial Equipment**
- **Minimum Instruction Fetch-Execute Time of 4.5μs (Maximum Clock Frequency of 3.6MHz) at V_{DD} = 5V, T_A = +25°C**
- **Operation Over the Full Military Temperature Range . . . . . -55°C to +125°C**
- **Any Combination of Standard RAM and ROM Up to 65,536 Bytes**
- **8–Bit Parallel Organization With Bidirectional Data Bus and Multiplexed Address Bus**
- **16 x 16 Matrix of Registers for Use as Multiple Program Counters, Data Pointers, or Data Registers**
- **On-Chip DMA, Interrupt, and Flag Inputs**
- **High Noise Immunity . . . . . 30% of V_{DD}**

Ordering Information

PACKAGE	TEMP. RANGE (°C)	5V - 3.2MHz	PKG NO.
SBDIP	-55 to 125	CDP1802ACD3	D40.6

Description

The CDP1802A/3 High-Reliability LSI CMOS 8-bit register oriented Central-Processing Unit (CPU) is designed for use as a general purpose computing or control element in a wide range of stored-program systems or products.

The CDP1802A/3 includes all of the circuits required for fetching, interpreting, and executing instructions which have been stored in standard types of memories. Extensive input/output (I/O) control features are also provided to facilitate system design.

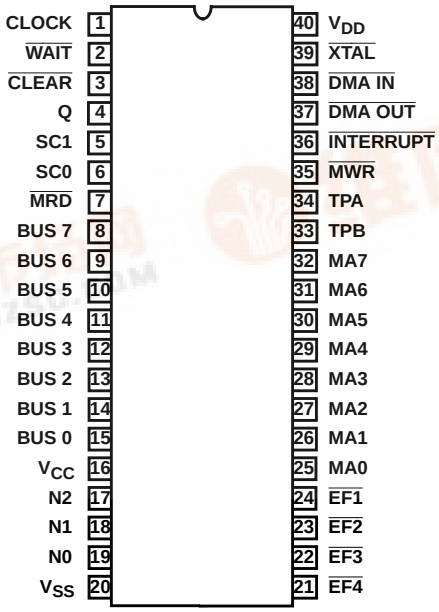
The 1800 Series Architecture is designed with emphasis on the total microcomputer system as an integral entity so that systems having maximum flexibility and minimum cost can be realized. The 1800 Series CPU also provides a synchronous interface to memories and external controllers for I/O devices, and minimizes the cost of interface controllers. Further, the I/O interface is capable of supporting devices operating in polled, interrupt-driven, or direct memory-access modes.

The CDP1802AC/3 is functionally identical to its predecessor, the CDP1802. The “A” version includes some performance enhancements and can be used as a direct replacement in systems using the CDP1802.

This type is supplied in 40 lead dual-in-line sidebrazed ceramic packages (D suffix).

Pinout

CDP1802AC/3 (SBDIP)
TOP VIEW



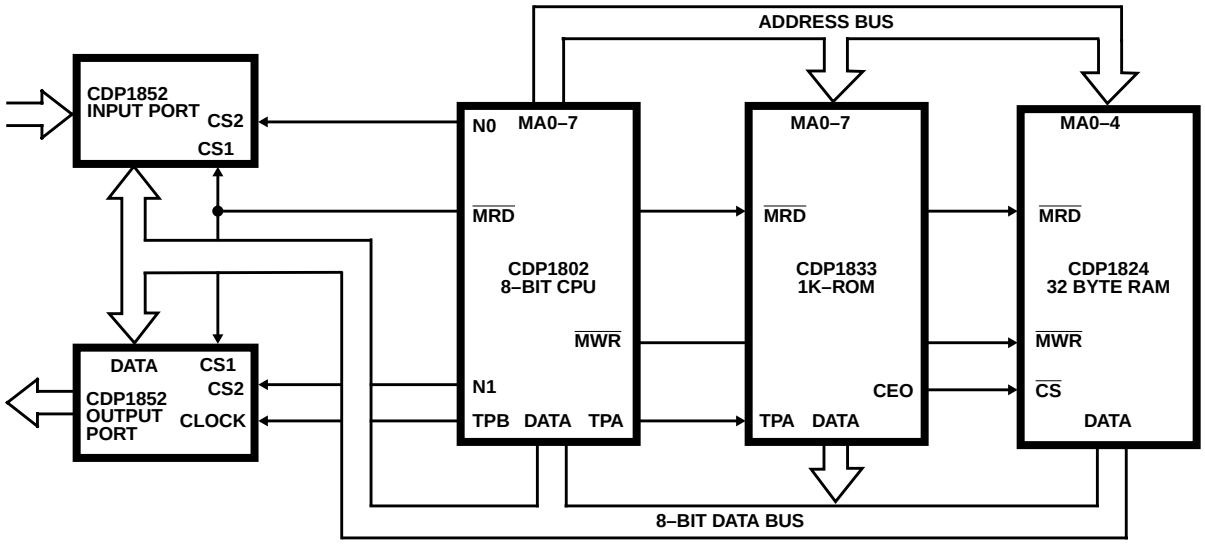


FIGURE 1. TYPICAL CDP1802A/3 SMALL MICROPROCESSOR SYSTEM

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1802AC/3 . . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, any One Input . . . . . ±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (^{o}C/W)	θ_{JC} (^{o}C/W)
SBDIP Package	55	15

Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range 100mW
Operating Temperature Range (T_A)
Package Type D . . . . . -55^{o}C to +125^{o}C
Storage Temperature Range (T_{STG}) . . . . . -65^{o}C to +150^{o}C
Lead Temperature (During Soldering)
At distance 1/16 ±1/32 In. (1.59 ±0.79mm)
from case for 10s max . . . . . +265^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges

PARAMETER	MIN	MAX	UNITS
DC Operating Voltage Range	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V
Maximum Clock Input Rise or Fall Time	-	1	µs

Performance Specifications

PARAMETER	V_{DD} (V)	-55^{o}C TO +25^{o}C	+125^{o}C	UNITS
Minimum Instruction Time (Note 1)	5	4.5	5.9	µs
Maximum DMA Transfer Rate	5	450	340	Kbytes/s
Maximum Clock Input Frequency, Load Capacitance (C_L) = 50pF, f_{CL}	5	DC-3.6	DC-2.7	MHz

NOTE:

1. Equals 2 machine cycles - one Fetch and one Execute operation for all instructions except Long Branch and Long Skip, which require 3 machine cycles - one Fetch and two Execute operations.

Static Electrical Specifications

All Limits are 100% Tested

PARAMETER	CONDITIONS			-55^{o}C, +25^{o}C		+125^{o}C		UNITS
	V_{OUT} (V)	V_{IN}, (V)	V_{CC}, V_{DD} (V)	MIN	MAX	MIN	MAX	
Quiescent Device Current, I_{DD}	-	-	5	-	100	-	250	µA
Output Low Drive (Sink) Current (Except $\overline{XTAL}$), I_{OL}	0.4	0, 5	5	1.20	-	0.90	-	mA
$\overline{XTAL}$	0.4	5	5	185	-	140	-	µA
Output High Drive (Source) Current (Except $\overline{XTAL}$), I_{OH}	4.6	0, 5	5	-	-0.30	-	-0.20	mA
$\overline{XTAL}$	4.6	0	5	-	-135	-	-100	µA
Output Voltage Low-Level, V_{OL}	-	0, 5	5	-	0.1	-	0.2	V
Output Voltage High-Level, V_{OH}	-	0, 5	5	4.9	-	4.8	-	V

Static Electrical Specifications All Limits are 100% Tested **(Continued)**

PARAMETER	CONDITIONS			-55°C, +25°C		+125°C		UNITS
	V_{OUT} (V)	V_{IN}, (V)	V_{CC}, V_{DD} (V)	MIN	MAX	MIN	MAX	
Input Low Voltage, V_{IL}	0.5, 4.5	-	5	-	1.5	-	1.5	V
Input High Voltage, V_{IH}	0.5, 4.5	-	5	3.5	-	3.5	-	V
Input Leakage Current, I_{IN}	Any Input	0, 5	5	-	±1	-	±5	µA
Three-State Output Leakage Current, I_{OUT}	0, 5	0, 5	5	-	±1	-	±5	µA

NOTE:

2. 5V level characteristics apply to Part No. CDP1802AC/3, and 5V and 10V level characteristics apply to part No. CDP1802A/3.

Timing Specifications As a Function of T (T = 1/fCLOCK), C_L = 50 pF

PARAMETER	V_{DD} (V)	LIMITS (NOTE 3)		
		-55°C, +25°C	+125°C	UNITS
High-Order Memory-Address Byte Setup to TPA ↘ Time, t_{SU}	5	2T-450	2T-580	ns
High-Order Memory-Address Byte Hold After TPA Time, t_H	5	T/2 +0	T/2 +0	ns
Low-Order Memory-Address Byte Hold After WR Time, t_H	5	T-30	T-40	ns
CPU Data to Bus Hold After WR Time, t_H	5	T-170	T-250	ns
Required Memory Access Time Address to Data, t_{ACC}	5	5T-300	5T-400	ns

NOTE:

3. These limits are not directly tested.

Implicit Specifications (Note 4) T_A = -55°C to +25°C

PARAMETER		SYMBOL	V_{DD} (V)	TYPICAL VALUES	UNITS
Typical Total Power Dissipation Idle "00" at M(0000), C_L = 50pF	f = 2MHz	-	5	4	mW
Effective Input Capacitance any Input	-	C_{IN}	-	5	pF
Effective Three-State Terminal Capacitance Data Bus	-		-	7.5	pF
Minimum Data Retention Voltage	-	V_{DR}	-	2.4	V
Data Retention Current	-	I_{DR}	2.4	10	µA

NOTE:

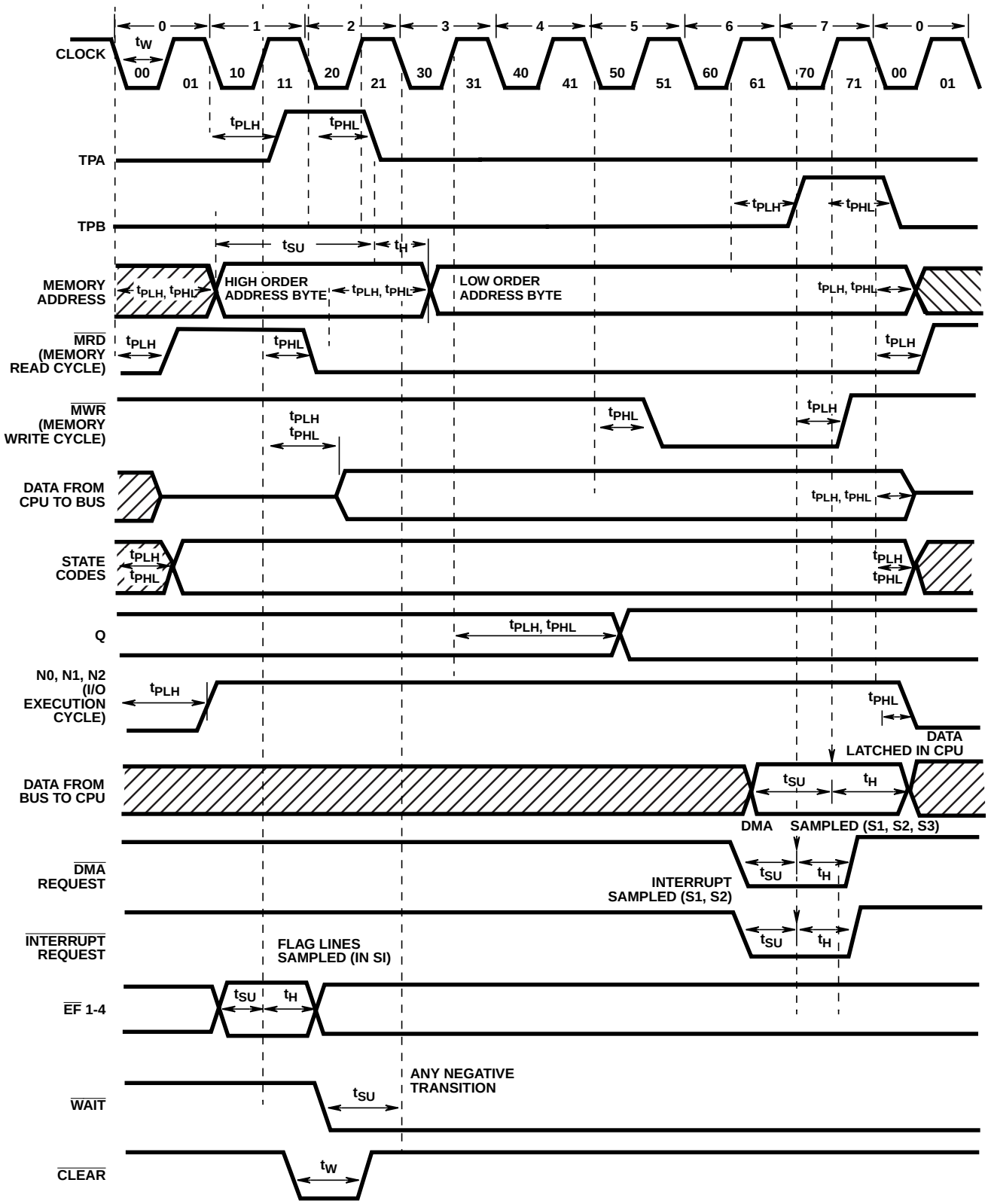
4. These specifications are not tested. Typical values are provided for guidance only.

Dynamic Electrical Specifications C_L = 50pF, Timing Measurement at 0.5 V_{DD} Point

PARAMETERS	V_{DD} (V)	-55°C TO +25°C		+125°C		UNITS
		MIN	MAX	MIN	MAX	
Progagation Delay Times, t_{PLH}, t_{PHL}						
Clock to TPA, TPB	5	-	275	-	370	ns
Clock-to-Memory High Address Byte, t_{PLH}, t_{PHL}	5	-	725	-	950	ns
Clock-to-Memory Low Address Byte Valid, t_{PLH}, t_{PHL}	5	-	340	-	425	ns
Clock to $\overline{MRD}$, t_{PLH}, t_{PHL}	5	-	340	-	425	ns
Clock to $\overline{MWR}$, t_{PLH}, t_{PHL}	5	-	275	-	370	ns
Clock to (CPU DATA to BUS) Valid, t_{PLH}, t_{PHL}	5	-	430	-	550	ns
Clock to State Code, t_{PLH}, t_{PHL}	5	-	440	-	550	ns
Clock to Q, t_{PLH}, t_{PHL}	5	-	375	-	475	ns
Clock to N (0 - 2), t_{PLH}, t_{PHL}	5	-	400	-	525	ns
Interface Timing Requirements (Note 5)						
Data Bus Input Setup, t_{SU}	5	10	-	10	-	ns
Data Bus Input Hold, t_H	5	175	-	230	-	ns
$\overline{DMA}$ Setup, t_{SU}	5	10	-	10	-	ns
$\overline{DMA}$ Hold, t_H	5	200	-	270	-	ns
Interrupt Setup, t_{SU}	5	10	-	10	-	ns
Interrupt Hold, t_H	5	175	-	230	-	ns
$\overline{WAIT}$ Setup, t_{SU}	5	30	-	30	-	ns
$\overline{EF1\text{-}4}$ Setup, t_{SU}	5	20	-	20	-	ns
$\overline{EF1\text{-}4}$ Hold, t_H	5	100	-	135	-	ns
Required Pulse Width Times						
$\overline{CLEAR}$ Pulse Width, t_{WL}	5	150	-	200	-	ns
$\overline{CLOCK}$ Pulse Width, t_{WL}	5	140	-	185	-	ns

NOTE:

5. Minimum input setup and hold times required by Part CDP1802AC/3.



NOTES:

6. This timing diagram is used to show signal relationships only, and does not represent any specific machine cycle.
7. All measurements are referenced to 50% point of the waveforms.
8. Shaded areas indicate “don’t care” or undefined state. Multiple transitions may occur during this period.

FIGURE 2. TIMING WAVEFORMS

Performance Curves

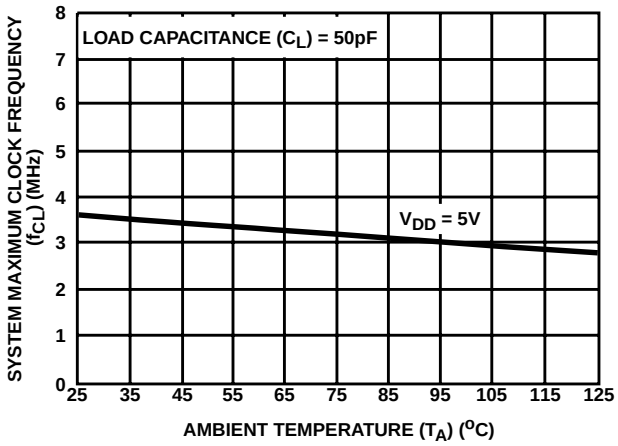


FIGURE 3. TYPICAL MAXIMUM CLOCK FREQUENCY AS A FUNCTION OF TEMPERATURE

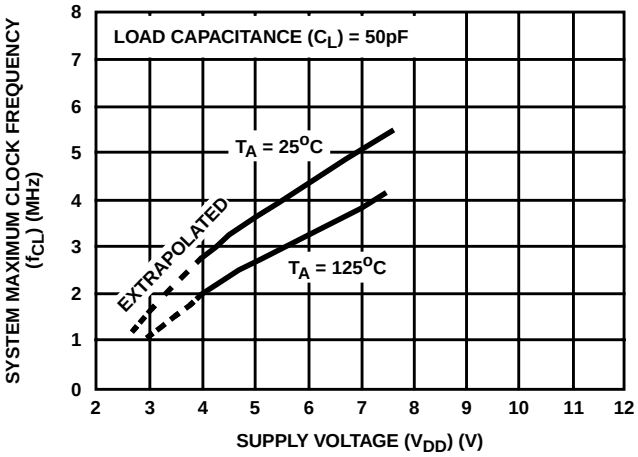


FIGURE 4. TYPICAL MAXIMUM CLOCK FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

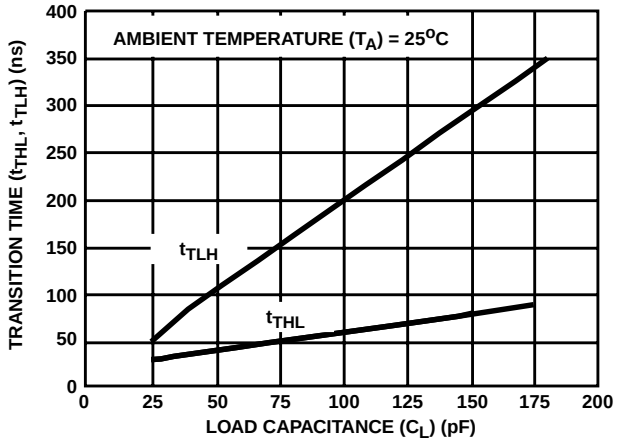


FIGURE 5. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

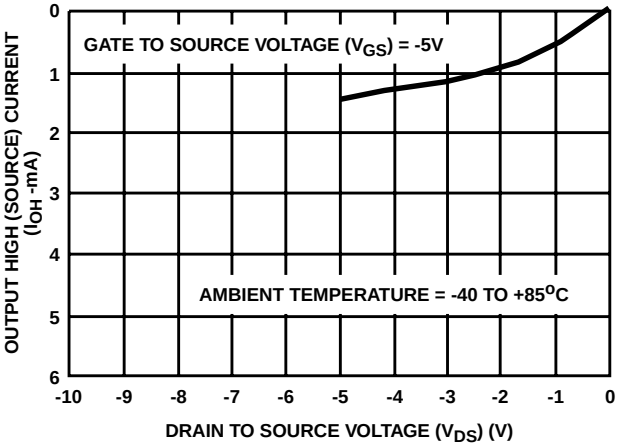


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

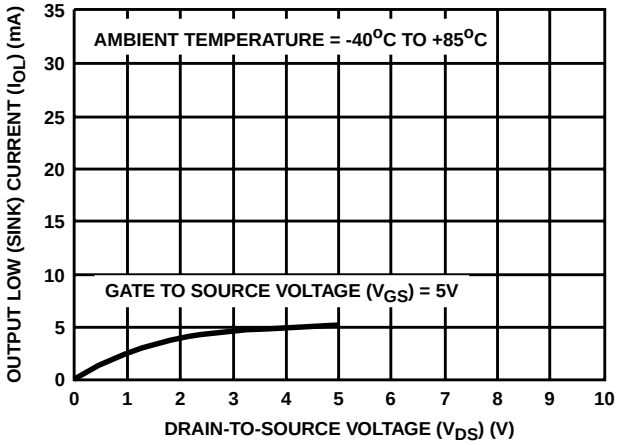
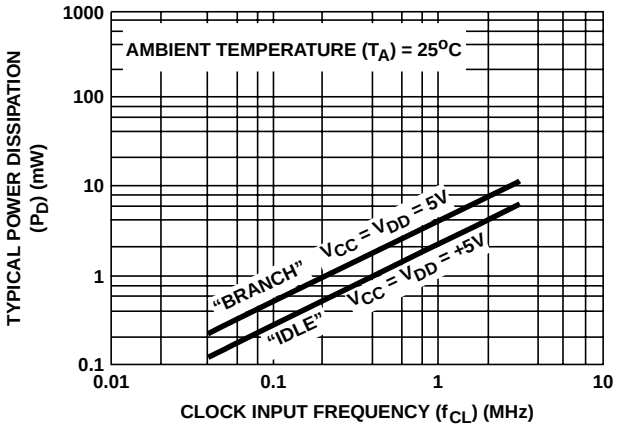


FIGURE 7. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

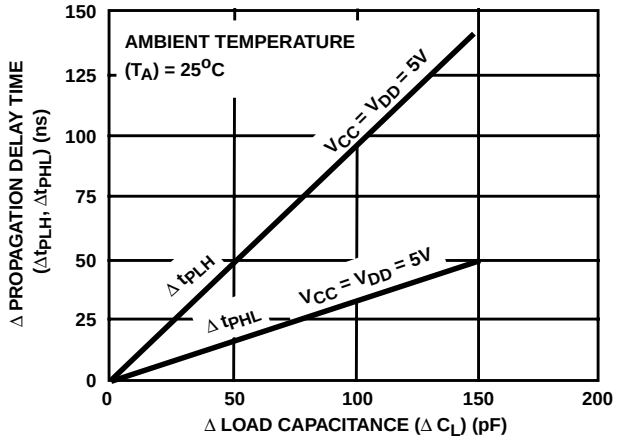


NOTES:

9. Idle = "00" at M (0000)
10. Branch = "3707" at M (8107)

FIGURE 8. TYPICAL POWER DISSIPATION AS A FUNCTION OF CLOCK FREQUENCY FOR BRANCH INSTRUCTION AND IDLE INSTRUCTION

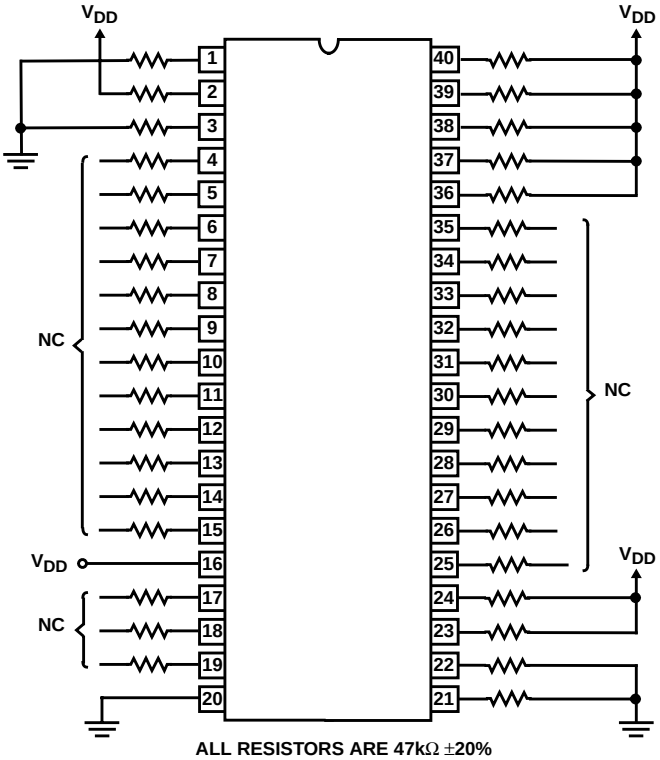
Performance Curves (Continued)



NOTE: Any output except $\overline{XTAL}$.

FIGURE 9. TYPICAL CHANGE IN PROPAGATION DELAY AS A FUNCTION OF A CHANGE IN LOAD CAPACITANCE

Burn-In Circuit



ALL RESISTORS ARE 47kΩ ±20%

TYPE	V_{DD}	TEMPERATURE	TIME
CDP1802AC	7V	+125°C	160 Hours

FIGURE 10. BIAS/STATIC BURN-IN CIRCUIT