intersil

CDP1823C/3

High-Reliability CMOS 128-Word x 8-Bit Static RAM

March 1997

Features

- For Applications in Aerospace, Military, and Critical Industrial Equipment
- Compatible with CDP1800-Series Microprocessors at Maximum Speed
- Interfaces with CDP1800-Series Microprocessors without Additional Components
- Fast Access Time
- At V_{DD} = 5V, +25°C 275ns
- Single Voltage Supply
- Common Data Inputs and Outputs
- Multiple Chip Select Inputs to Simplify Memory System Expansion
- High Noise Immunity . . . . . 30% of V_{DD}
- Memory Retention for Standby Battery Voltage Down to 2V at 25°C
- Latch-Up-Free Transient Radiation Tolerance

Ordering Information

PACKAGE	TEMP. RANGE	PART NUMBER (5V)	PKG. NO.
SBDIP	-55°C to +125°C	CDP1823CD3	D24.6

Description

The CDP1823C/3 is a 128 word x 8-bit CMOS/SOS static random access memory. It is compatible with the CDP1802, CDP1804, CDP1805, and CDP1806 microprocessors, and will interface directly without additional components. The CDP1823C has a recommended operating voltage range of 4V to 6.5V.

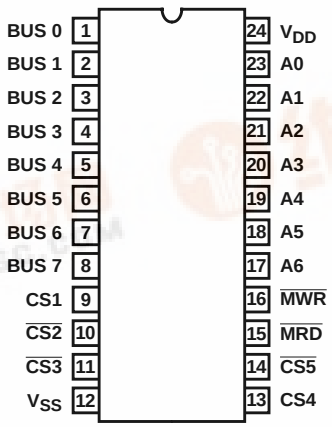
The CDP1823C memory has 8 common data input and data output terminals for direct connection to a bidirectional data bus and is operated from a single voltage supply. Five chip select inputs are provided to simplify memory system expansion. In order to enable the CDP1823C, the chip select inputs $\overline{CS2}$, $\overline{CS3}$, and $\overline{CS5}$ require a low input signal, and the chip select inputs CS1 and CS4 require a high input signal.

The $\overline{MRD}$ signal enables all 8 output drivers when in the low state and should be in a high state during a write cycle.

After valid data appear at the output, the address inputs may be changed immediately. Output data will be valid until either the $\overline{MRD}$ signal goes high, the device is deselected, or t_{AA} (access time) after address changes.

Pinout

CDP1823C/3
(SBDIP)
TOP VIEW



OPERATIONAL MODES

FUNCTION	$\overline{MRD}$	$\overline{MWR}$	CS1	$\overline{CS2}$	$\overline{CS3}$	CS4	$\overline{CS5}$	BUS TERMINAL STATE
Read	0	X	1	0	0	1	0	Storage State of Addressed Word
Write	1	0	1	0	0	1	0	Input High Impedance
Standby	1	1	1	0	0	1	0	High Impedance
Not Selected	X X X X X	X X X X X	0 X X X X	X 1 X X X	X X 1 X X	X X X 0 X	X X X X 1	High Impedance

NOTE:

1. Logic 1 = High, Logic 0 = Low, X = Don't Care.

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1823C/3 . . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input. . . . . ±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
SBDIP Package	60	17

Maximum Operating Temperature Range (T_A) . . . . -55^oC to $+125^oC$
Maximum Storage Temperature Range (T_{STG}) . . . -65^oC to $+150^oC$
Maximum Lead Temperature (During Soldering) . . . . . $+265^oC$
Maximum Junction Temperature . . . . . $+150^oC$

Recommended Operating Conditions

At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	LIMITS MIN	LIMITS MAX	UNITS
Supply Voltage Range	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V

Static Electrical Specifications

V_{DD} = 5V ±5%

PARAMETER		CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS -55°C, +25°C MIN	LIMITS -55°C, +25°C MAX	LIMITS +125°C MIN	LIMITS +125°C MAX	UNITS
Quiescent Device Current (Note 1)	I_{DD}	-	0, 5	5	-	270	-	1000	µA
Output Low (Sink) Current (Note 1)	I_{OL}	0.4	0, 5	5	2.7	-	1.5	-	mA
Output High (Source) Current (Note 1)	I_{OH}	4.6	0, 5	5	-	-1.3	-	-0.7	mA
Output Voltage Low-Level	V_{OL}	-	0, 5	5	-	0.1	-	0.1	V
Output Voltage High-Level	V_{OH}	-	0, 5	5	V_{DD} - 0.1	-	V_{DD} - 0.1	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	0.3 V_{DD}	-	0.3 V_{DD}	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	0.7 V_{DD}	-	0.7 V_{DD}	-	V
Input Leakage Current (Note 1)	I_{IN}	-	0, 5	5	-	±2.6	-	±10	µA
Operating Current (Note 1)	I_{DD1}	-	0, 5	5	-	5	-	10	mA
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	±2.6	-	±10	µA
Input Capacitance	C_{IN}	-	-	-	-	7.5	-	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	15	-	15	pF

NOTE:

1. Limits designate 100% testing, all other limits are designer's parameters under given test conditions and do not represent 100% testing.

Read Cycle Dynamic Electrical Specifications

t_R, t_F = 10ns, C_L = 50pF

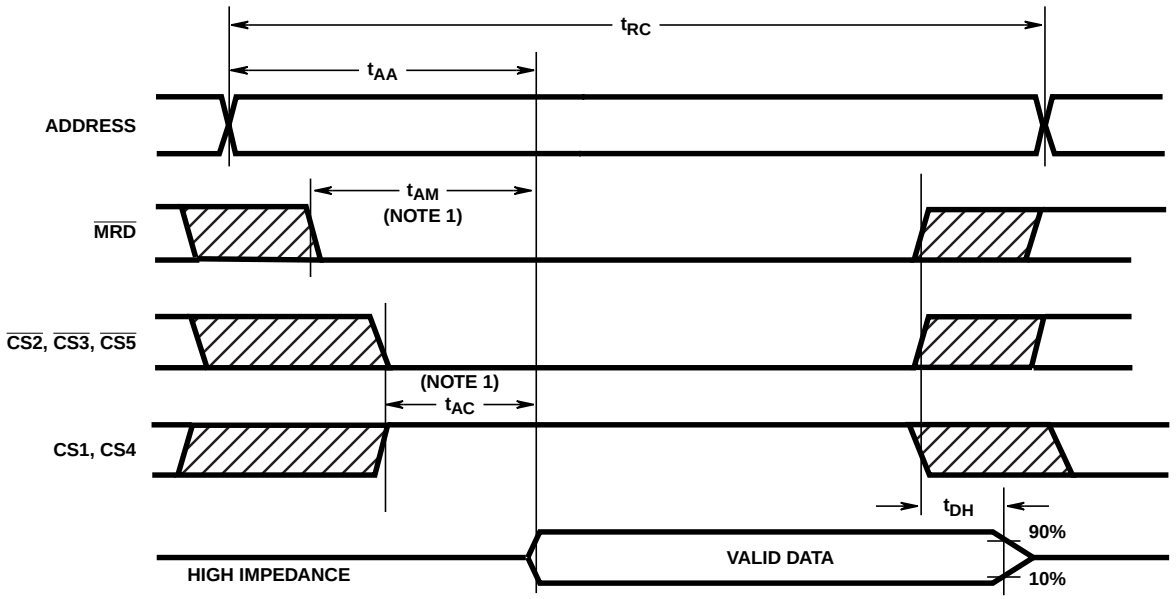
PARAMETER	SYMBOL	V_{DD} (V)	LIMITS +25°C, -55°C MIN	LIMITS +25°C, -55°C MAX	LIMITS +125°C MIN	LIMITS +125°C MAX	UNITS
Read Cycle	t_{RC}	5	360	-	505	-	ns
Access Time from Address Change (Note 1)	t_{AA}	5	-	360	-	505	ns
Access Time from Chip Select	t_{AC}	5	-	360	-	505	ns

Read Cycle Dynamic Electrical Specifications t_R, t_F = 10ns, C_L = 50pF **(Continued)**

PARAMETER	SYMBOL	V_{DD} (V)	LIMITS				UNITS
			+25°C, -55°C		+125°C		
			MIN	MAX	MIN	MAX	
Access Time from $\overline{MRD}$ (Note 1)	t_{AM}	5	-	310	-	435	ns
Data Hold Time After Read	t_{DH}	5	50	-	70	-	ns

NOTE:

1. Limits designate 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing.



NOTES:

1. Minimum timing for valid data output. Longer times will initiate an earlier but invalid output.
2. $\overline{MWR}$ is high during read operation. Timing measurement reference is $0.5V_{DD}$.

FIGURE 1. READ CYCLE TIMING DIAGRAM

Write Cycle Dynamic Electrical Specifications t_R, t_F = 10ns, C_L = 50pF

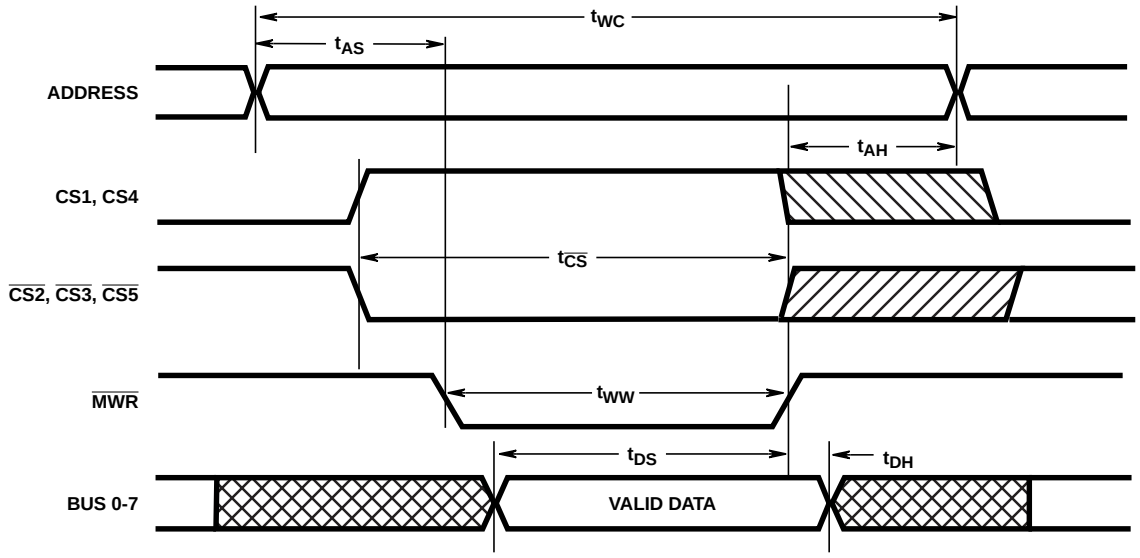
PARAMETER	SYMBOL	V_{DD} (V)	LIMITS				UNITS
			+25°C, -55°C		+125°C		
			(NOTE 2) MIN	MAX	(NOTE 2) MIN	MAX	
Write Cycle	t_{WC}	5	280	-	400	-	ns
Address Setup Time (Note 1)	t_{AS}	5	70	-	100	-	ns
Address Hold Time	t_{AH}	5	70	-	100	-	ns
Write Pulse Width (Note 1)	t_{WW}	5	140	-	200	-	ns
Data to $\overline{MWR}$ Setup Time (Note 1)	t_{DS}	5	70	-	100	-	ns

Write Cycle Dynamic Electrical Specifications t_R, t_F = 10ns, C_L = 50pF **(Continued)**

PARAMETER	SYMBOL	V_{DD} (V)	LIMITS +25°C, -55°C (NOTE 2) MIN	+25°C, -55°C MAX	+125°C (NOTE 2) MIN	+125°C MAX	UNITS
Data Hold Time from $\overline{MWR}$ (Note 1)	t_{DH}	5	50	-	70	-	ns
Chip Select Setup	$t_{\overline{CS}}$	5	210	-	300	-	ns

NOTES:

1. Limits designate 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing.
2. Minimum timing to allow the indicated function to occur.



NOTE:

1. $\overline{MRD}$ must be high during write operation.

FIGURE 2. WRITE CYCLE TIMING WAVEFORMS

Data Retention Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_{DR} (V)	TEST CONDITIONS V_{DD} (V)	LIMITS +25°C, -55°C MIN	+25°C, -55°C MAX	+125°C MIN	+125°C MAX	UNITS
Minimum Data Retention Voltage (Note 1)	V_{DR}	-	-	-	2	-	2.5	V
Data Retention Quiescent Current	I_{DD}	2	-	-	100	-	400	µA
Chip Deselect to Data Retention Time	t_{CDR}	-	5	450	-	650	-	ns
Recovery to Normal Operation Time	t_{RC}	-	5	450	-	650	-	ns

NOTE:

1. Limits designate 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

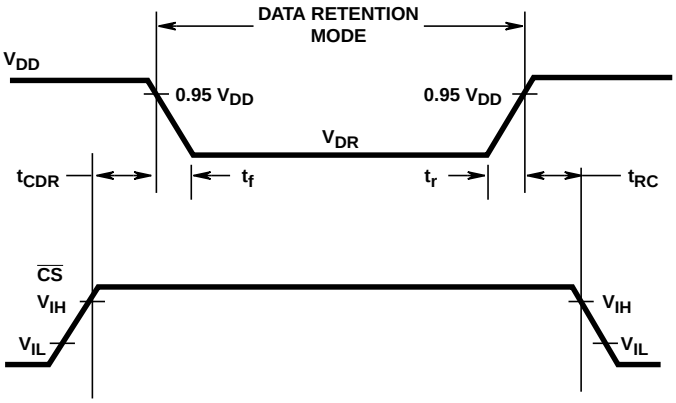
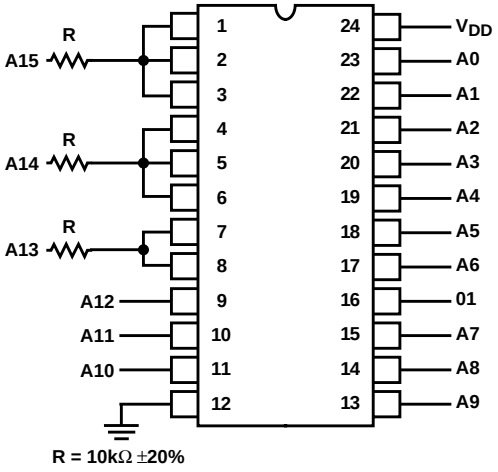
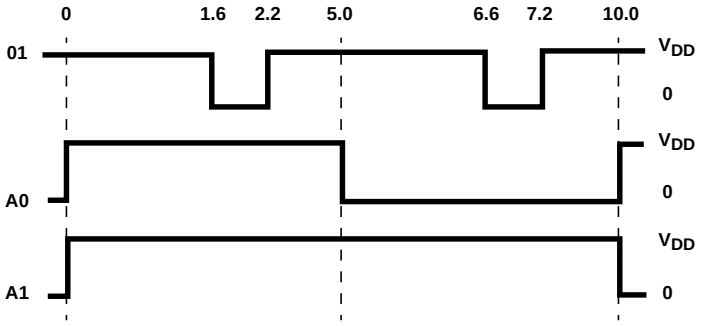


FIGURE 3. LOW V_{DD} DATA RETENTION WAVEFORMS



PACKAGE	TEMPERATURE	DURATION	V_{DD}
D	125^{O}C	160 Hrs	7V



NOTE:

1. A1 - A11 are division by 2 based on A0.

FIGURE 4. DYNAMIC/OPERATING BURN-IN CIRCUIT AND TIMING DIAGRAM

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.