intersil

CDP1826C

CMOS 64-Word x 8-Bit Static RAM

March 1997

Features

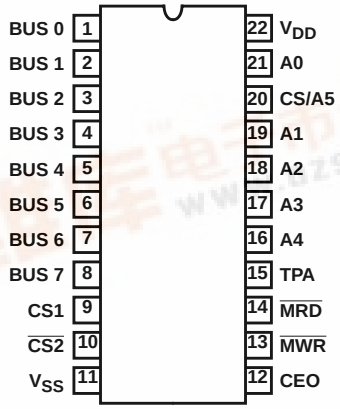
- **Ideal for Small, Low-Power RAM Memory Requirements in Microprocessor and Microcomputer Applications**
- **Interfaces with CDP1800-Series Microprocessors Without Additional Address Decoding**
- **Daisy Chain Feature to Further Reduce External Decoding Needs**
- **Multiple Chip-Select Inputs for Versatility**
- **Single Voltage Supply**
- **No Clock or Precharge Required.**

Ordering Information

PACKAGE	TEMP. RANGE	PART NUMBER	PKG. NO.
PDIP	-40^{o}C to +85^{o}C	CDP1826CE	E22.4

Pinout

CDP1826C (PDIP)
TOP VIEW



Description

The CDP1826C is a general purpose, fully static, 64-word x 8-bit random-access memory, for use in CDP1800-series or other microprocessor systems where minimum component count and/or price performance and simplicity in use are desirable.

The CDP1826C has 8 common data input and data-output terminals with three-state capability for direct connection to a standard bidirectional data bus. Two chip-select inputs - CS1 and $\overline{CS2}$ - are provided to simplify memory-system expansion. An additional select pin, CS/A5, is provided to enable the CDP1826C to be selected directly from the CDP1800 multiplexed address bus without additional latching or decoding. In an 1800 system, the CS/A5 pin can be tied to any MA address line from the CDP1800 processor. A TPA input is provided to latch the high-order bit of this address line as a chip-select for the CDP1826C. If this CS/A5 input is latched high, and if CS = 1 and $\overline{CS2}$ = 0 at the appropriate time in the memory cycle, the CDP1826C will be enabled for writing or reading. In a non-1800 system, the TPA pin can be tied high, and the CS/A5 pin can be used as a normal address input.

The six input-address buffers are gated with the chip-select function to reduce standby current when the device is deselected, as well as to provide for a simplified power down mode by reducing address buffer sensitivity to long fall times from address drivers which are being powered down.

Two memory control signals, $\overline{MRD}$ and $\overline{MWR}$, are provided for reading from the writing to the CDP1826C. The logic is designed so that $\overline{MWR}$ overrides $\overline{MRD}$, allowing the chip to be controlled from a single R/$\overline{W}$.

A CHIP ENABLE OUTPUT is provided for daisy-chaining to additional memories or I/O devices. This output is high whenever the chip-select function selects the CDP1826C, which deselects any other chip which has its $\overline{CS}$ input connected to the CDP1826C CEO output. The connected chip is selected when the CDP1826C is deselected and the $\overline{MRD}$ input is low. Thus, the CEO is only active for a read cycle and can be setup so that a CEO of another device can feed the $\overline{MRD}$ of the CDP1826C, which in turn selects a third chip in the daisy chain.

The CDP1826C has a recommended operating voltage of 4.5V to 5.5V and is supplied in 22 lead dual-in-line plastic packages (E suffix). The CDP1826C is also available in chip form (H suffix).

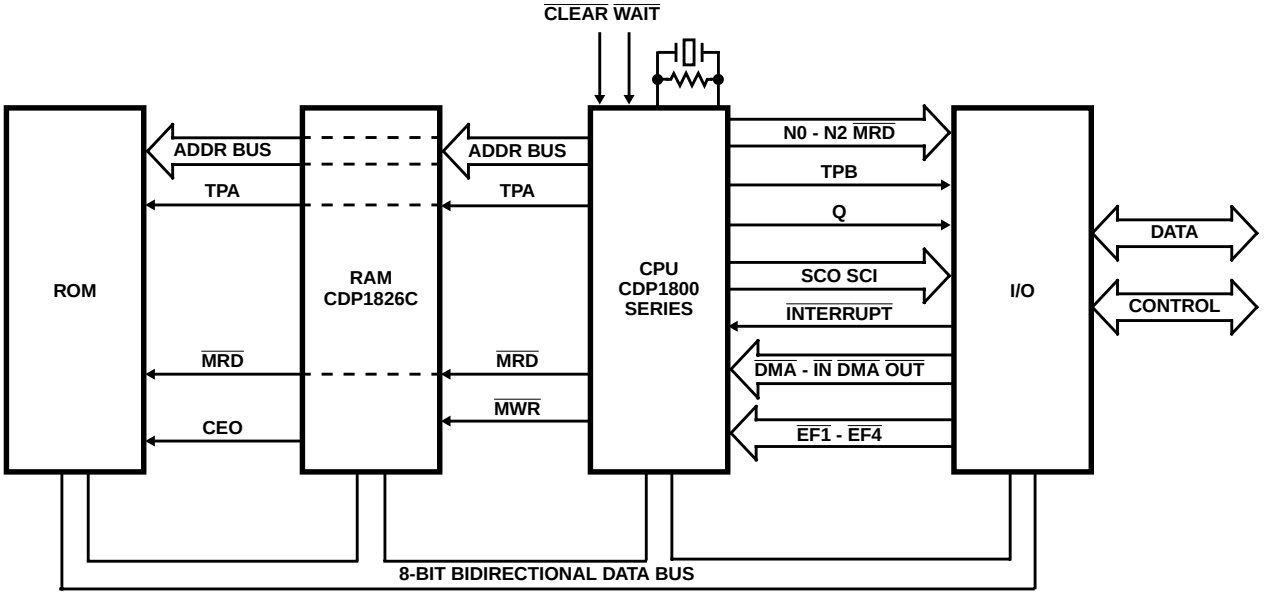


FIGURE 1. TYPICAL CDP1802 MICROPROCESSOR SYSTEM

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1826C. . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input. . . . . ±10mA
Power Dissipation Per Package (P_D)
T_A = -40°C to +60°C (Package Type E) 500mW
T_A = +60°C to +85°C (Package Type E). . . . . Derate Linearly at 12mW/°C to 200mW
T_A = -55°C to +100°C (Package Type D) 500mW
T_A = +100°C to +125°C (Package Type D). . . . Derate Linearly at 12mW/°C to 200mW

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	75	N/A

Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range
(All Package Types) 100mW
Operating Temperature Range (T_A)
Package Type D. . . . . -55°C to +125°C
Package Type E. . . . . -40°C to +85°C
Storage Temperature Range (T_{STG}). . . . . -65°C to +150°C
Lead Temperature (During Soldering)
At distance 1/16 ±1/32 In. (1.59 ±0.79mm)
from case for 10s max . . . . . +265°C

Recommended Operating Conditions

At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	SYMBOL	CDP1826C		UNITS
		MIN	MAX	
DC Operating Voltage Range		4	6.5	V
Input Voltage Range		V_{SS}	V_{DD}	V
Input Signal Rise or Fall Time, V_{DD} = 5V	t_R, t_F	-	10	µs

Static Electrical Specifications

At T_A = -40°C to +85°C, V_{DD} = 5V ±5%, Except as Noted:

PARAMETER		SYMBOL	CONDITIONS		LIMITS			
					CDP1826C			
			V_O (V)	V_{IN} (V)	MIN	(NOTE 1) TYP	MAX	UNITS
Quiescent Device Current		I_{DD}	-	0, V_{DD}	-	5	50	µA
Output Low (Sink) Current	BUS	I_{OL}	0.4	0, V_{DD}	1.6	3.2	-	mA
	CEO		0.4	0, V_{DD}	0.8	1.6	-	mA
Output High (Source) Current	BUS	I_{OH}	V_{DD} -0.4	0, V_{DD}	-1.0	-1.5	-	mA
	CEO		V_{DD} -0.4	0, V_{DD}	-0.6	-1.0	-	mA
Output Voltage Low-Level		V_{OL}	-	0, V_{DD}	-	0	0.1	V
Output Voltage High-Level		V_{OH}	-	0, V_{DD}	V_{DD} -0.1	V_{DD}	-	V
Input Low Voltage		V_{IL}	-	-	-	-	1.5	V
Input High Voltage		V_{IH}	-	-	3.5	-	-	V
Input Leakage Current		I_{IN}	Any Input	0, V_{DD}	-	±0.1	±1	µA
Operating Device Current (Note 2)		I_{OPER}	-	0, V_{DD}	-	5	10	mA
Three-State Output Leakage Current		I_{OUT}	0, V_{DD}	0, V_{DD}	-	±0.1	±1	µA
Input Capacitance		C_{IN}	-	-	-	5	7.5	pF
Output Capacitance		C_{OUT}	-	0, V_{DD}	-	10	15	pF

NOTES:

1. Typical values are for T_A = +25°C and nominal V_{DD}.
2. Outputs open circuited; Cycle time = 1µs.

Signal Descriptions

A0 - A4, CS/A5 (Address Inputs): These inputs must be stable prior to a write operation, but may change asynchronously during Read operations.

In an 1800 system, the multiplexed high-order address bit at pin CS/A5 can be latched at the end of TPA. A high level will provide a valid chip select for the CDP1826C. The low-order address bit which appears after TPA is used for data word selection. In non-1800 systems, TPA can be tied high to disable the latch and allow the CS/A5 pin to function as a normal address input.

BUS 0 - BUS 7: 8-bit three-state common input/output data bus.

TPA: High-order address strobe input. The high-order address bit at input CS/A5 is latched on the high-to-low transition of the TPA input. Tie TPA high to disable the CS/A5 latch feature.

CS1, $\overline{CS2}$ (Chip Selector): Either chip select (CS1 or $\overline{CS2}$), when not valid, powers down the chip, disables READ and WRITE functions, and gates off the address and output buffers.

$\overline{MRD}$, $\overline{MWR}$: Read and Write control signals. $\overline{MWR}$ overrides $\overline{MRD}$, allowing the CDP1826C to be controlled from a single R/$\overline{W}$ line.

CEO (Chip Enable Output): Allows daisy chaining to additional memories. CEO is high whenever the CDP1826C is selected. CEO is only active (low) for a Read cycle with the CDP1826C deselected and the $\overline{MRD}$ input low.

V_{DD}, V_{SS}: Power supply connections.

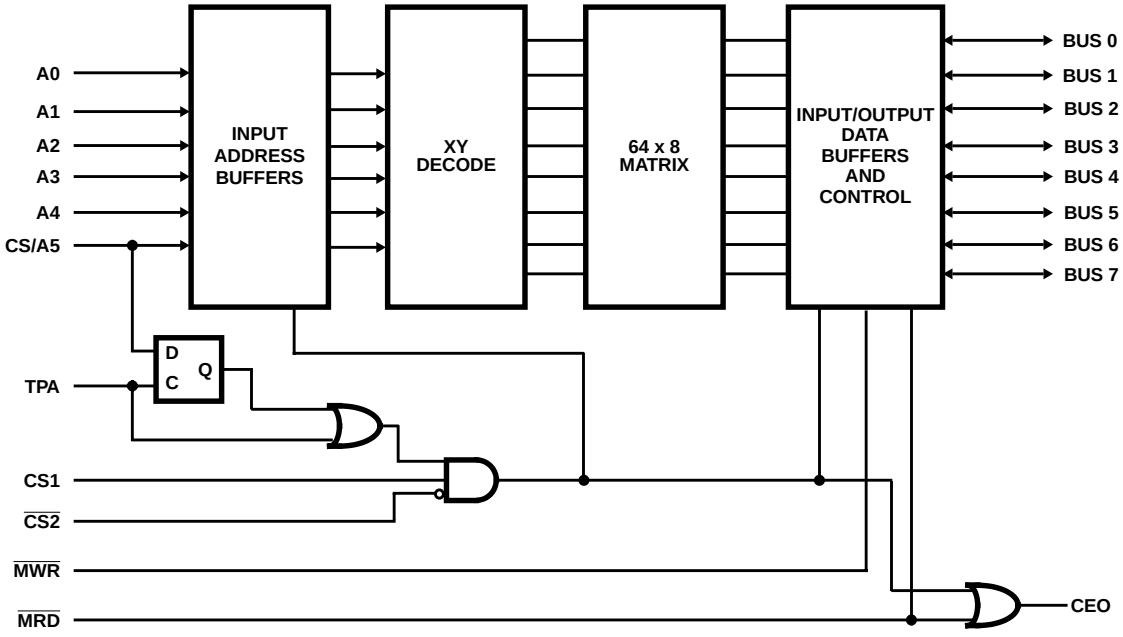
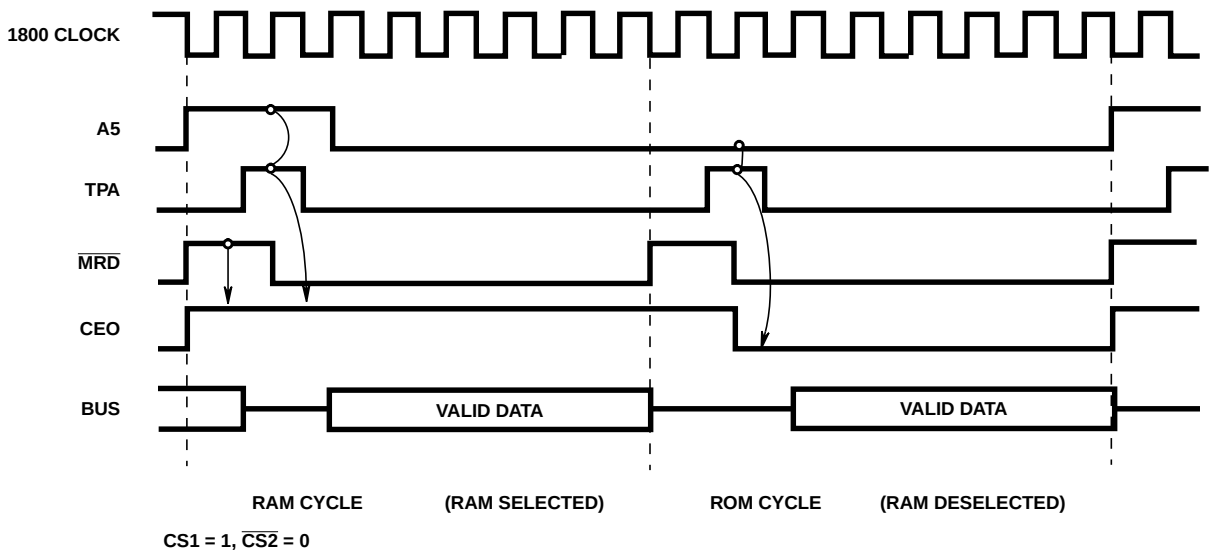


FIGURE 2. FUNCTIONAL DIAGRAM



OPERATING MODES

	FUNCTION	$\overline{MRD}$	$\overline{MWR}$	CS1 • $\overline{CS2}$	TPA	(NOTE 1) CS/A5	CEO
CDP1800 Mode	Write	X	O	I	⎍	I	I
	Read	O	I	I	⎍	I	I
	Deselect	I	I	I	⎍	I	I
	Deselect	I	X	O	X	X	I
	Deselect	O	X	O	X	X	O
	Deselect	I	X	X	⎍	O	I
	Deselect	O	X	X	⎍	O	O
Non-CDP1800 Mode	Write	X	O	I	I	X	I
	Read	O	I	I	I	X	I
	Deselect	I	I	I	I	X	I
	Deselect	I	X	O	I	X	I
	Deselect	O	X	O	I	X	O

NOTE:

1. For CDP1800 Mode, refers to high order memory address bit level at time when TPA ⎍ transition takes place.

FIGURE 3. CHIP ENABLE OUTPUT TIMING WAVEFORMS FOR CDP1800 BASED SYSTEMS

Dynamic Electrical Specifications At T_A = -40 to +85^{o}C, V_{DD} = 5V ±5%, Input t_R, t_F = 10ns; C_L = 50pF and 1 TTL Load

PARAMETER		LIMITS CDP1826C (NOTE 1) MIN	(NOTE 2) TYP	MAX	UNITS
READ - CYCLE TIMES (FIGURES 4 AND 5)					
Address to TPA Setup	t_{ASH}	100	-	-	ns
Address to TPA Hold	t_{AH}	100	-	-	ns
Access from Address Change	T_{AA}	-	500	1000	ns
TPA Pulse Width	t_{PAW}	200	-	-	ns
Output Valid from $\overline{MRD}$	t_{AM}	-	500	1000	ns
Access from Chip Select	t_{AC}	-	500	1000	ns
CEO Delay from TPA ↘ Edge	t_{CA}	-	150	300	ns
$\overline{MRD}$ to CEO Delay	t_{MC}	75	-	-	ns
Output High Z from Invalid $\overline{MRD}$	t_{RHZ}	-	-	125	ns
Output High Z from Chip Deselect	t_{SHZ}	-	-	225	ns

NOTES:

1. Time required by a limit device to allow tor the indicated function.
2. Typical values are or T_A = 25^{o}C and nominal V_{DD}.

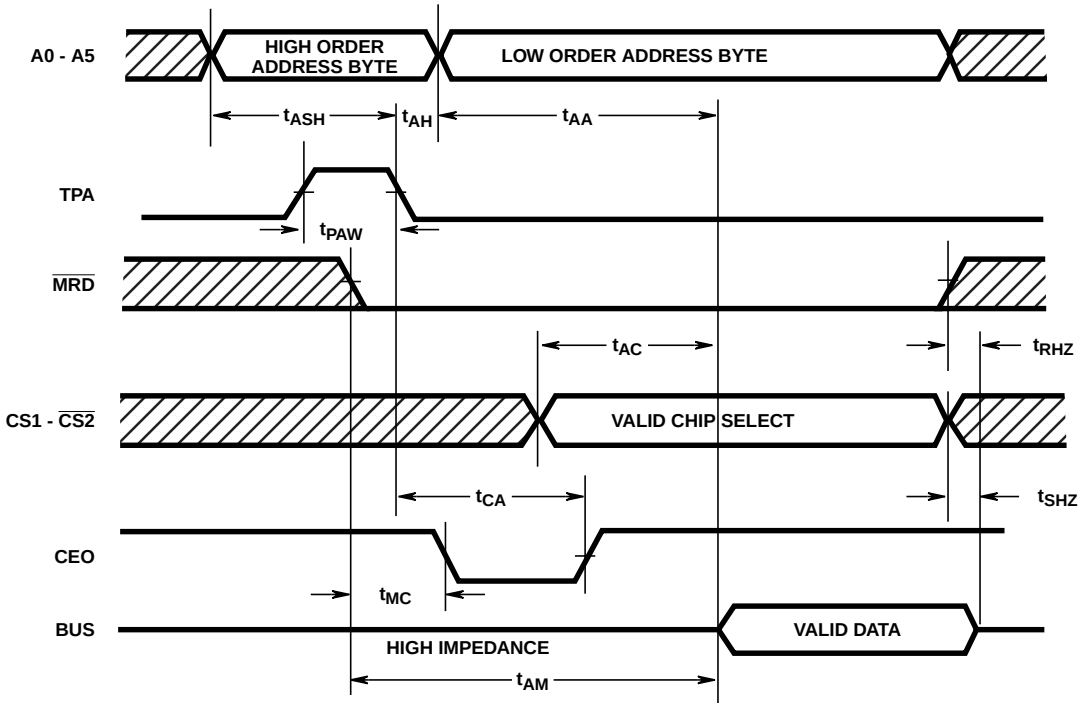


FIGURE 4. TIMING WAVEFORMS FOR READ CYCLE 1

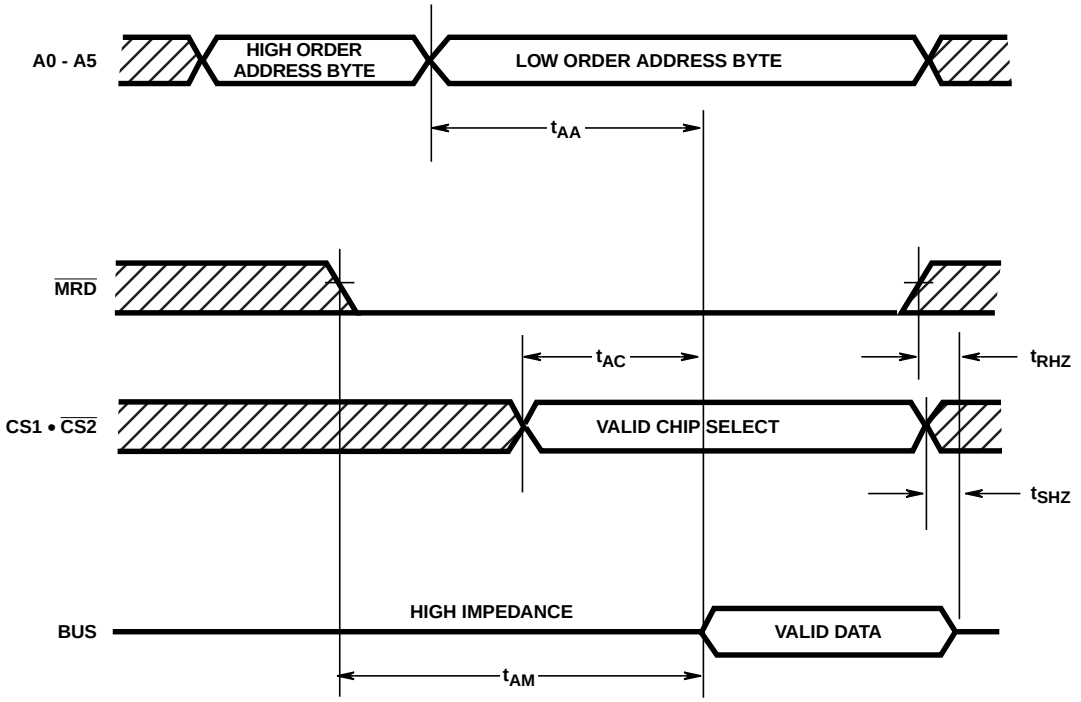


FIGURE 5. TIMING WAVEFORMS FOR READ-CYCLE 2 (TPA HIGH)

Dynamic Electrical Specifications At T_A = -40 to +85^{o}C, V_{DD} = 5V ± 5%,Input t_R, t_F = 10ns; C_L = 50pF and 1 TTL Load

PARAMETER		LIMITS CDP1826C (NOTE 1) MIN	(NOTE 2) TYP	MAX	UNITS
WRITE - CYCLE TIMES (FIGURES 6 AND 7)					
Address to TPA Setup, High Byte	t_{ASH}	100	-	-	ns
Address to TPA Hold	t_{AH}	100	-	-	ns
Address Setup, Low Byte	T_{ASL}	500	250	-	ns
TPA Pulse Width	t_{PAW}	200	-	-	ns
Chip Select Setup	t_{CS}	700	350	-	ns
Write Pulse Width	t_{WW}	300	200	-	ns
Write Recovery	t_{WR}	100	-	-	ns
Data Setup	t_{DS}	400	200	-	ns
Data Hold from End of $\overline{MWR}$	t_{DH1}	100	50	-	ns
Data Hold from End of Chip Select	t_{DH2}	125	50	-	ns

NOTES:

1. Time required by a limit device to allow tor the indicated function.
2. Typical values are for T_A = 25^{o}C and nominal V_{DD}.

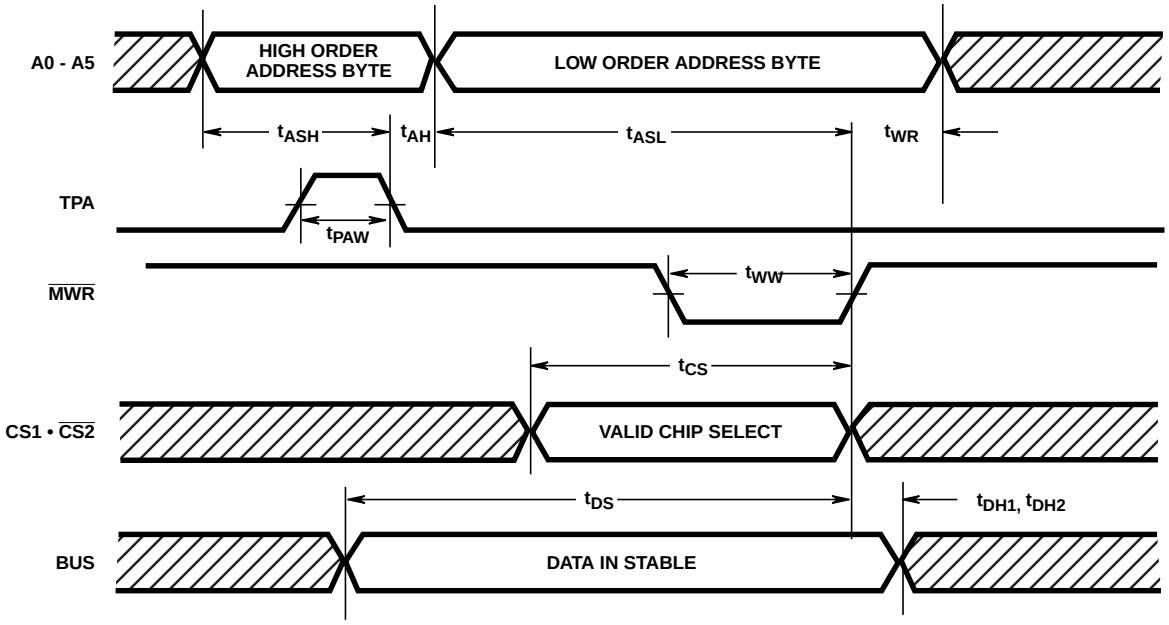


FIGURE 6. TIMING WAVEFORMS FOR WRITE-CYCLE 1

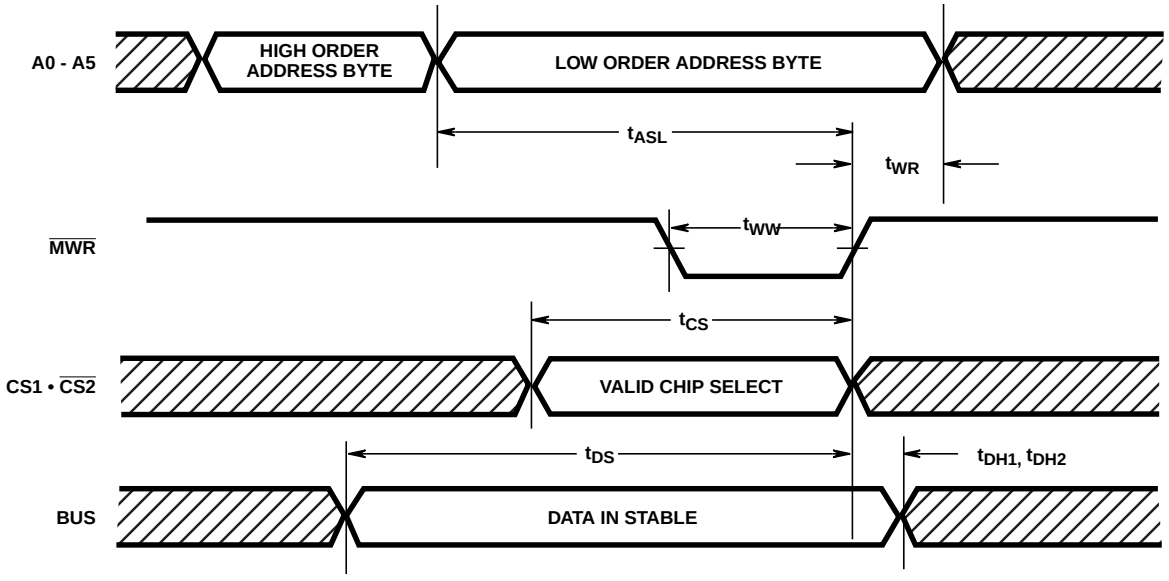


FIGURE 7. TIMING WAVEFORMS FOR WRITE-CYCLE 2 (TPA = HIGH)

Data Retention Specifications At T_A = -40 to +85^{o}C, see Figure 8

PARAMETER	TEST CONDITIONS V_{DR} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	LIMITS CDP1826C MAX	UNITS
Minimum Data Retention Voltage V_{DR}	-	-	-	2	2.5	V
Data Retention Quiescent Current t_{DD}	2.5	-	-	5	25	µA
Chip Deselect to Data Retention Time t_{CDR}	-	5	600	-	-	ns
Recovery to Normal Operation Time t_{RC}	-	5	600	-	-	ns
V_{DD} to V_{DR} Rise and Fall Time t_R, t_F	2.5	5	1	-	-	µA

NOTE:

1. Typical values are or T_A = 25^{o}C and nominal V_{DD}.

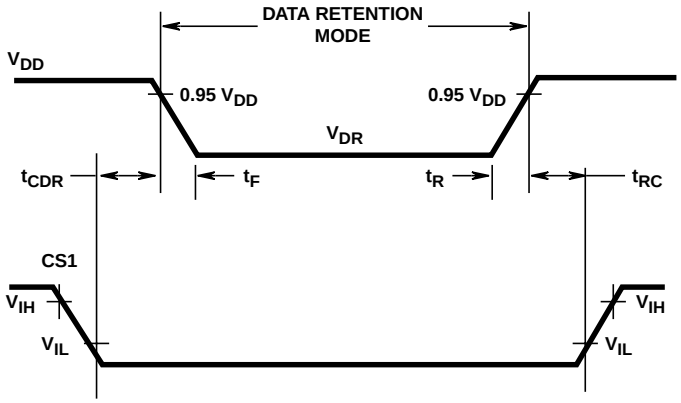


FIGURE 8. LOW V_{DD} DATA RETENTION TIMING WAVEFORMS

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029