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CDP1851, CDP1851C

March 1997

CMOS Programmable I/O Interface

Features

- **20 Programmable I/O Lines**
- **Programmable for Operation in Four Modes:**
  - **Input**
  - **Output**
  - **Bidirectional**
  - **Bit-programmable**
- **Operates in Either I/O or Memory Space**

Ordering Information

PACKAGE	TEMP. RANGE	5V	10V	PKG. NO.
PDIP	-40°C to +85°C	CDP1851CE	CDP1851E	E40.6
Burn-In		CDP1851CEX	-	E40.6
SBDIP	-40°C to +85°C	CDP1851CD	-	D40.6
Burn-In		CDP1851CDX	CDP1851DX	D40.6

Description

THE CDP1851 and CDP1851C are CMOS programmable two-port I/Os designed for use as general-purpose I/O devices. They are directly compatible with CDP1800-series microprocessors functioning at maximum clock frequency. Each port can be programmed in either byte-I/O or bit-programmable modes for interfacing with peripheral devices such as printers and keyboards.

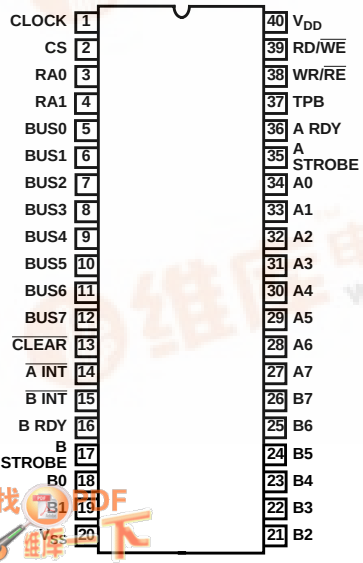
Both ports A and B can be separately programmed to be 8-bit input or output ports with handshaking control lines, RDY and STROBE. Only port A can be programmed to be a bidirectional port. This configuration provides a means for communicating with a peripheral device or microprocessor system on a single 8-bit bus for both transmitting and receiving data. Handshaking signals are provided to maintain proper bus access control. Port A handshaking lines are used for input control and port B handshaking lines are used for output; therefore port B must be in the bit-programmable mode where handshaking is not used.

Ports A and B can be separately bit programmed so that each individual line can be designated as an input or output line. The handshaking lines may also be individually programmed as input or output when port A is not in bidirectional mode.

The CDP1851 has a supply-voltage range of 4V to 10.5V, and the CDP1851C has a range of 4V to 6.5V. Both types are supplied in 40-lead dual-in-line plastic (E suffix) or hermetic ceramic (D suffix) packages. The CDP1851C is also available in chip form (H suffix).

Pinout

CDP1851, CDP1851C
(PDIP, SBDIP)
TOP VIEW



CDP1851 Programming Modes

MODE	(8) PORT A DATA PINS	(2) PORT A HANDSHAKING PINS	(8) PORT B DATA PINS	(2) PORT B HANDSHAKING PINS
Input	Accept Input Data	READY, STROBE	Accept Input Data	READY, STROBE
Output	Output Data	READY, STROBE	Output Data	READY, STROBE
Bidirectional (Port A Only)	Transfer Input/Output Data	Input Handshaking for Port A	Must be Previously Set to Bit-Programmable Mode	Output Handshaking for Port A
Bit-Programmable	Programmed Individually as Inputs or Outputs	Programmed Individually as Inputs or Outputs	Programmed Individually as Inputs or Outputs	Programmed Individually as Inputs or Outputs

Absolute Maximum Ratings

DC Supply-Voltage Range, (V_{DD})
(Voltage Referenced to V_{SS} Terminal)
CDP1851 . . . . . -0.5 to+11V
CDP1851C . . . . . -0.5 to +7V
Input Voltage Range, All Inputs . . . . . -0.5 to V_{DD} +0.5V
DC Input Current, Any One Input. . . . . ±10mA
Device Dissipation Per Output Transistor
For T_A = Full Package-Temperature Range
(All Package Type) 40mW
Operating-Temperature Range (T_A)
Package Type D, H . . . . . -55°C to +125°C
Package Type E . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	50	N/A
SBDIP Package	36	12

Maximum Storage Temperature Range (T_{STG}) . . . . -65°C to +150°C
Maximum Lead Temperature (During Soldering)
At Distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from Case for 10s max . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Operating Conditions

At T_A = Full Package-Temperature Range. For Maximum Reliability, Operating Conditions Should be Selected so that Operation is Always within the Following Ranges:

PARAMETER	LIMITS				UNITS
	CDP1851		CDP1851C		
	MIN	MAX	MIN	MAX	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

Functional Diagram

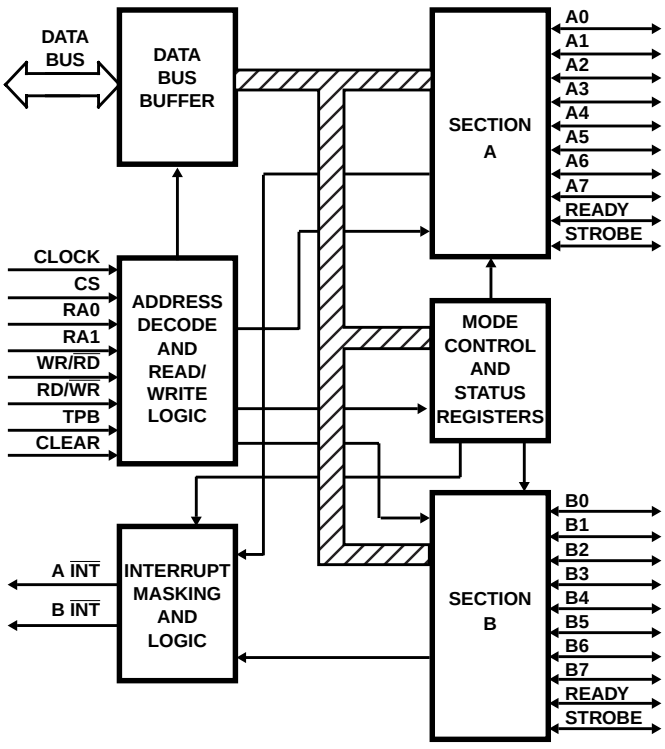


FIGURE 1. FUNCTIONAL DIAGRAM FOR CDP1851 AND CDP1851C

Static Electrical Specifications At T_A = -40°C to +85°C, V_{DD} 5%, Unless Otherwise Specified

PARAMETER		CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS CDP1851 MIN	LIMITS CDP1851 (NOTE1) TYP	LIMITS CDP1851 MAX	LIMITS CDP1851C MIN	LIMITS CDP1851C (NOTE1) TYP	LIMITS CDP1851C MAX	UNITS
Quiescent Device Current	I_{DD}	-	0, 5	5	-	0.01	50	-	0.02	200	µA
		-	0, 10	10	-	1	200	-	-	-	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	1.6	3.2	-	1.6	3.2	-	mA
		0.5	0, 10	10	2.6	5.2	-	-	-	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-1.15	-2.3	-	-1.15	-2.3	-	mA
		9.5	0, 10	10	-2.6	-5.2	-	-	-	-	mA
Output Voltage Low-Level (Note 2)	V_{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage High Level (Note 2)	V_{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		0.5, 9.5	-	10	-	-	3	-	-	-	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	3.5	-	-	V
		0.5, 9.5	-	10	7	-	-	-	-	-	V
Input Leakage Current	I_{IN}	Any Input	0, 5	5	-	-	±1	-	-	±1	µA
			0, 10	10	-	-	±2	-	-	-	µA
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	-	±1	-	-	±1	µA
		0, 10	0, 10	10	-	-	±1	-	-	-	µA
Operating Current (Note 3)	I_{DD1}	-	0, 5	5	-	1.5	3	-	1.5	3	mA
		-	0, 10	10	-	6	12	-	-	-	mA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	-	10	15	pF

NOTES:

1. Typical values are for T_A = 25°C and nominal V_{DD}.
2. $I_{OL} = I_{OH}$ = 1µA
3. Operating current is measured at 200kHz for V_{DD} = 5V and 400kHz for V_{DD} = 10V, with open output (worst-case frequencies for CDP1802A system operating at maximum speed of 3.2MHz).

Functional Description

The CDP1851 has four modes of operation: input, output, bidirectional, and bit-programmable. Port A is programmable in all modes; port B is programmable in all but the bidirectional mode. A control byte must be loaded into the control register to program the ports. In the input and output modes, each port has two handshaking signals, STROBE and RDY. In the bidirectional mode, port A has four handshaking signals: A RDY and A STROBE for input, B RDY and B STROBE for output. If port A is programmed in the bidirectional mode, port B must be programmed in the bit-programmable mode. Each terminal of port A or B may be individually programmed for input or output in the bit-programmable mode. Since handshaking is not used in this mode, the RDY and STROBE lines may also be used for bit-programming if port A is not in the bidirectional mode.

Input Mode

When a peripheral device has data to input, it sends a STROBE pulse to the PIO. The leading edge of this pulse clears the RDY line, inhibiting further transmission from the peripheral. The trailing edge of the STROBE pulse latches the data into the PIO buffer register and also activates the INT line to signal the CPU to read this data. The INT pin can be wired to the INT pin of the CPU or the EF lines for polling. The CPU

then executes an input or a load instruction, depending on the mapping technique used. In either case the proper code must be asserted on the RAO, RA1, and CS lines to read the buffer register (see Table 6).

The $\overline{INT}$ line is deactivated on the leading edge of TPB. The trailing edge of TPB sets the RDY line to signal the peripheral that the port is ready to be loaded with new data. If RDY is low when the input mode is entered (i.e. after a reset), a "dummy" read must be done to set RDY high and signal the peripheral device that the port is ready to be loaded.

Output Mode

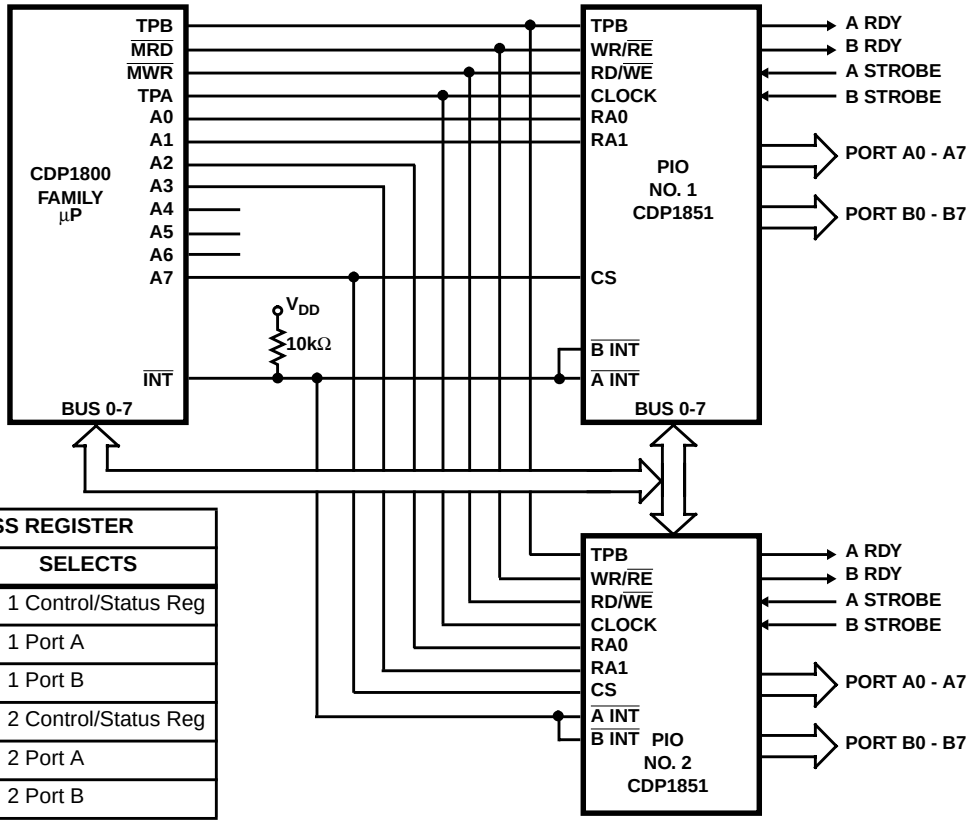
A peripheral STROBE pulse sent to the PIO generates an interrupt to signal the CPU that the peripheral device is ready for data. The CPU executes the proper output or store instruction. Data are then read from memory and placed on the bus. The data are latched into the port buffer at the end of the window when RE/$\overline{WE}$ = 0 and WR/$\overline{RE}$ = 1. The RDY line is also set at this time, indicating to the peripheral that there is data in the port buffer. The $\overline{INT}$ line is deactivated at the beginning of the window. After the peripheral reads valid port data, it can send another STROBE pulse, clearing the RDY line and activating the $\overline{INT}$ line as in the input mode.

Bidirectional Mode

This mode programs port A to function as both an input and output port. The bidirectional feature allows the peripheral to control port direction by using both sets of handshake signals. The port A handshaking pins are used to control input data from peripheral to PIO, while the port B handshaking pins are used to control output data from PIO to peripheral. Data are transferred in the same manner as the input and output modes. Since A INT is used for both input and output, the status register must be read to determine what condition caused A INT to be activated (see Table 5).

Bit-Programmable Mode

This mode allows individual bits of port A or port B to be programmed as inputs or outputs. To output data to bits programmed as outputs, the CPU loads a data byte into the 8-bit port as in the output mode (no handshaking). Only bits programmed for outputs latch this data. Data must be stable when reading from bits programmed as inputs, since the input bits do not latch. When the CDP1851 inputs data to the CPU the CPU also reads the output bits latched during the last output cycle. The RDY and STROBE lines may be used for I/O by using the STROBE/RDY I/O control byte in Table 2. An additional feature available in the bit-programmable mode is the ability to generate interrupts based on input/output byte combinations. These interrupts can be programmed to occur on logic conditions (AND, OR, NAND, and NOR) generated by the eight I/O lines of each port (The STROBE and RDY lines cannot generate interrupts).



ADDRESS REGISTER	
ADDRESS	**SELECTS**
8001	No. 1 Control/Status Reg
8002	No. 1 Port A
8003	No. 1 Port B
8004	No. 2 Control/Status Reg
8008	No. 2 Port A
800C	No. 2 Port B

FIGURE 2. MEMORY SPACE I/O. THIS CONFIGURATION ALLOWS UP TO FOUR CDP1851s TO OCCUPY MEMORY SPACE 8XXX WITH NO ADDITIONAL HARDWARE (A4-A5 AND A6-A7 ARE USED AS RA0 AND RA1 ON THE THIRD AND FOURTH PIO's)

Programming

Initialization and Controls

The CDP1851 PIO must be cleared by a low on the $\overline{\text{CLEAR}}$ input during power-on to set it for programming. Once programmed, modes can be changed without clearing except when exiting the bit-programmable mode. A low on the $\overline{\text{CLEAR}}$ input sets both ports to the input modes, disables interrupts, unmasks all bit-programmed interrupt bits, and resets the status register, A RDY, and B RDY.

Mode Setting

The control register must be sequentially loaded with the appropriate mode set control bytes in order as shown in Table 1 (i.e. input mode then output mode, etc.). Port A is set with the SET A bit = 1 and port B is set with the SET B bit = 1. If a port is set to the bit-programmable mode, the bit-programming control byte from Table 2 must be loaded. A bit is programmed for output with the I/O bit = 1 and for input with the I/O bit = 0. The STROBE and RDY lines may be programmed for input or output with the STROBE/RDY control byte of Table 2. Input data on the STROBE and RDY lines is detected by reading the status register. When using the STROBE or RDY lines for output, the control byte must be loaded every time output data is to be changed. To program logical conditions that will generate an interrupt, the interrupt control byte of Table 3 must be loaded. An interrupt mask of the eight I/O lines may be loaded next, if bit D4 (mask follows) of the interrupt control byte = 1. The I/O lines are masked if the corresponding bit of the interrupt mask register is 1, otherwise it is monitored. Any combination of masked bits are permissible, except all bits masked (mask = FF).

$\overline{\text{INT}}$ Enable Disable

To enable or disable the $\overline{\text{INT}}$ line in all modes, the interrupt ENABLE/DISABLE byte must be loaded (see Table 4). Interrupts can also be detected by reading the status register (see Table 5). All interrupts should be disabled when programming or false interrupts may occur. The $\overline{\text{INT}}$ outputs are open drain NMOS devices that allow wired O Ring (use 10K pull-up registers).

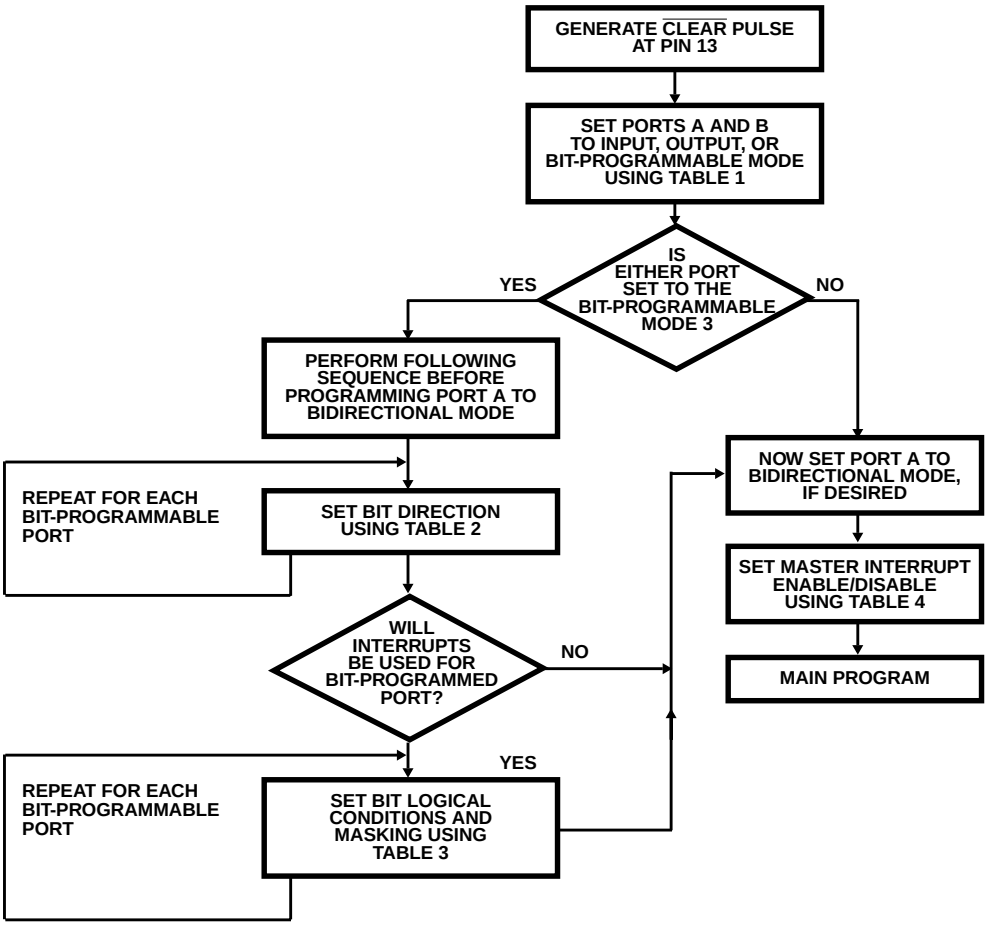


FIGURE 3. A FLOW CHART GUIDE TO CDP1851 MODE PROGRAMMING

NOTES:

1. STROBE/READY I/O Control Byte (Table 2) is also used to output data to STROBE and READY lines when bit-programmed.
2. Status register (Table 2) is used to input data from STROBE and READY lines when bit-programmed.
3. Interrupt status is also read from status register.

TABLE 1. (RA1 = 0, RA0 = 1)

(NOTE 1) **MODE SET**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Input	0	0	X	Set B	Set A	X	1	1
Output	0	1	X	Set B	Set A	X	1	1
Bit-Programmable	1	1	X	Set B	Set A	X	1	1
Bidirectional	1	0	X	X	Set A	X	1	1

NOTE:

1. Modes should be set in order as shown in Table 1.

If either port is set for bit-programmable mode, the two following control bytes should immediately follow:

TABLE 2. (RA1 = 0, RA0 = 1)

	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit-Programming (Note 1)	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
STROBE/RDY I/O Control (Notes 2 - 8)	D7	D6	D5	D4	D3	D2	D1	D0

NOTES:

1. Output = 1, Input = 0
2. (D1) 0 = Port A, 1 = Port B
3. (D2) 0 = No change to RDY line function, 1 = Change per bit (D6)
4. (D3) 0 = No change to STROBE line function, 1 = Change per bit (D7)
5. (D4) RDY line output data
6. (D5) STROBE line output data
7. (D6) RDY line used as:
   Output = 1
   Input = 0
8. (D7) STROBE line used as:
   Output = 1
   Input = 0

If interrupts will be used for either bit-programmed port, the following control bytes should be loaded.

TABLE 3. (RA1 = 0, RA0 = 1)

INTERRUPT CONTROL	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Logical Conditions and Mask	0	D6	D5	D4	D3	1	0	1

NOTES:

1. (D3) 0 = Port A, 1 = Port B
2. (D4) 0 = No change in mask, 1 = Mask follows (See Table 3A)
3. (D5)(D6) 0, 0 = NAND; 1, 0 = OR; 0, 1 = NOR; 1, 1 = AND

TABLE 3A. (RA1 = 0, RA0 = 1)

INTERRUPT CONTROL	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mask Register (If D4 = 1)	B7 Mask	B6 Mask	B5 Mask	B4 Mask	B3 Mask	B2 Mask	B1 Mask	B0 Mask

NOTE:

1. If Bn Mask = 1 then mask Bit (for n = 0 to 7)

TABLE 4. (RA1 = 0, RA0 = 1)

INTERRUPT CONTROL	7	6	5	4	3	2	1	0
Interrupt Enable/Disable	$\overline{INT}$ Enable	X	X	X	A/B	0	0	1

NOTES:

1. $\overline{INT}$ Enable = 1, $\overline{INT}$ Enabled
   = 0, $\overline{INT}$ Disabled
2. A/B = 0, Port A
   = 1, Port B

TABLE 5. (RA1 = 0, RA0 = 1)

	7	6	5	4	3	2	1	0
Status Register	D7	D6	D5	D4	D3	D2	D1	D0

NOTES:

1. All Modes
   (D0) $\overline{B\ INT}$ status (1 means set)
   (D1) $\overline{A\ INT}$ status (1 means set)
2. Bidirectional Mode Only
   (D2) 1 = $\overline{A\ INT}$ was caused by A STROBE
   (D3) 1 = $\overline{A\ INT}$ was caused by B STROBE
3. Bit-Programmable Mode
   (D4) A RDY input data
   (D5) A STROBE input data
   (D6) B RDY input data
   (D7) B STROBE input data

TABLE 6. CPU CONTROLS

(NOTE 1) **CS**	RA1	RA0	RD/$\overline{WE}$	WR/$\overline{RE}$	ACTION
0	X	X	X	X	No-op bus three-stated
X	0	0	X	X	No-op bus three-stated
X	X	X	0	0	No-op bus three-stated
X	X	X	1	1	No-op bus three-stated
X	X	X	1	1	No-op bus three-stated
1	0	1	1	0	Read status register (Note 1)
1	0	1	0	1	Load control register
1	1	0	1	0	Read port A (Note 1)
1	1	0	0	1	Load port A
1	1	1	1	0	Read port B (Note 1)
1	1	1	0	1	Load port B

NOTE:

1. Read = RD/$\overline{WE}$ = 1 and WR/$\overline{RE}$ = 0 is latched on trailing edge of CLOCK.

TABLE 7. MEMORY I/O USE

	RD/$\overline{WE}$ INPUT	WR/$\overline{RE}$ INPUT	TPB INPUT	
I/O Space	$\overline{MRD}$	TPB	TPB	} CPU Terminals
Memory Space	$\overline{MWR}$	$\overline{MRD}$	TPB	

} PIO Terminal

Function Pin Definition

CLOCK (Input):

Positive input pulse that latches READ and CS on its trailing edge.

CS - CHIP SELECT (Input)

A high-level voltage at this input selects the CDP1851 PIO.

RA0 - REGISTER ADDRESS 0 (Input):

This input and RA1 are used to select either the ports or the control/status registers.

RA1 - REGISTER ADDRESS 1(Input):

See RAO

BUS 0 - BUS 7:

Bidirectional CPU data bus.

$\overline{\text{CLEAR}}$ (Input)

A low-level voltage at this input resets both ports to the input mode, and also resets the status register, A RDY, B RDY, and interrupt enable (disabling interrupts).

$\overline{\text{A INT}}$ - $\overline{\text{A INTERRUPT}}$ (Output):

A low-level voltage at this output indicates the presence of one of the interrupt conditions listed in Table 3. This output is an open-drain NMOS device (to allow wired O Ring) and must be tied to a pullup resistor, normally 10kΩ.

$\overline{\text{B INT}}$ - $\overline{\text{B INTERRUPT}}$ (Output):

A low-level voltage at this output indicates the presence of one of the interrupt conditions listed in Table 3. This output is also an open-drain NMOS device and must be tied to a pullup resistor.

B RDY - B READY (Output):

This output is a handshaking or data bit I/O line in the bit-programmable mode.

B STROBE (Input):

An input handshaking line for port B in the input and output modes, and for port A when it is in the bidirectional mode. It can be used as a data bit I/O line in the bit-programmable mode except when port A is not programmed as bidirectional.

B0 - B7:

Data input or output lines for port B.

V_{SS}

Ground

A0 - A7:

Data input or output lines for port A.

A STROBE (Input):

An input handshaking line for port A in the input, output, and bidirectional modes. It can also be used as a data bit I/O line when port A is in the bit-programmable mode.

ARDY - AREADY (Output):

A output handshaking line or data bit I/O line.

TPB (Input):

A positive input pulse used as a data load, set, or reset strobe.

WR/$\overline{\text{RE}}$ - WRITE/$\overline{\text{READ ENABLE}}$ (Input):

A positive input used to write data from the CDP1851 to the CPU bus.

RD/$\overline{\text{WE}}$ - READ/$\overline{\text{WRITE ENABLE}}$ (Input):

A positive input used to read data from the CPU bus to the CDP1851 bus.

V_{DD}:

Positive supply voltage.

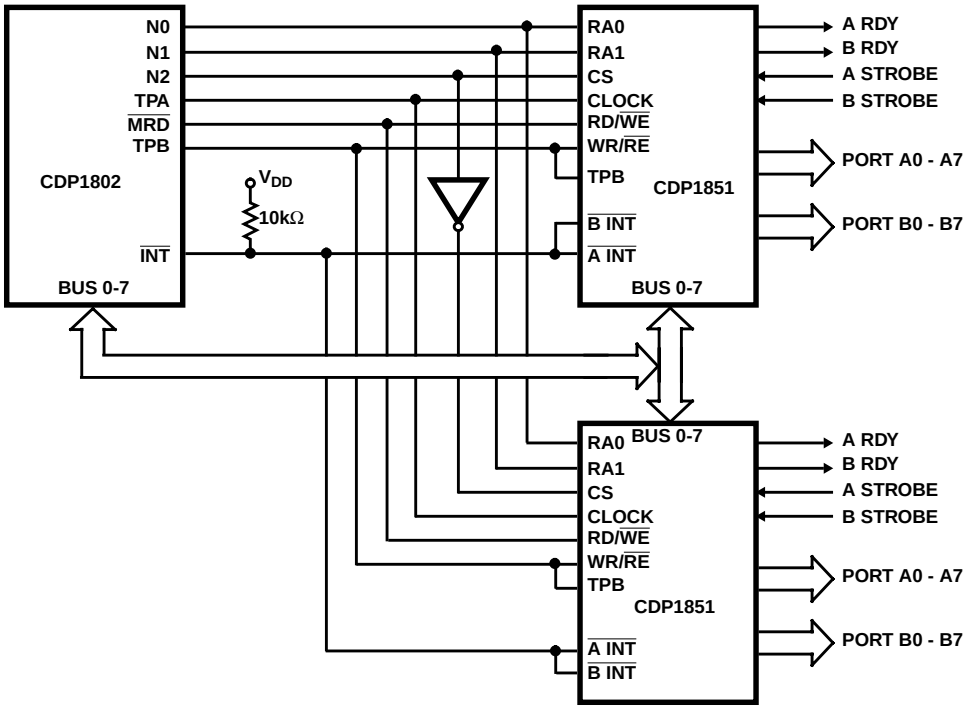


FIGURE 4. I/O SPACE I/O

Dynamic Electrical Specifications

At T_A = -40°C to +85°C, V_{DD} ±5%, t_r, t_f = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF

PARAMETER		V_{DD} (V)	LIMITS						UNITS
			CDP1851			CDP1851C			
			MIN	(NOTE 1) TYP	(NOTE 2) MAX	MIN	(NOTE 1) TYP	(NOTE 2) MAX	
INPUT MODE SEE FIGURES 4 AND 5									
Minimum Setup Times: Chip Select to CLOCK	t_{CSCL}	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns
RD/$\overline{WE}$ to CLOCK	t_{RWCL}	5	-	75	120	-	75	120	ns
		10	-	40	60	-	-	-	ns
WR/$\overline{RE}$ to CLOCK	t_{WRCL}	5	-	75	120	-	75	120	ns
		10	-	40	60	-	-	-	ns
Data in to STROBE	t_{DIST}	5	-	75	120	-	75	120	ns
		10	-	40	60	-	-	-	ns
Minimum Hold Times: Chip Select After CLOCK	t_{HCSCL}	5	-	75	120	-	75	120	ns
		10	-	40	60	-	-	-	ns
Address After TPB	t_{HATPB}	5	-	-50	0	-	-50	0	ns
		10	-	-25	0	-	-	-	ns
Data In After STROBE	t_{HSTDI}	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns
Data Bus Out After Address	t_{HADOH}	5	50	325	500	50	325	500	ns
		10	25	165	250	-	-	-	ns
Propagation Delay Times: TPB to $\overline{INT}$	t_{PINT}	5	-	200	300	-	200	300	ns
		10	-	100	150	-	-	-	ns
STROBE to $\overline{INT}$	t_{STINT}	5	-	200	300	-	200	300	ns
		10	-	100	150	-	-	-	ns
TPB to RDY	t_{TPRDY}	5	-	250	375	-	250	375	ns
		10	-	125	200	-	-	-	ns
STROBE to RDY	t_{STRDY}	5	-	260	400	-	260	400	ns
		10	-	130	200	-	-	-	ns
Minimum Pulse Widths: CLOCK	t_{WCL}	5	-	75	120	-	75	120	ns
		10	-	40	60	-	-	-	ns
TPB	t_{WTPB}	5	-	75	120	-	75	120	ns
		10	-	40	60	-	-	-	ns
STROBE	t_{WST}	5	-	100	150	-	100	150	ns
		10	-	50	75	-	-	-	ns
Access Time, Address to Data Bus Out	t_{ADA}	5	-	325	500	-	325	500	ns
		10	-	165	250	-	-	-	ns

NOTES:

1. Typical values are for T_A = 25°C and nominal voltages.
2. Maximum limits of minimum characteristics are the values above which all devices function.

Test Circuit and Waveforms

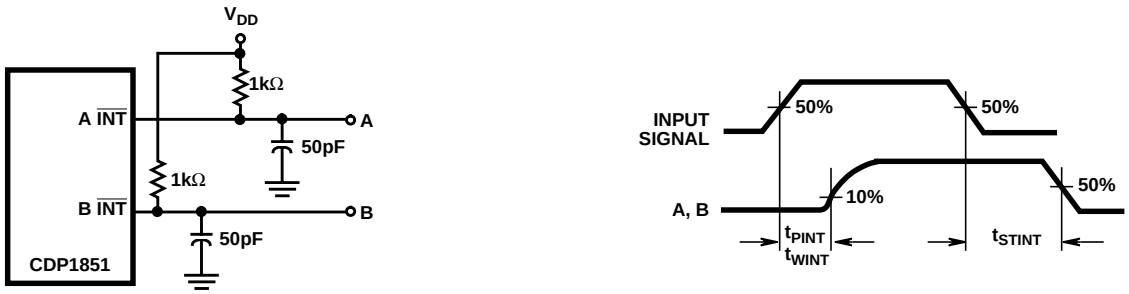


FIGURE 5. INTERRUPT SIGNAL PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS

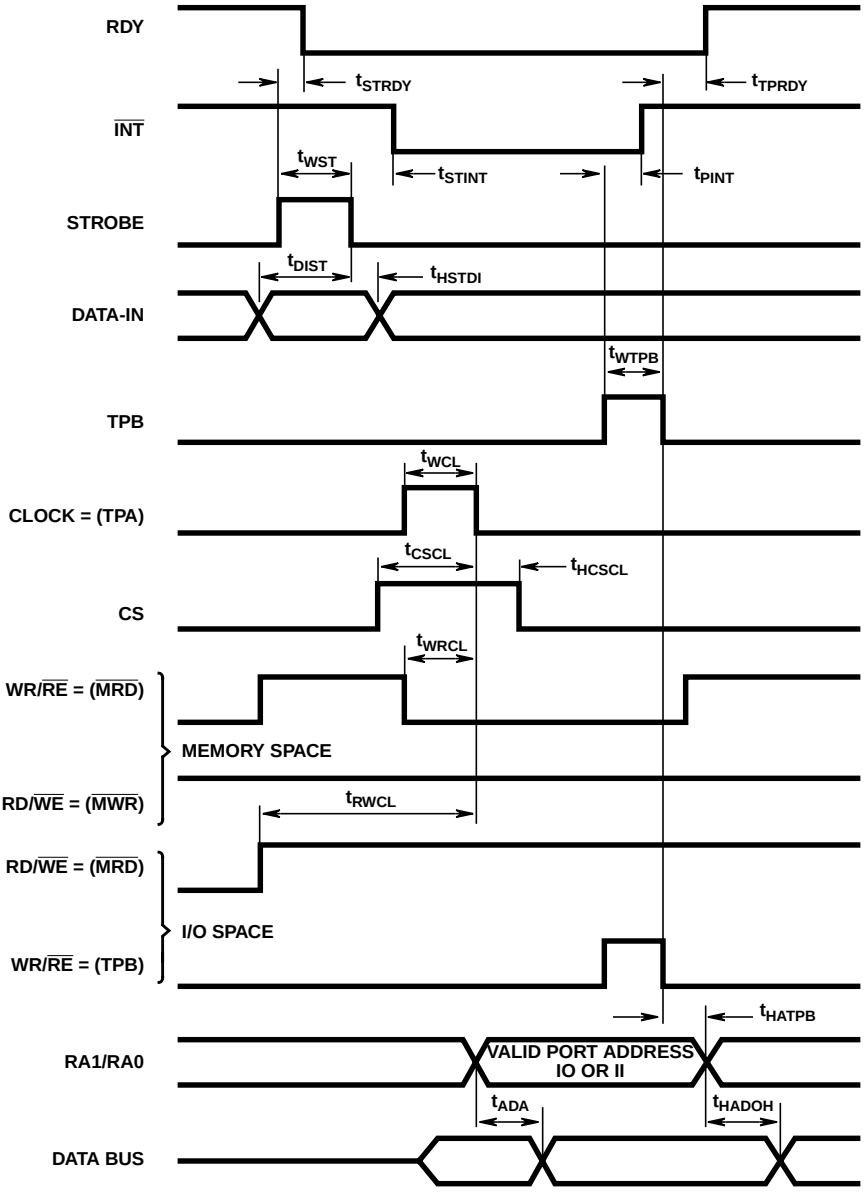


FIGURE 6. INPUT MODE TIMING WAVEFORMS

Dynamic Electrical Specifications At T_A = -40°C to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF

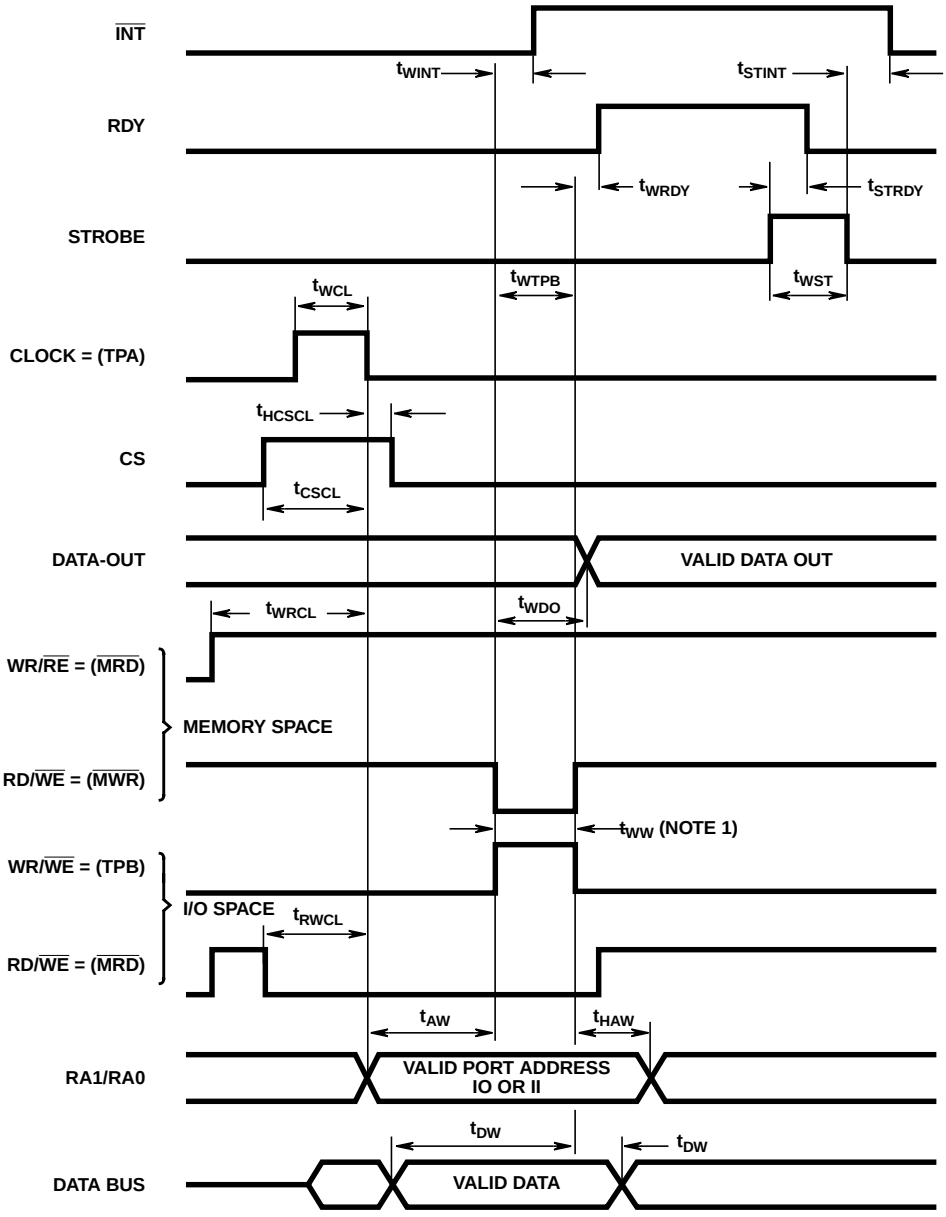
PARAMETERS		V_{DD} (V)	LIMITS						UNITS
			CDP1851			CDP1851C			
			MIN	(NOTE 1) TYP	(NOTE 2) MAX	MIN	(NOTE 1) TYP	(NOTE 2) MAX	
OUTPUT MODE SEE FIGURES 4 AND 6									
Minimum Setup Times:									
Chip Select to CLOCK	t_{CSCL}	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns
RD/$\overline{WE}$ to CLOCK	t_{RWCL}	5	-	75	120	-	75	120	ns
		10	-	40	60	-	-	-	ns
WR/$\overline{RE}$ to CLOCK	t_{WRCL}	5	-	75	120	-	75	120	ns
		10	-	40	60	-	-	-	ns
Address to WRITE (Note 3)	t_{AW}	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns
Data Bus to WRITE (Note 3)	t_{DW}	5	-	80	120	-	80	120	ns
		10	-	40	60	-	-	-	ns
Minimum Hold Times:									
Chip Select After CLOCK	t_{HCSCL}	5	-	75	120	-	75	120	ns
		10	-	40	60	-	-	-	ns
Address After WRITE (Note 3)	t_{HAW}	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns
Data Bus After WRITE (Note 3)	t_{HDW}	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns
Propagation Delay Times:									
WRITE to Data Out (Note 3)	t_{WDO}	5	-	225	350	-	225	350	ns
		10	-	125	200	-	-	-	ns
WRITE to $\overline{INT}$ (Note 3)	t_{WINT}	5	-	300	450	-	300	450	ns
		10	-	150	225	-	-	-	ns
WRITE to RDY (Note 3)	t_{WRDY}	5	-	350	525	-	350	525	ns
		10	-	175	275	-	-	-	ns
STROBE to $\overline{INT}$	t_{STINT}	5	-	200	300	-	200	300	ns
		10	-	100	150	-	-	-	ns
STROBE to RDY	t_{STRDY}	5	-	260	400	-	260	400	ns
		10	-	130	200	-	-	-	ns

Dynamic Electrical Specifications At T_A = -40°C to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF

PARAMETERS		V_{DD} (V)	LIMITS						UNITS
			CDP1851			CDP1851C			
			MIN	(NOTE 1) TYP	(NOTE 2) MAX	MIN	(NOTE 1) TYP	(NOTE 2) MAX	
Minimum Pulse Widths:									
CLOCK	t_{WCL}	5	-	75	120	-	75	120	ns
		10	-	40	60	-	-	-	ns
STROBE	t_{WST}	5	-	100	150	-	100	150	ns
		10	-	50	75	-	-	-	ns
WRITE (Note 3)	t_{WW}	5	-	175	275	-	175	275	ns
		10	-	90	150	-	-	-	ns

NOTES:

1. Typical values are for T_A = 25°C and nominal voltages.
2. Maximum limits of minimum characteristics are the values above which all devices function.
3. WRITE is the overlap of RD/$\overline{WE}$ = 0 and WR/$\overline{RE}$ = 1.



NOTE:

1. Write is the overlap of WR/RE = 1 and RD/WE = 0

FIGURE 7. OUTPUT MODE TIMING WAVEFORMS