

intersil

CDP1872C, CDP1874C, CDP1875C

March 1997

High-Speed 8-Bit Input and Output Ports

Features

- Parallel 8-Bit Input/Output Register with Buffered Outputs
- High-Speed Data-In to Data-Out 85ns (Max) at $V_{DD} = 5V$
- Flexible Applications In Microprocessor Systems as Buffers and Latches
- High Order Address-Latch Capability in CDP1800-Series Microprocessor Systems
- Output Sink Current = 5mA (Min) at $V_{DD} = 5V$
- Three-State Output - CDP1872C and CDP1874C

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
CDP1872CE	-40°C to +85°C	PDIP	E22.4
CDP1874CE	-40°C to +85°C	PDIP	E22.4
CDP1875CE	-40°C to +85°C	PDIP	E22.4

Description

The CDP1872C, CDP1874C and CDP1875C devices are high-speed 8-bit parallel input and output ports designed for use in the CDP1800 microprocessor system and for general use in other microprocessor systems. The CDP1872C and CDP1874C are 8-bit input ports; the CDP1875C is an 8-bit output port.

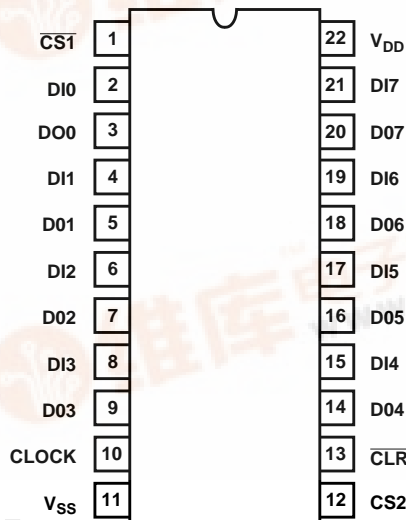
These devices have flexible capabilities as buffers and data latches and are reset by \overline{CLR} input when the data strobe is not active.

The CDP1872C and CDP1874C are functionally identical except for device selects. The CDP1872C has one active low and one active high select; the CDP1874C has two active high device selects. These devices also feature Three-state outputs when deselected. Data is strobed into the register on the leading edge of the CLOCK and latched on the trailing edge of the CLOCK.

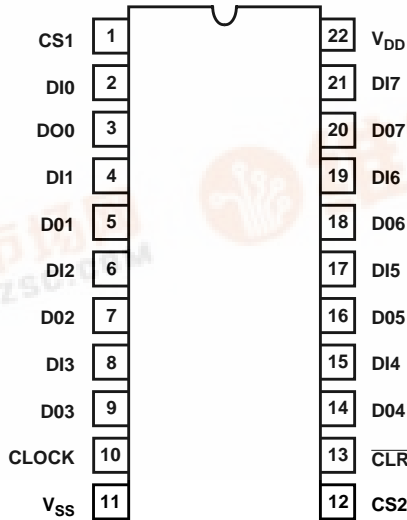
The CDP1875C is an output port with data latched into the registers when the device selects are active. There are two active high and one active low selects. The output buffers are enabled at all times.

Pinouts

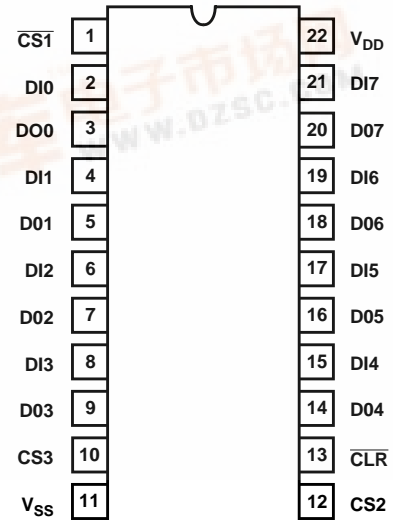
CDP1872C INPUT PORT
(PDIP)
TOP VIEW



CDP1874C INPUT PORT
(PDIP)
TOP VIEW



CDP1875C OUTPUT PORT
(PDIP)
TOP VIEW



CDP1872C, CDP1874C, CDP1875C

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD}) -0.5V to +7V
 (Voltage referenced to V_{SS} Terminal)
 Input Voltage Range, All Inputs -0.5V to V_{DD} +0.5V
 DC Input Current, Any One Input. ± 10 mA

Thermal Information

Thermal Resistance (Typical) θ_{JA} ($^{\circ}\text{C/W}$)
 PDIP Package 75
 Device Dissipation Per Output Transistor
 T_A = Full Package Temperature Range
 (All Package Types) 100mW
 Operating Temperature Range (T_A)
 Package Type E -40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$
 Storage Temperature Range (T_{STG}) -65 $^{\circ}\text{C}$ to +150 $^{\circ}\text{C}$
 Lead Temperature (During Soldering)
 At distance 1/16 \pm 1/32 In. (1.59 \pm 0.79mm)
 from case for 10s max. +265 $^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

At T_A = -40 to +85 $^{\circ}\text{C}$. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	LIMITS ALL TYPES	UNITS
DC Operating-Voltage Range	4 to 6.5	V
Input Voltage Range	V_{SS} to V_{DD}	V

Static Electrical Specifications

At T_A = -40 to +85 $^{\circ}\text{C}$, V_{DD} $\pm 5\%$, Unless Otherwise Specified.

PARAMETER		TEST CONDITIONS			LIMITS ALL TYPES			UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	
Quiescent Device Current	I_{DD}	-	0, 5	5	-	25	50	μA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	5	10	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-4	-7	-	mA
Output Voltage Low-Level (Note 2)	V_{OL}	-	0, 5	5	-	0	0.1	V
Output Voltage High-Level (Note 2)	V_{OH}	-	0, 5	5	4.9	5	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	V
Input Leakage Current	I_{IN}	-	0, 5	5	-	-	± 1	μA
Three-State Output Leakage Current (Note 3)	I_{OUT}	0, 5	0, 5	5	-	-	± 5	μA
Input Capacitance	C_{IN}	-	-	-	-	15	-	pF
Output Capacitance (Note 3)	C_{OUT}	-	-	-	-	15	-	pF

NOTES:

- Typical values are for T_A = +25 $^{\circ}\text{C}$ and nominal V_{DD} $\pm 5\%$.
- I_{OL} = I_{OH} = 1 μA
- For CDP1872C and CDP1874C only.

CDP1872C, CDP1874C, CDP1875C

Logic Diagrams

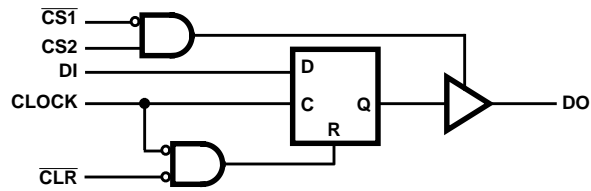


FIGURE 1. EQUIVALENT LOGIC DIAGRAM (1 OF 8 LATCHES SHOWN) FOR CDP1872C

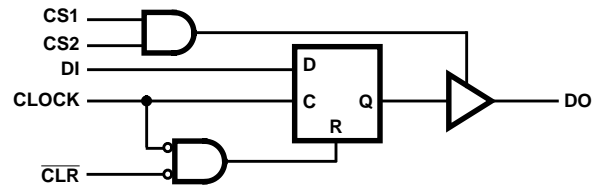


FIGURE 2. EQUIVALENT LOGIC DIAGRAM (1 OF 8 LATCHES SHOWN) for CDP1874C

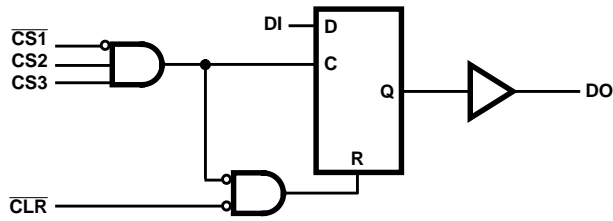


FIGURE 3. EQUIVALENT LOGIC DIAGRAM (1 OF 8 LATCHES SHOWN) FOR CDP1875C

Dynamic Electrical Specifications At $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $t_R, t_F = 10\text{ns}$, $V_{IH} = 0.7V_{DD}$, $V_{IL} = 0.3V_{DD}$, $C_L = 150\text{pF}$

PARAMETER		LIMITS			UNITS
		CDP1872C, CDP1874C			
		MIN	(NOTE 1) TYP	(NOTE 2) MAX	
INPUT PORT (FIGURE 4)					
Output Enable	t _{EN}	-	45	90	ns
Output Disable	t _{DIS}	-	45	90	ns
Clock to Data Out	t _{CLO}	-	45	90	ns
$\overline{\text{Clear}}$ to Output	t _{CRO}	-	80	160	ns
Data In to Data Out	t _{DIO}	-	50	85	ns
Minimum Data Setup Time	t _{DSU}	-	10	30	ns
Data Hold Time	t _{DH}	-	10	30	ns
Minimum Clock Pulse Width	t _{CL}	-	30	60	ns
Minimum $\overline{\text{Clear}}$ Pulse Width	t _{CR}	-	30	60	ns

NOTES:

- Typical values are for $T_A = +25^\circ\text{C}$ and $V_{DD} \pm 5\%$.
- Maximum values are for $T_A = +85^\circ\text{C}$ and $V_{DD} \pm 5\%$

CDP1872C, CDP1874C, CDP1875C

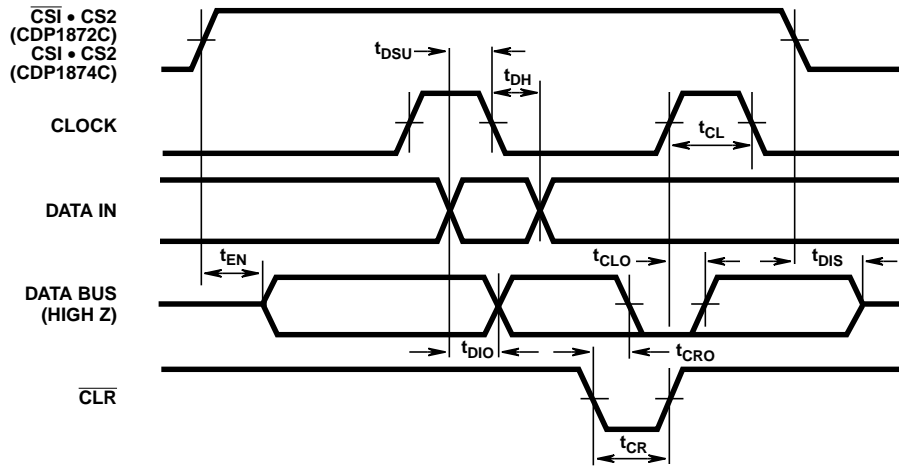


FIGURE 4. TIMING WAVEFORMS FOR CDP1872C AND CDP1874C (INPUT-PORT TYPES)

Dynamic Electrical Specifications At $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $t_R, t_F = 10\text{ns}$, $V_{IH} = 0.7V_{DD}$, $V_{IL} = 0.3V_{DD}$, $C_L = 150\text{pF}$

PARAMETER		LIMITS			UNITS
		CDP1875C			
		MIN	(NOTE 1) TYP	(NOTE 2) MAX	
OUTPUT PORT (FIGURE 5)					
Clock to Data Out	t _{CLO}	-	50	100	ns
Clear to Output	t _{CRO}	-	80	160	ns
Data In to Data Out	t _{DIO}	-	50	85	ns
Minimum Data Setup Time	t _{DS}	-	10	30	ns
Data Hold Time	t _{DH}	-	10	30	ns
Minimum Clear Pulse Width	t _{CR}	-	30	60	ns

NOTES:

1. Typical values are for $T_A = +25^\circ\text{C}$ and $V_{DD} \pm 5\%$.
2. Maximum values are for $T_A = +85^\circ\text{C}$ and $V_{DD} \pm 5\%$

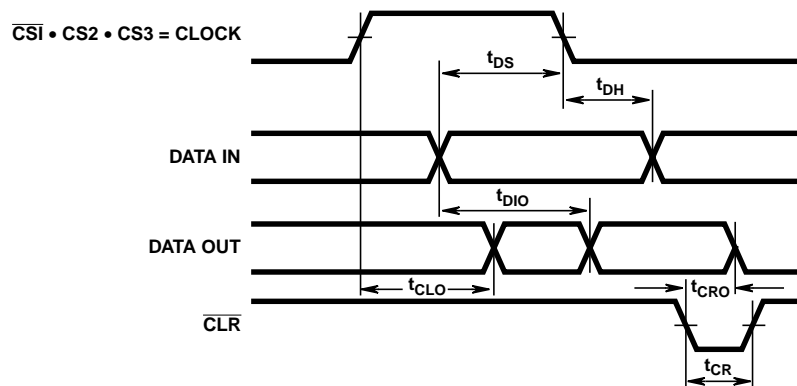


FIGURE 5. TIMING WAVEFORMS FOR CDP1875C (OUTPUT PORT)

CDP1872C, CDP1874C, CDP1875C

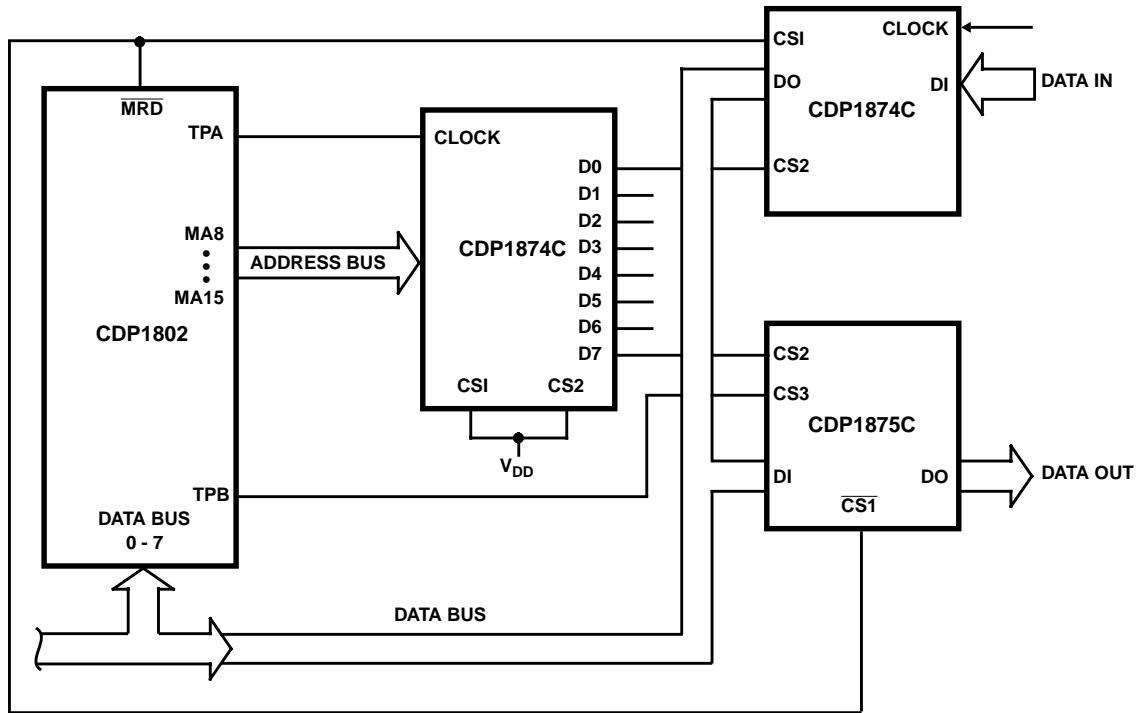


FIGURE 6. CDP1874C USED AS AN INPUT PORT AND ADDRESS LATCH WITH CDP1875C USED AS AN OUTPUT PORT

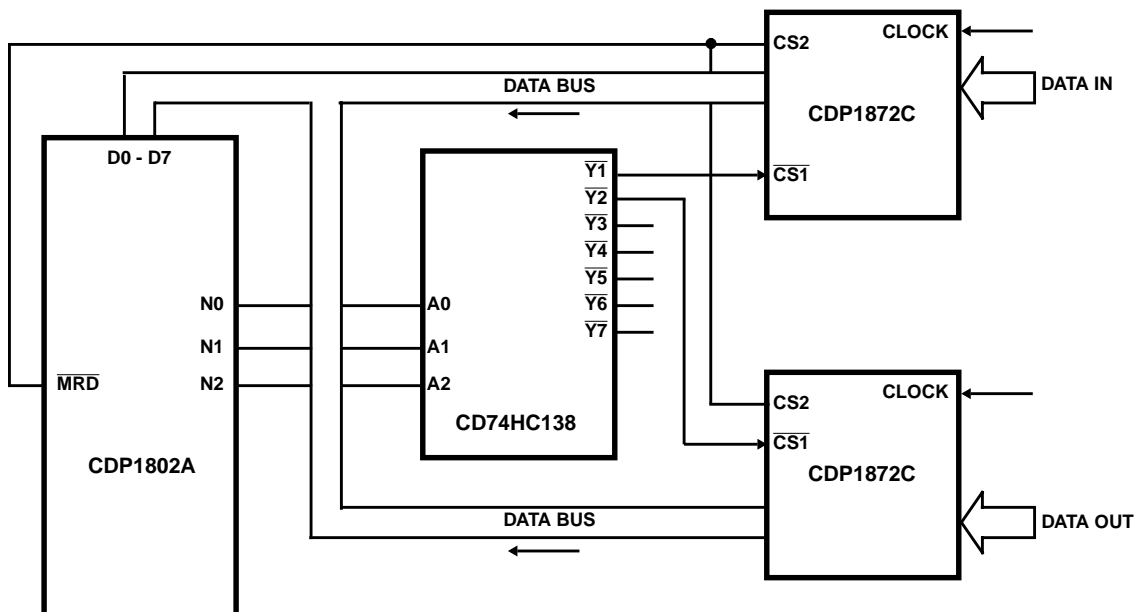


FIGURE 7. CDP1872C USED AS AN INPUT PORT AND SELECTED BY CD74HC138

CDP1872C, CDP1874C, CDP1875C

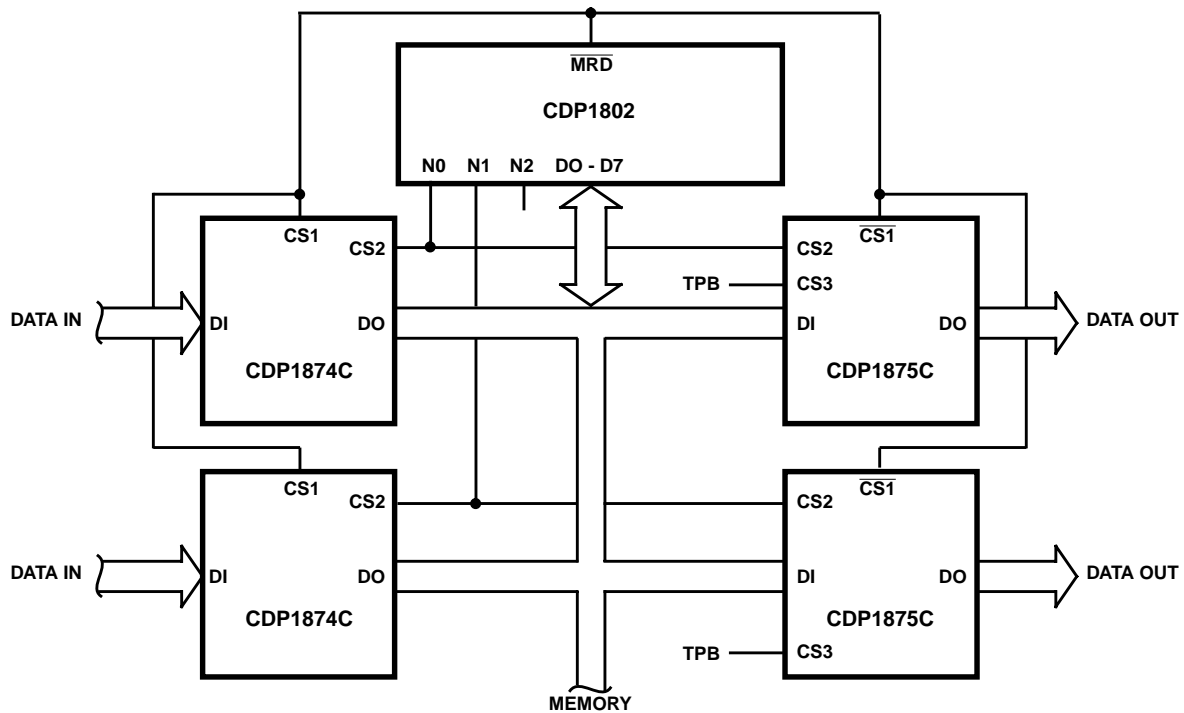


FIGURE 8. CDP1874C AND CDP1875C USED AS INPUT/OUTPUT BUFFERS

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE

Intersil SA
Mercure Center
100, Rue de la Fusée
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029