CMOS Serial 8-Bit Input/Output Port

The CDP68HC68P1 is a serially addressed 8-bit Input/Output port that allows byte or individual bit control. It consists of three registers, an output buffer and control logic. Data is shifted in and out of the device via shift register that utilizes the SPI (Serial Peripheral Interface) bus. The I/O port data flow is controlled by the Data Direction Register and data is stored in the Data Register that outputs or senses the logic levels at the buffered I/O pins. All inputs, including the serial interface are Schmitt triggered. This device also features a compare function that compares the data register and port pin values for 4 programmable conditions and sets a software accessible flag if the condition is satisfied. The user also has the option of bit-set or bit-clear when writing to the data register.

Ordering Information

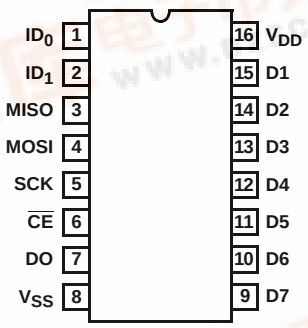
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CDP68HC68P1E	-55 to 85	16 Ld PDIP	E16.3
CDP68HC68P1M	-55 to 85	16 Ld SOIC	M16.15

Features

- Fully Static Operation
- Operating Voltage Range 3-6V
- Compatible with Intersil/Motorola SPI Bus
- 2 External Address Pins Tied to V_{DD} or V_{SS} to Allow Up to 4 Devices to Share the Same Chip Enable
- Versatile Bit-Set and Bit-Clear Capability
- Accepts Either SCK Clock Polarity - SCK Voltage Level is Latched When Chip Enable Goes Active
- All Inputs are Schmitt-Trigger
- 8-Bit I/O Port - Each Bit can be Individually Programmed as an Input or Output Via an 8-Bit Data Direction Register
- Programmable On Board Comparator
- Simultaneous Transfer of Compare Information to CPU During Read or Write - Separate Access Not Required

Pinout

CDP68HC68P1
(PDIP, SOIC)
TOP VIEW



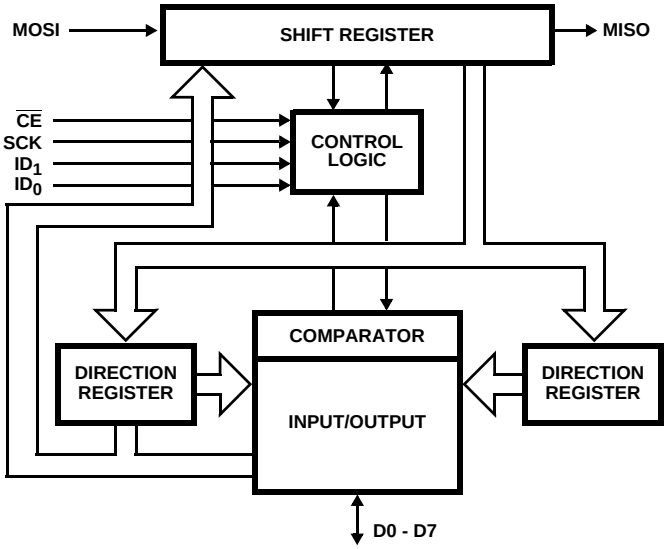


FIGURE 1. SINGLE PORT I/O BLOCK DIAGRAM

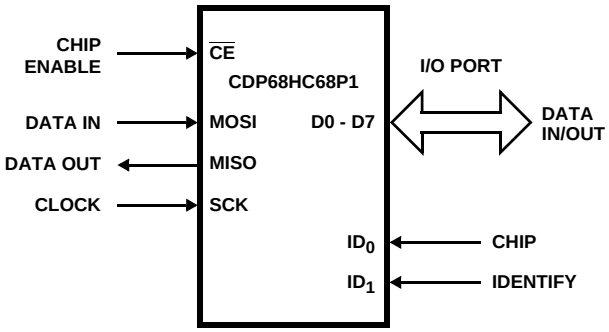


FIGURE 2. SINGLE PORT I/O

Pin Descriptions

ID_0, ID_1 - Chip identify pins, normally tied to V_{DD} to V_{SS}. The 4 possible combinations of these pins allow 4 I/Os to share a common chip enable. When the levels at these pins match those of the identify bits in the control word, the serial bus is enabled. The chip identify pins will retain their previous logic state if the lines driving them become Hi-Z.

MISO - Master-in, Slave out pin. Data bytes are shifted out at this pin most significant bit first. When the chip enable signal is high, this pin is Hi-Z.

MOSI - Master-out, Slave in pin. Data bytes are shifted in at this pin most significant bit first. This pin will retain its previous logic state if its driving line becomes Hi-Z.

SCK - Serial clock input. This input causes serial data to be latched from the MOSI input and shifted out on the MISO output.

$\overline{CE}$ - A negative chip enable input. A high to low transition on this pin latches the inactive SCK polarity and compare flag and indicates the start of a data transfer. The serial interface logic is enabled only when CE is low. This pin will retain its previous logic state if its driving line becomes Hi-Z.

D0 -D7 - I/O Port pins. Individual programmable inputs or outputs.

V_{DD} and V_{SS} - Positive and negative power supply line.

All pins except the power supply lines and MISO have Schmitt-trigger buffered inputs.

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD}) . . . . . .-0.5V to +7V
(Voltage Referenced to V_{SS} Terminal)
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input . . . . . ±10mA
Power Dissipation Per Package (P_D)
T_A = -40°C to 60°C (Package Type E) 500mW
T_A = 60°C to 85°C (Package Type E)
Derate Linearly at . . . . . 12mW/°C to 200mW
T_A = -40°C to 60°C (Package Type M) (Note 1) 300mW
T_A = 60°C to 85°C (Package Type M) (Note 1)
Derate Linearly at . . . . . 5mW/°C to 175mW

Operating Conditions

Temperature Range (T_A)
Package Type E, M . . . . . -55°C to 85°C
DC Operating Voltage Range . . . . . 3V Min, 6V Max
Serial Clock Frequency, f_{SCK}, V_{DD} = 3V. . . . . .1.05MHz Max
Serial Clock Frequency, f_{SCK}, V_{DD} = 4.5V . . . . . .2.1MHz Max
Input Voltage Range, V_{IH} . . . . . V_{DD} +0.3V Max
Input Voltage Range, V_{IL} . . . . . -0.3V Min

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	90	NA
SOIC Package	110	NA

Device Dissipation Per Output Transistor 100mW
T_A = Full Package Temperature Range (All Package Types)
Maximum Storage Temperature Range (T_{STG}) . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s)
At Distance 1/16in ± 1/32in. (1.59 ± 0.79mm) . . . . . .265°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Printed circuit board mount: 57mm x 57mm minimum area x 1.6mm thick G10 epoxy glass, or equivalent.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Static Electrical Specifications T_A = -40°C to 85°C, V_{DD} = 3.3V ±10%, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	(NOTE 3) TYP	MAX	UNITS
Output Voltage	V_{OH}	I_{OH} = -0.4mA, V_{DD} = 3V	2.7	-	-	V
	V_{OL}	I_{OL} = 0.4mA, V_{DD} = 3V	-	-	0.3	V
Input Voltage						
D0 - D7 Positive Trigger Threshold	V_P		1.85	-	2.4	V
Negative Trigger Threshold	V_N		0.85	-	1.35	V
Hysteresis	V_{IH}		0.85	-	1.25	V
Input Voltage						
ID_0, ID_1, MOSI, SCK, $\overline{CE}$ Positive Trigger Threshold	V_P		1.3	-	1.9	V
Negative Trigger Threshold	V_N		0.8	-	1.2	V
Hysteresis	V_{IH}		0.5	-	0.95	V
Input Leakage Current	I_{IN}		-	-	±1	µA
Standby Device Current	I_{DDS}		-	1	15	µA
Three-State Output Leakage Current	I_{OUT}		-	-	±10	µA
Operating Device Current (Note 4)	I_{OPER}	V_{IN} = V_{IL}, V_{IH}	-	0.1	1	mA
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1MHz, T_A = 25°C	-	4	6	pF

NOTES:

3. Typical values are for T_A = 25°C and nominal V_{DD}.
4. Outputs open circuited; cycle time = Min. t_{CYCLE}, duty = 100%.

Static Electrical Specifications

At $T_A = -40^oC$ to 85^oC, $V_{DD} = 5V \pm 10\%$, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	(NOTE 5) TYP	MAX	UNITS
Output Voltage	V_{OH}	$I_{OH} = -1.6mA$, $V_{DD} = 4.5V$	3.7	-	-	V
	V_{OL}	$I_{OL} = 1.6mA$, $V_{DD} = 4.5V$	-	-	0.4	V
	V_{OH}	$I_{OH} \leq 20\mu A$, $V_{DD} = 4.5V$	4.4	-	-	V
	V_{OL}	$I_{OL} \leq 20\mu A$, $V_{DD} = 4.5V$	-	-	0.1	V
Input Voltage						
D0 - D7 Positive Trigger Threshold	V_P		2.15	-	3.05	V
Negative Trigger Threshold	V_N		1.35	-	2	V
Hysteresis	V_{IH}		0.8	-	1.2	V
Input Voltage						
ID_0, ID_1, MOSI, SCK, $\overline{CE}$ Positive Trigger Threshold	V_P		3.15	-	3.85	V
Negative Trigger Threshold	V_N		1.7	-	2.25	V
Hysteresis	V_{IH}		1.3	-	1.7	V
Input Leakage Current	I_{IN}		-	-	± 1	µA
Standby Device Current	I_{DDS}		-	1	15	µA
Three-State Output Leakage Current	I_{OUT}		-	-	± 10	µA
Operating Device Current (Note 6)	I_{OPER}	$V_{IN} = V_{IL}$, V_{IH}	-	0.2	2	mA
Input Capacitance	C_{IN}	$V_{IN} = 0V$, f = 1MHz, $T_A = 25^oC$	-	4	6	pF

NOTES:

5. Typical values are for $T_A = 25^oC$ and nominal V_{DD}.
6. Outputs open circuited; cycle time = Min, t_{CYCLE}, duty = 100%.

Dynamic Electrical Specifications - Bus Timing

$V_{DD} \pm 10\%$, $V_{SS} = 0V$ DC, $T_A = -40^oC$ to 85^oC, $C_L = 200pF$. See Figures 8 and 9.

PARAMETER	SYMBOL	$V_{DD} = 3.3V$		$V_{DD} = 5V$		UNITS
		MIN	MAX	MIN	MAX	
Chip Enable Set-Up Time	t_{EVCV}	200	-	100	-	ns
Chip Enable after Clock Hold Time	t_{CVEX}	250	-	125	-	ns
Clock Width High	t_{WH}	400	-	200	-	ns
Clock Width Low	t_{WL}	400	-	200	-	ns
Data In to Clock Set-Up Time	t_{DVCV}	200	-	100	-	ns
Data In after Clock Hold Time	t_{CVDX}	200	-	100	-	ns
Clock to Data Propagation Delay	t_{CVDV}	-	200	-	100	ns
Chip Disable to Output High Z	t_{EXQZ}	-	200	-	100	ns
Output Rise Time	t_r	-	200	-	100	ns
Output Fall Time	t_f	-	200	-	100	ns
Clock to Data Out Archive	t_{CVQX}	-	200	-	100	ns
Clock Recovery Time	t_{REC}	200	-	200	-	ns

Waveforms

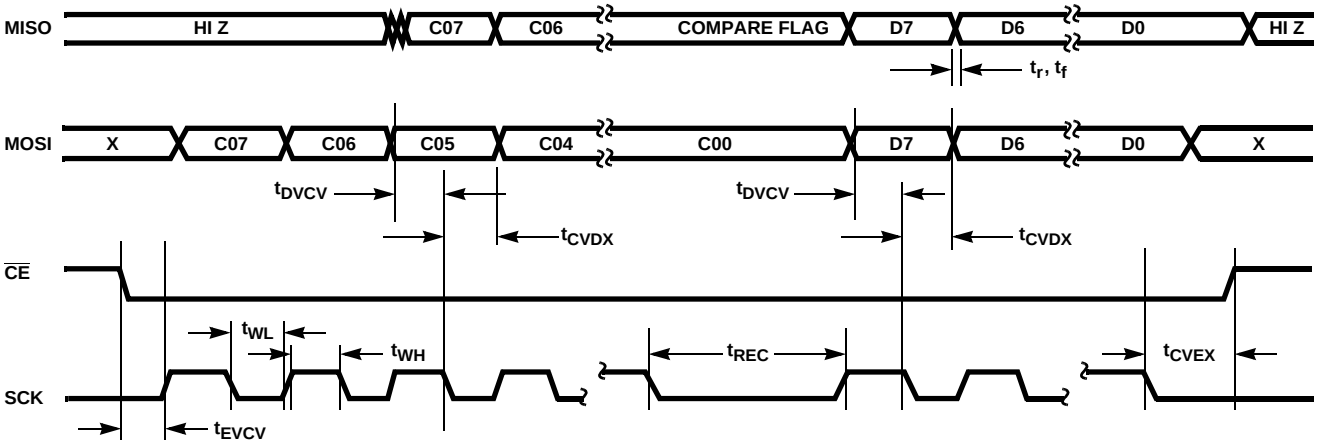


FIGURE 3. PORT-PIN DATA CHANGES

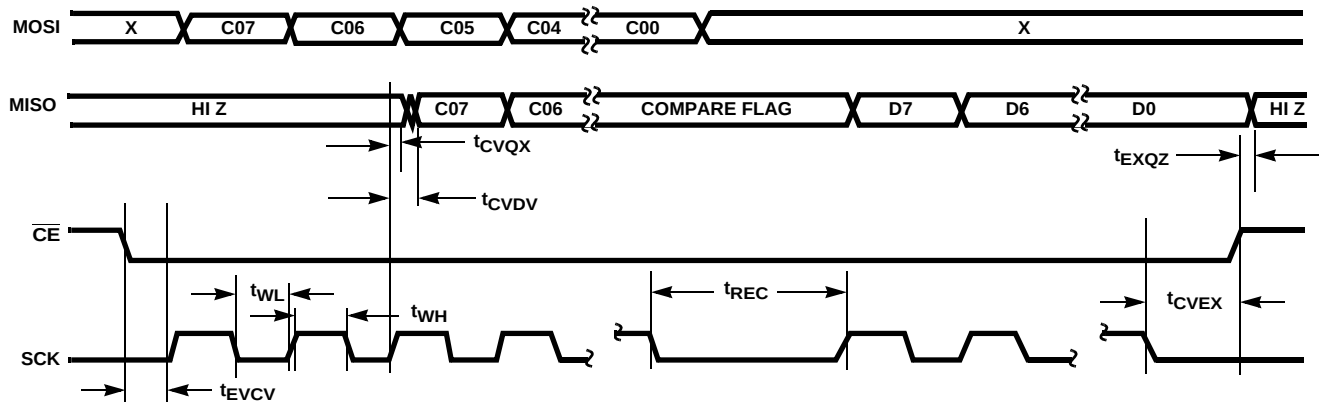
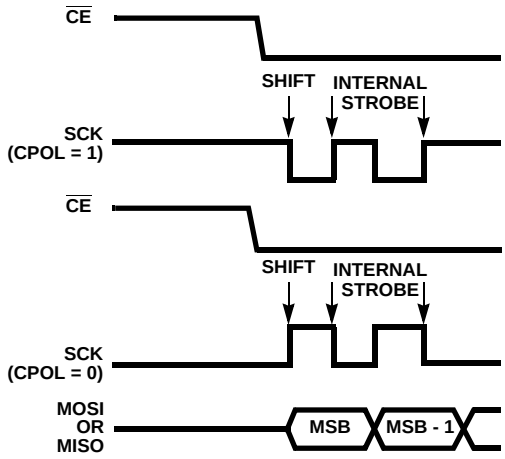


FIGURE 4. READ CYCLE TIMING WAVEFORMS



NOTE: CPOL and CPHA are bits in the CDP68HC05C4B and CDP68HC05C16B MCU control register and determine inactive clock polarity and phase. CPHA must always equal 1.

FIGURE 5. DATA TRANSFERS UTILIZING CLOCK INPUT

Introduction

The single port I/O is serially accessed via the synchronous SPI bus. It features 8 data pins that are programmed as inputs or outputs. Serial access consists of a two-byte operation. The first byte shifted in is the control byte that configures the device. The second byte transferred is the data byte that is read from or written to the data register or data direction register. This data byte can also be programmed to act as a mask to set or clear individual bits.

Functional Description

The single port I/O consists of three byte-wide registers, (data direction, data and shift) an input/output buffer and control logic circuitry (See Figure 1). Data is transferred between the I/O data and data direction registers via the shift register. Once the I/O port is selected, the first byte shifted in to the shift register is the control byte that selects the register (the Data or Data direction register), determines data transfer direction (read or write) and sets the compare

feature and function (mask or data) of the byte immediately following the control byte, the data byte (See Addressing the Single Port I/O). Each bit of the data register may be individually programmed as an input or output. A logic low in a data direction bit programs that pin as an input, a logic high makes it an output. A read operation of data register pins programmed as inputs reflects the current logic level present at the buffered port pins. A read operation of those data register pins programmed as outputs indicates the last value written to that location. At power-up, all port pins are configured as unterminated inputs. Two chip identify pins are used to allow up to 4 I/O ports to share the same chip enable signal. The first two bits shifted in are compared with the hardwired levels at the chip identify pins to enable the selected I/O for serial data transfer. Note that when chip enable becomes true, the compare flag is latched for all devices sharing the same chip enable.

Compare Function

The value of a port pin (D0 - D7), configured as an input, is compared with the corresponding bit value (DR0 - DR7) stored in the Data Register. Pins configured as outputs are assumed to have the same value as the corresponding bit stored in the Data Register. The compare function is programmed via C01 and C00 (CM1, CM0) of the Address Byte. As shown in Table 1, the values for CM1 and CM0 will sense one of four separate conditions.

The compare flag is set to one when the programmed condition is satisfied. Otherwise, the flag is cleared to zero. The compare flag is latched when the device is enabled (a transition of $\overline{CE}$ from “High” to “Low”).

TABLE 1.

CM1	CM0	CONDITION
0	0	At least one non-match
0	1	All match
1	0	All are non-match
1	1	At least one match

Data Format

During write operations, the data byte that follows the control byte is normally the data word that is transferred to the data or data direction register. Control bits 2 and 3 (DF0 and DF1) change the interpretation of this data as shown in Table 2. Note that one or more bits can be set or cleared in either register without having to write to bits not requiring change.

TABLE 2.

C03 DF1	C02 DF0	OPERATION
0	X	Data following the control word will be written to the selected register.
1	0	Data following the control word is a mask. Those bits which are a 1 will cause that register flip-flop to be cleared to 0. Those which are a 0 will cause that register flip-flop to be unchanged.
1	1	Data following the control word is a mask. Those bits which are a 1 will cause that register flip-flop to be set to 1; those which are a 0 will cause that register flip-flop to be unchanged.

TABLE 3. EXAMPLE

CONTROL	DATA	PREVIOUS REGISTER VALUE	NEW REGISTER VALUE
C07 C06 C05 1 0 X C01 C00	11110000	10101010	11110000
C07 C06 C05 1 1 1 C01 C00	11110000	10101010	11111010
C07 C06 C05 1 1 0 C01 C00	11110000	10101010	00001010
C07 C06 C05 1 1 X C01 C00	00000000	10101010	10101010

X = Don’t Care

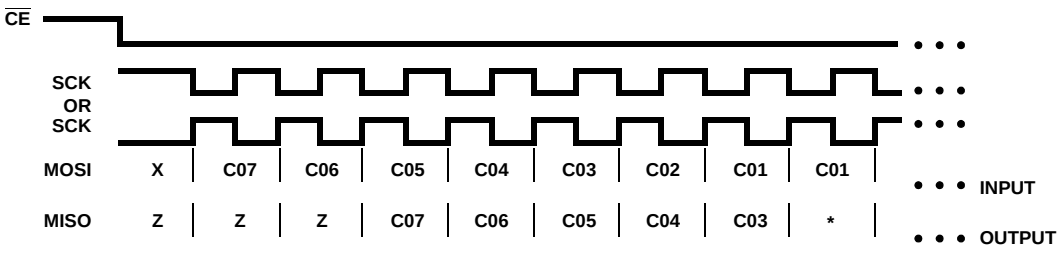


FIGURE 6. CONTROL BYTE

Addressing the Single Port I/O

The Serial Peripheral Interface (SPI) utilized by the I/O Port is a serial synchronous bus for control and data transfers. It consists of a SCK clock input pin that shifts data out of the I/O port (MISO, MASTER IN, SLAVE OUT) and latches data presented at the input pin, MOSI (master out, slave in). Data is transferred most significant bit first. There is one SCK clock for each bit transferred and bits are transferred in groups of eight.

When the I/O port is selected by bringing the chip enable pin low, the logic level at the SCK input is sampled to determine the internal latching and shift polarity for input and output signals on the SPI. (See Figure 3).

The first byte shifted in when the chip is selected is always the control byte followed by one or more bytes that become data or a mask for the data and data direction register. As the control byte is being shifted in one the MOSI line, data on the MOSI line shifts out. (See Figure 4).

7	6	5	4	3	2	1	0
ID1	ID0	RS	$\overline{R}$/W	DF1	DF0	CM1	CM0

C07 (ID_1), C06 (ID_0): Chip-Identify bits.

C05 (RS) - Register Select. When RS is low, the data register is selected. When RS is high, the Direction Register is selected.

C04 ($\overline{R}$/W) - $\overline{Read}$/Write. Low when data is to be transferred from the SPI I/O to the CPU (read) and high when the I/O is receiving data from the CPU (write).

C03 (DF1), C02 (DF0) - Data Format Bits. These have meaning only when $\overline{R}$/W is high. During a write operation, DF1 and DF0 control how the byte following the control word is interpreted. See Data Format.

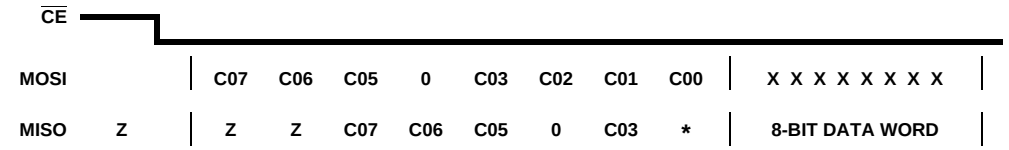
C01 (CM1), C00 (CM0) - Compare Mode Select. These bits select one of four events which will set the internal Condition Flag. See Compare Operation.

Read Operation

During a read operation, the CPU transfers data from the I/O by first sending a control byte on the MOSI line while the chip-selected I/O sends compare information followed by one or more data bytes on the MISO line. The selected register will be continuously read if $\overline{CE}$ is held low after the first data byte is shifted out.

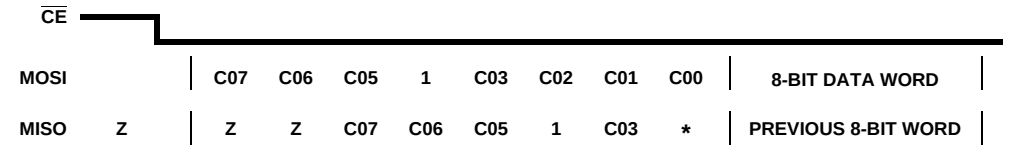
Write Operation

During a write operation, the data byte follows the control byte for the selected register. While this byte is being shifted in, old data from that register is shifted out. If CE remains low after the data byte is shifted in, MISO becomes high impedance and the new data is placed in the selected register. At the time the eighth data bit is strobed into the data pins (D0 - D7) will change as indicated in Figure 7-9.



X = DON'T CARE
Z = HIGH IMPEDANCE
* = COMPARE FLAG

FIGURE 7. READ BYTES



Z = HIGH IMPEDANCE
* = COMPARE FLAG

FIGURE 8. READ BYTES

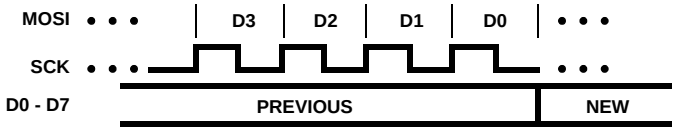
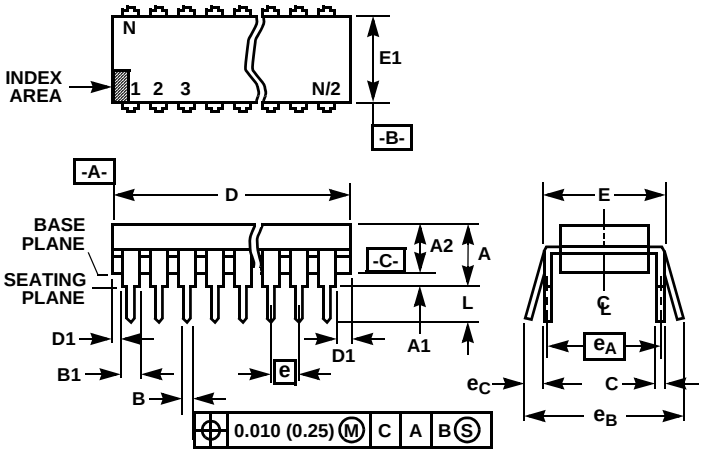


FIGURE 9. PORT-PIN DATA CHANGES

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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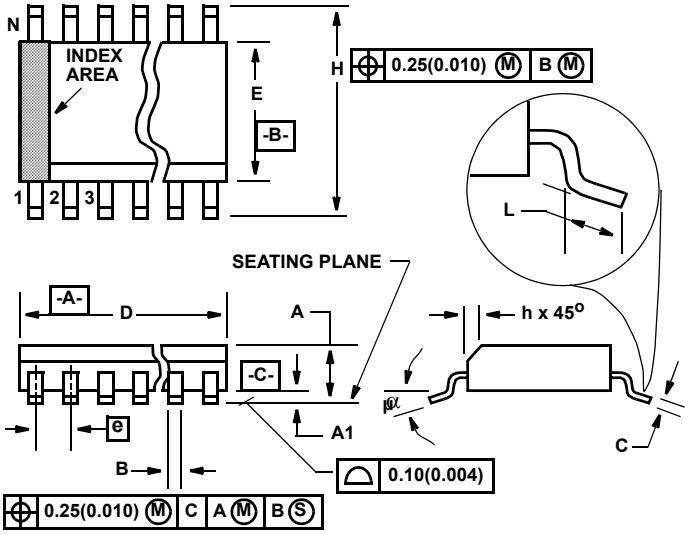
Small Outline Plastic Packages (SOIC)



M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
B	0.014	0.019	0.35	0.49	9
C	0.007	0.010	0.19	0.25	-
D	0.386	0.394	9.80	10.00	3
E	0.150	0.157	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.228	0.244	5.80	6.20	-
h	0.010	0.020	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.