



# CEP21A3/CEB21A3

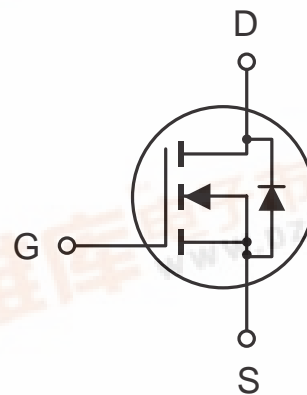
Nov. 2002

## N-Channel Logic Level Enhancement Mode Field Effect Transistor

4

### FEATURES

- 30V , 20A ,  $R_{DS(ON)}=45m\Omega$  @  $V_{GS}=10V$ .  
 $R_{DS(ON)}=70m\Omega$  @  $V_{GS}=4.5V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- TO-220 & TO-263 package.



### ABSOLUTE MAXIMUM RATINGS ( $T_c=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous -Pulsed	$I_D$	20	A
	$I_{DM}$	60	A
Drain-Source Diode Forward Current	$I_S$	20	A
Maximum Power Dissipation @ $T_c=25^\circ C$ Derate above $25^\circ C$	$P_D$	43	W
		0.29	W/ $^\circ C$
Operating and Storage Temperature Range	$T_J, T_{STG}$	-65 to 175	$^\circ C$

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.5	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ C/W$



# CEP21A3/CEB21A3

4

## ELECTRICAL CHARACTERISTICS (Tc=25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V			1	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V			±100	nA
<b>ON CHARACTERISTICS<sup>a</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	0.8		2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 12A		36	45	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 15A		55	70	mΩ
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 10V	20			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 10V, I <sub>D</sub> = 12A		20		S
<b>DYNAMIC CHARACTERISTICS<sup>b</sup></b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V f = 1.0MHz		364		pF
Output Capacitance	C <sub>OSS</sub>			197		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			62		pF
<b>SWITCHING CHARACTERISTICS<sup>b</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> = 15V, I <sub>D</sub> = 12A V <sub>GS</sub> = 10V, R <sub>GEN</sub> = 2.5Ω		12	25	ns
Rise Time	t <sub>r</sub>			5	15	ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			14	30	ns
Fall Time	t <sub>f</sub>			14	30	ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15V, I <sub>D</sub> = 6A V <sub>GS</sub> = 10V		10	15	nC
Gate-Source Charge	Q <sub>gs</sub>			2		nC
Gate-Drain Charge	Q <sub>gd</sub>			3		nC

# CEP21A3/CEB21A3

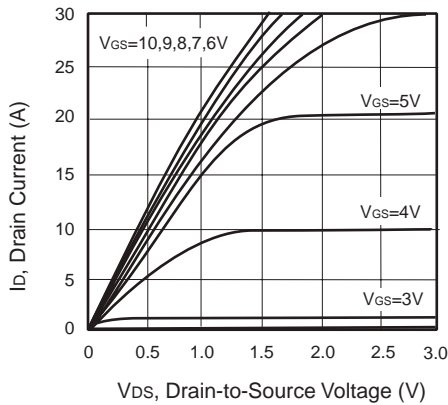
## ELECTRICAL CHARACTERISTICS (T<sub>c</sub>=25°C unless otherwise noted)

4

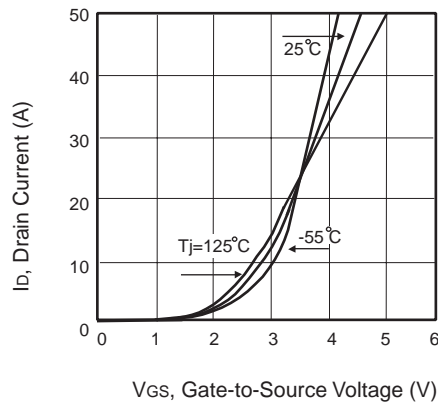
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS <sup>a</sup></b>						
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> = 12A		0.9	1.3	V

**Notes**

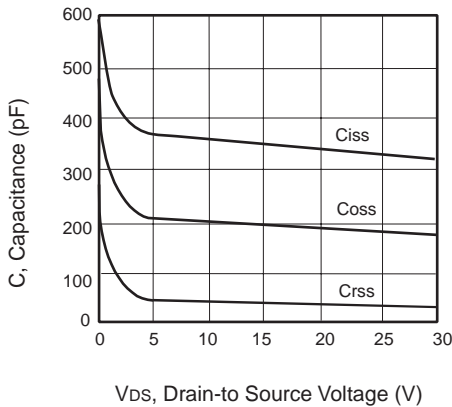
- a. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.



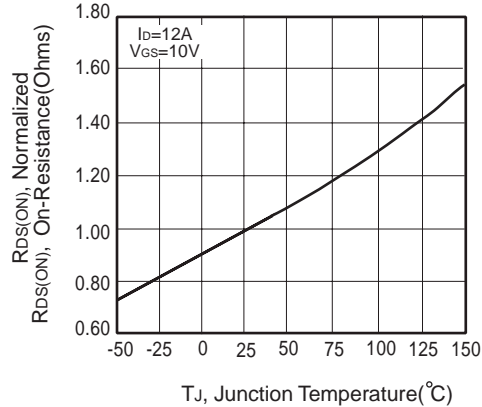
**Figure 1. Output Characteristics**



**Figure 2. Transfer Characteristics**



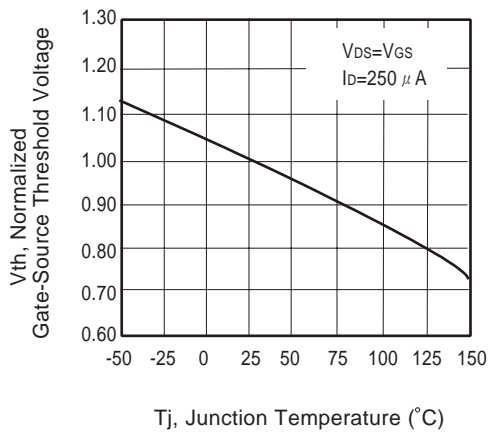
**Figure 3. Capacitance**



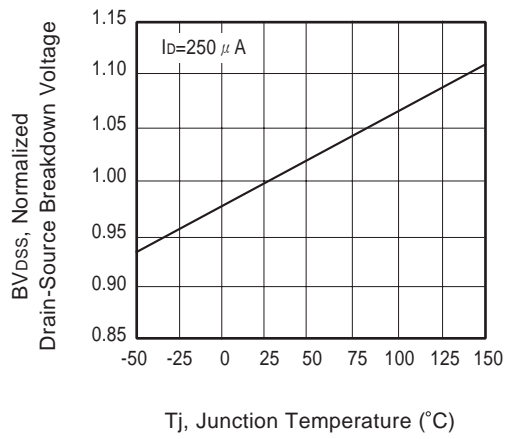
**Figure 4. On-Resistance Variation with Temperature**

# CEP21A3/CEB21A3

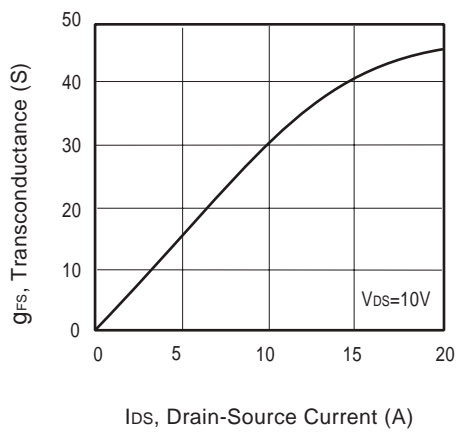
4



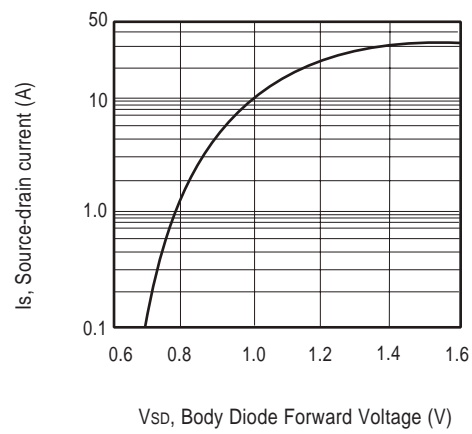
**Figure 5. Gate Threshold Variation with Temperature**



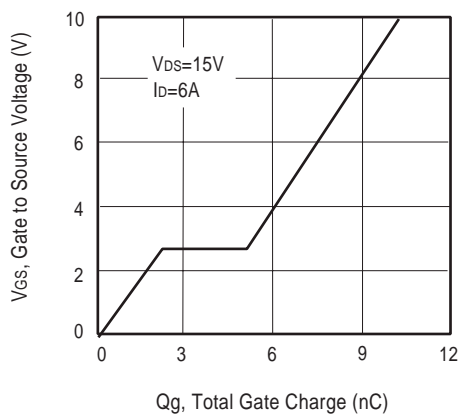
**Figure 6. Breakdown Voltage Variation with Temperature**



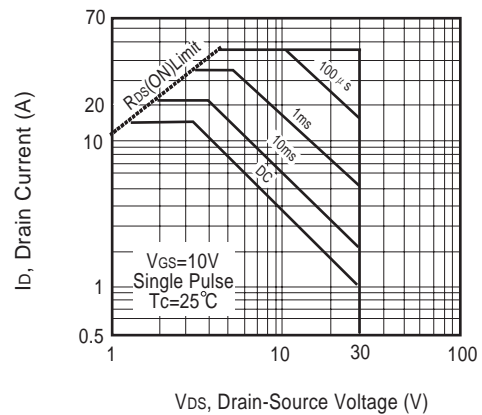
**Figure 7. Transconductance Variation with Drain Current**



**Figure 8. Body Diode Forward Voltage Variation with Source Current**



**Figure 9. Gate Charge**



**Figure 10. Maximum Safe Operating Area**

# CEP21A3/CEB21A3

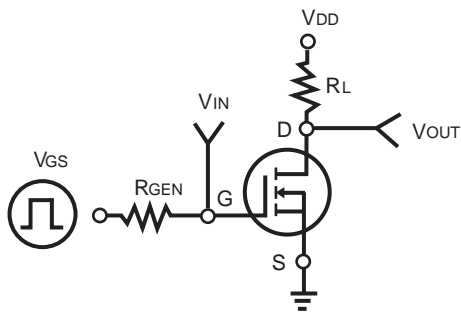


Figure 11. Switching Test Circuit

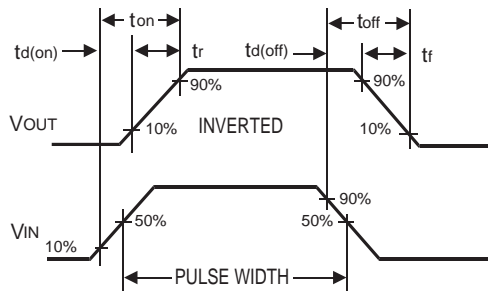


Figure 12. Switching Waveforms

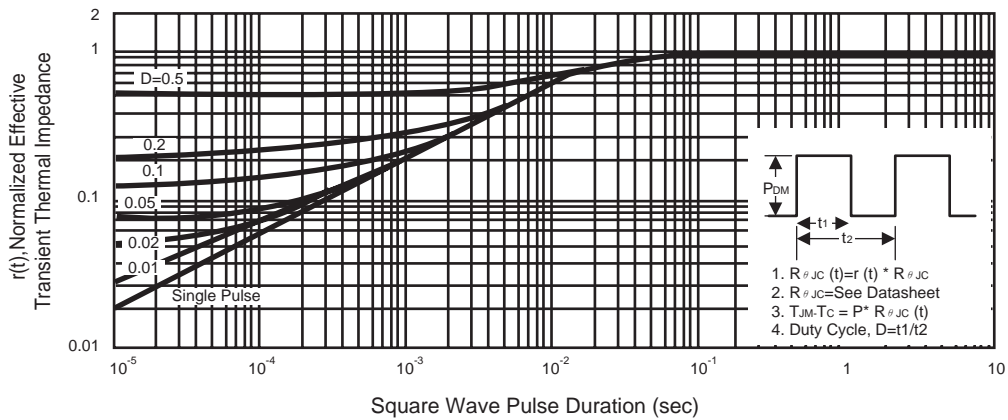


Figure 13. Normalized Thermal Transient Impedance Curve