

CEP8060LR/CEB8060LR



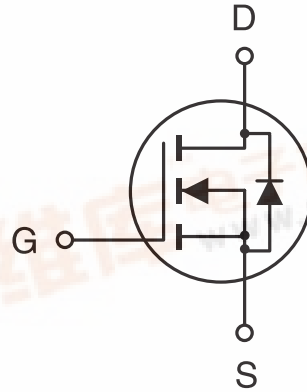
PRELIMINARY

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N-Channel Logic Level Enhancement Mode Field Effect Transistor

FEATURES

- 60V , 80A , $R_{DS(ON)}=9.0m\Omega$ @ $V_{GS}=10V$.
 $R_{DS(ON)}=12.0m\Omega$ @ $V_{GS}= 5V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- TO-220 & TO-263 package.



ABSOLUTE MAXIMUM RATINGS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	VDS	60	V
Gate-Source Voltage	VGS	±20	V
Drain Current-Continuous -Pulsed	ID	80	A
	IDM	225	A
Drain-Source Diode Forward Current	IS	80	A
Maximum Power Dissipation @Tc=25°C Derate above 25°C	PD	150	W
		1	W/°C
Operating and Storage Temperature Range	TJ, TSTG	-65 to 175	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W

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ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ	Max	Unit
DRAIN-SOURCE AVALANCHE RATING^a						
Single Pulse Drain-Source Avalanche Energy	E _{AS}	V _{DD} =25V, I _D =150A		430		mJ
Maximum Drain-Source Avalanche Current	I _{AS}	L=25μH		150		A
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V			25	μA
Gate-Body Leakage	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
ON CHARACTERISTICS^a						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1		2	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =37.5A			9	mΩ
		V _{GS} =5V, I _D =37.5A			12	mΩ
On-State Drain Current	I _{D(ON)}	V _{GS} =5V, V _{DS} =10V	60			A
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =37.5A		15		S
SWITCHING CHARACTERISTICS^b						
Turn-On Delay Time	t _{D(ON)}	V _{DD} =30V, I _D =75A, V _{GS} =5V R _{GEN} =10Ω		20	40	ns
Rise Time	t _r			460	600	ns
Turn-Off Delay Time	t _{D(OFF)}			125	150	ns
Fall Time	t _f			210	400	ns
Total Gate Charge	Q _g	V _{DS} =48V, I _D =75A, V _{GS} =5V		61	115	nC
Gate-Source Charge	Q _{gs}			15		nC
Gate-Drain Charge	Q _{gd}			18		nC

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ELECTRICAL CHARACTERISTICS ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS^b						
Input Capacitance	C_{ISS}	$V_{DS}=25\text{V}, V_{GS}=0\text{V}$ $f=1.0\text{MHz}$		3230	4200	pF
Output Capacitance	C_{OSS}			1230	1600	pF
Reverse Transfer Capacitance	C_{RSS}			615	800	pF
DRAIN-SOURCE DIODE CHARACTERISTICS^a						
Diode Forward Voltage	V_{SD}	$V_{GS}=0\text{V}, I_S=10\text{A}$		0.86	1.2	V

Notes

a. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

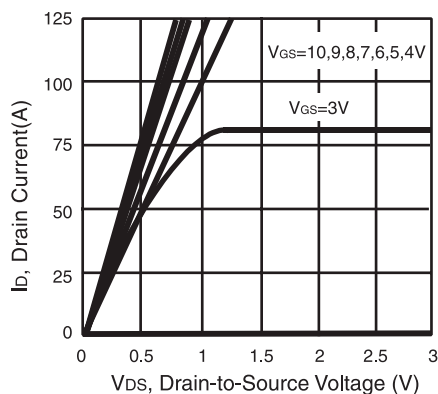


Figure 1. Output Characteristics

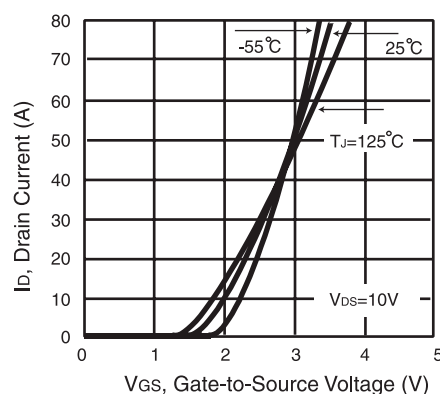


Figure 2. Transfer Characteristics

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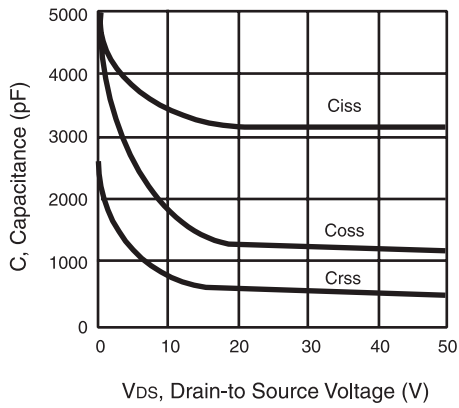


Figure 3. Capacitance

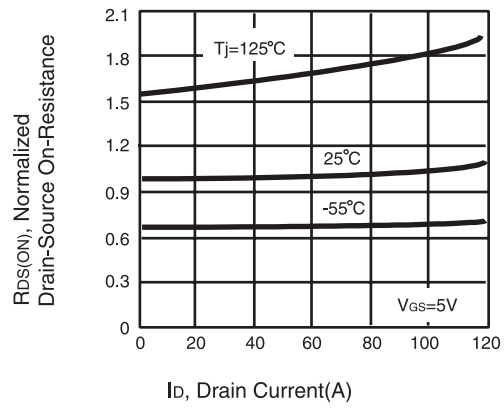


Figure 4. On-Resistance Variation with Drain Current and Temperature

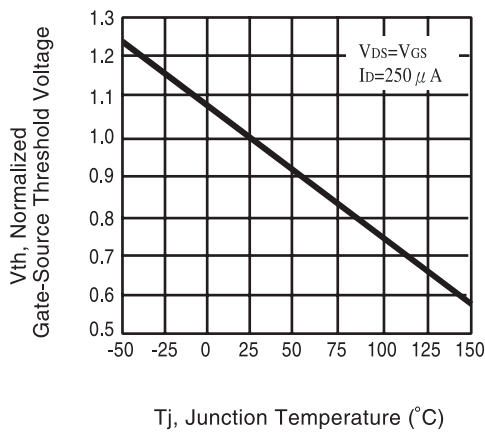


Figure 5. Gate Threshold Variation with Temperature

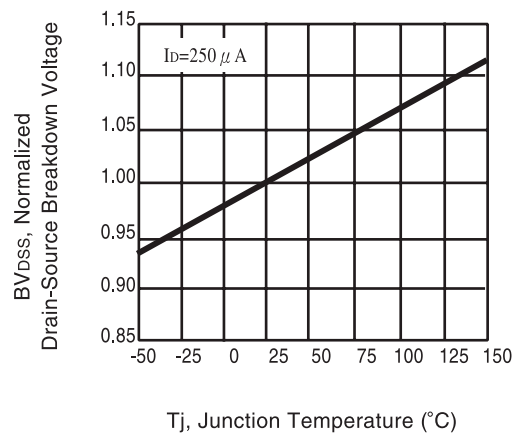


Figure 6. Breakdown Voltage Variation with Temperature

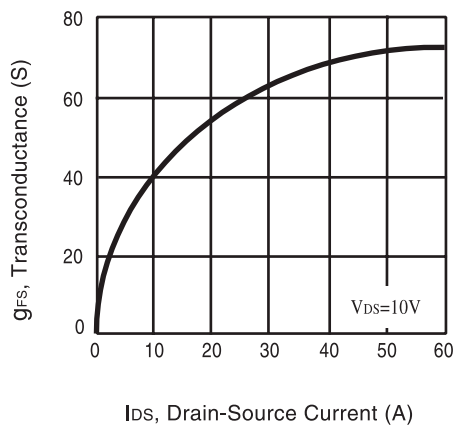


Figure 7. Transconductance Variation with Drain Current

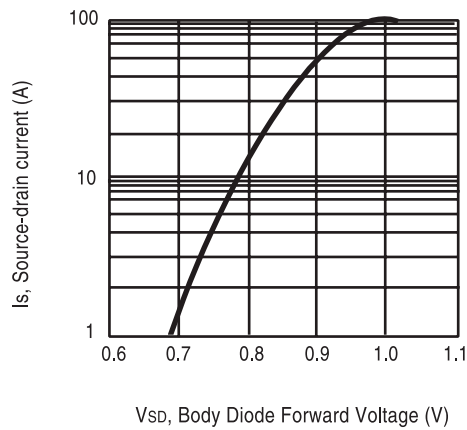


Figure 8. Body Diode Forward Voltage Variation with Source Current

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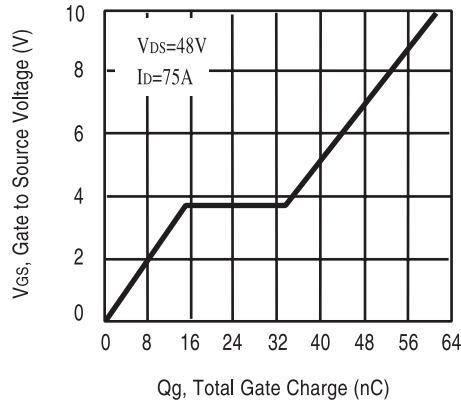


Figure 9. Gate Charge

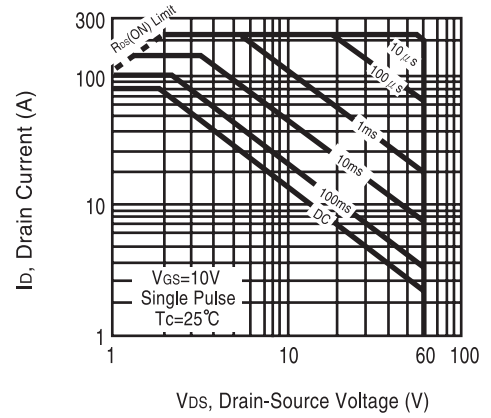


Figure 10. Maximum Safe Operating Area

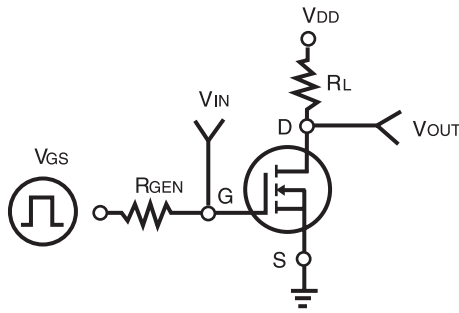


Figure 11. Switching Test Circuit

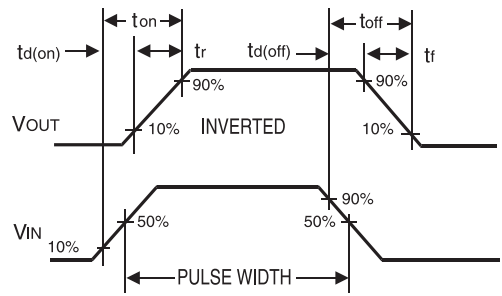


Figure 12. Switching Waveforms

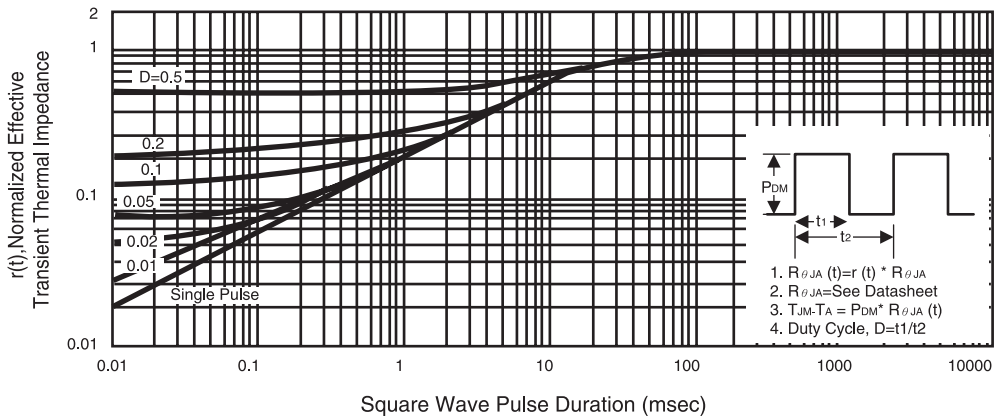


Figure 13. Normalized Thermal Transient Impedance Curve