

CED3055L5/CEU3055L5



PRELIMINARY

N-Channel Enhancement Mode Field Effect Transistor

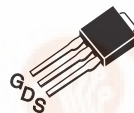
FEATURES

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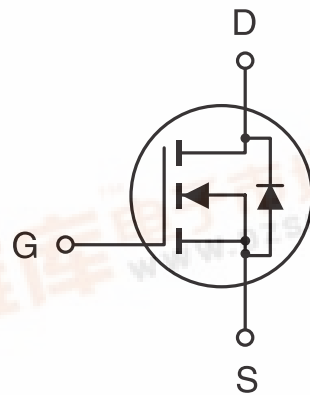
- 55V, 8A, $R_{DS(ON)}=150m\Omega$ @ $V_{GS}=10V$,
 $R_{DS(ON)}=180m\Omega$ @ $V_{GS}=5V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- TO-251 & TO-252 package.



CEU SERIES
TO-252AA(D-PAK)



CED SERIES
TO-251(L-PAK)



ABSOLUTE MAXIMUM RATINGS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	55	V
Gate-Source Voltage	V _{GS}	±20	V
Drain Current-Continuous -Pulsed	I _D	8	A
	I _{DM}	20	A
Drain-Source Diode Forward Current	I _S	8	A
Maximum Power Dissipation @T _c =25°C Derate above 25°C	P _D	20	W
		0.13	W/°C
Operating and Storage Temperature Range	T _J , T _{STG}	-65 to 175	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	R _{θJC}	7.5	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	°C/W

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ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	55			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 55V, V _{GS} = 0V			1	μA
Gate-Body Leakage	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V			±100	nA
ON CHARACTERISTICS^a						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1	1.5	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = 5V, I _D = 2A			180	mΩ
		V _{GS} = 10V, I _D = 4A			150	mΩ
On-State Drain Current	I _{D(ON)}	V _{DS} = 5V, V _{GS} = 10V	15			A
Forward Transconductance	g _{FS}	V _{DS} = 10V, I _D = 6A		8		S
DYNAMIC CHARACTERISTICS^b						
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V f = 1.0MHz		430	600	pF
Output Capacitance	C _{OSS}			126	200	pF
Reverse Transfer Capacitance	C _{RSS}			28	100	pF
SWITCHING CHARACTERISTICS^b						
Turn-On Delay Time	t _{D(ON)}	V _{DD} = 30V, I _D = 2.5A, V _{GS} = 10V, R _G = 10 Ω R _L = 12 Ω		5		ns
Rise Time	t _r			20		ns
Turn-Off Delay Time	t _{D(OFF)}			50		ns
Fall time	t _f			20		ns
Total Gate Charge	Q _g	V _{DS} = 48V, I _D = 8A, V _{GS} = 5V		14	17	nC
Gate-Source Charge	Q _{gs}			3		nC
Gate-Drain Charge	Q _{gd}			2		nC

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ELECTRICAL CHARACTERISTICS ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS^b						
Diode Forward Voltage	V_{SD}	$V_{GS} = 0V, I_S = 4A$		0.95	1.3	V

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Notes

- Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

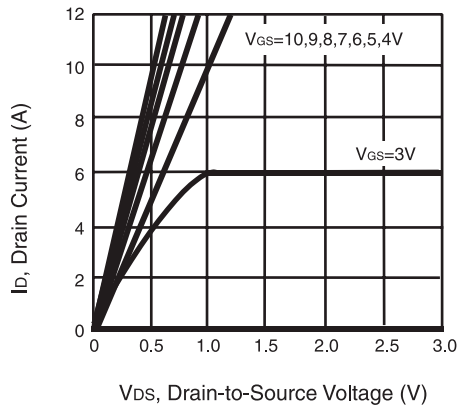


Figure 1. Output Characteristics

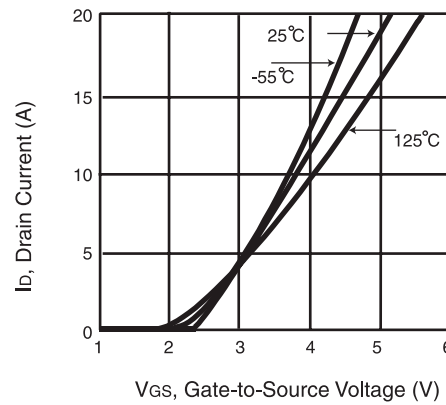


Figure 2. Transfer Characteristics

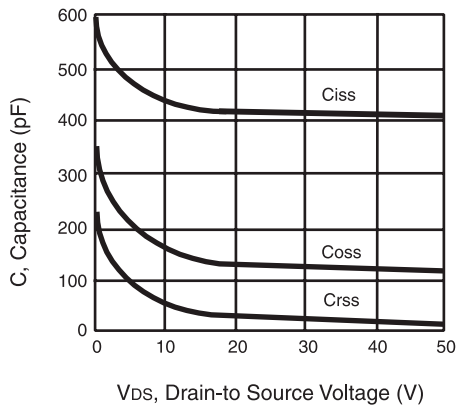


Figure 3. Capacitance

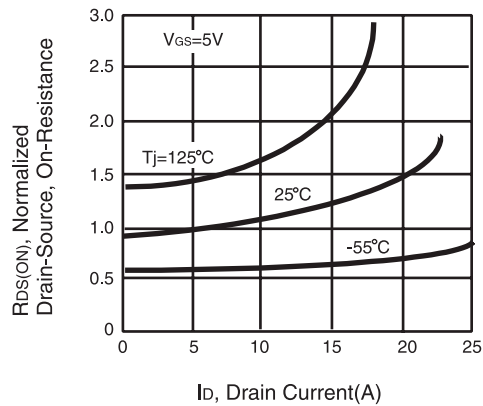


Figure 4. On-Resistance Variation with Drain Current and Temperature

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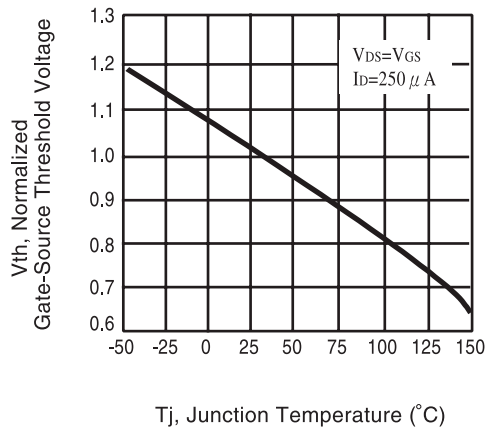


Figure 5. Gate Threshold Variation with Temperature

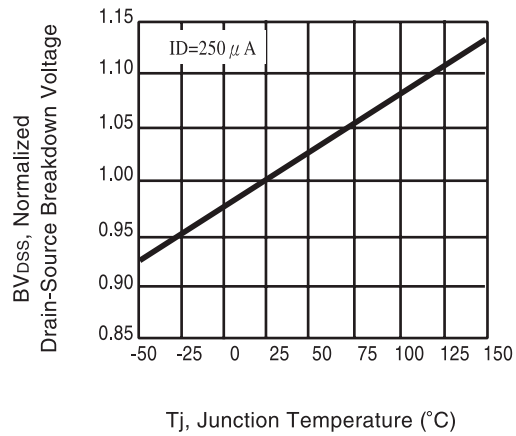


Figure 6. Breakdown Voltage Variation with Temperature

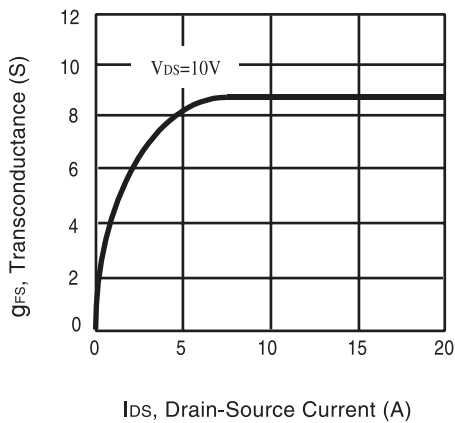


Figure 7. Transconductance Variation with Drain Current

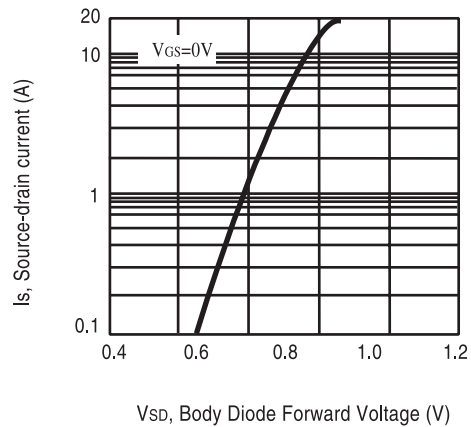


Figure 8. Body Diode Forward Voltage Variation with Source Current

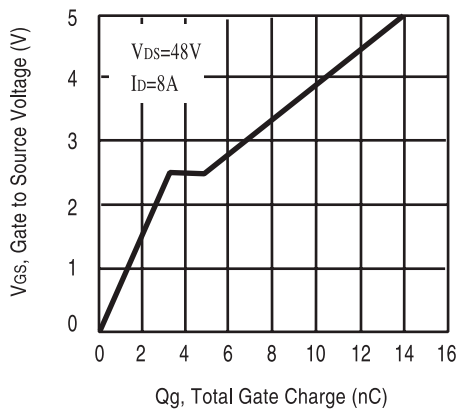


Figure 9. Gate Charge

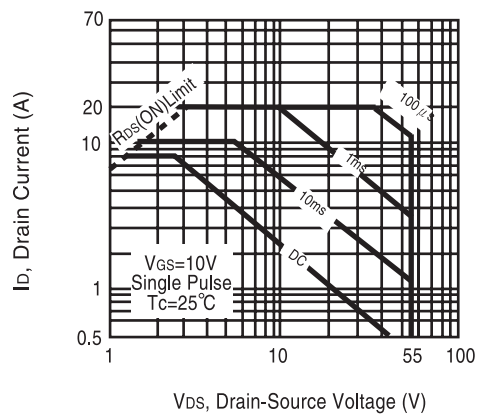


Figure 10. Maximum Safe Operating Area

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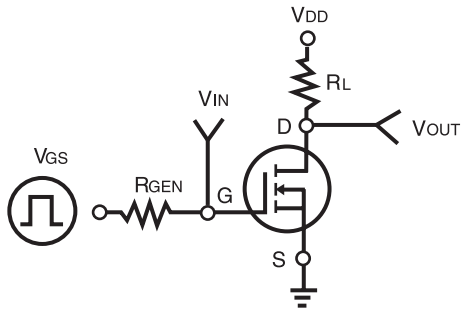


Figure 11. Switching Test Circuit

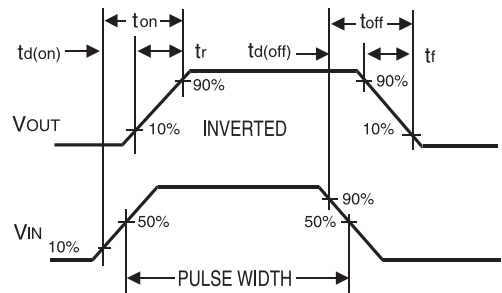


Figure 12. Switching Waveforms

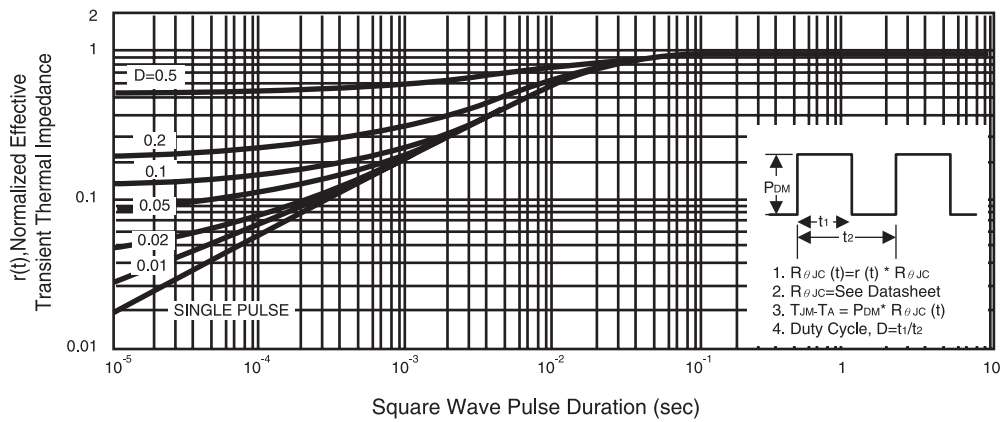


Figure 13. Normalized Thermal Transient Impedance Curve