TOSHIBA

TC55257CPI/CFI/CSPI/CFTI/CTRI-85L/10L

PRELIMINARY

SILICON GATE CMOS

32,768 WORD x 8 BIT STATIC RAM

Description

The TC55257CPI is a 262,144 bit CMOS static random access memory organized as 32,768 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 85ns.

When $\overline{CE}$ is a logical high, the device is placed in a low power standby mode in which the standby current is 2μA at room temperature. The TC55257CPI has two control inputs. Chip enable ($\overline{CE}$) allows for device selection and data retention control, while an output enable input ($\overline{OE}$) provides fast memory access. The TC55257CPI is suitable for use in microprocessor systems where high speed, low power, and battery backup are required. The TC55257CPI is guaranteed over an operating temperature range of -40 ~ 85°C so the TC55257CPI is suitable for use in wide operating temperature systems.

The TC55257CPI is offered in a standard dual-in-line 28-pin plastic package (0.6/0.3 inch width), a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 2μA (max.) at Ta = 25°C
- Single 5V power supply
- Access time (max.)

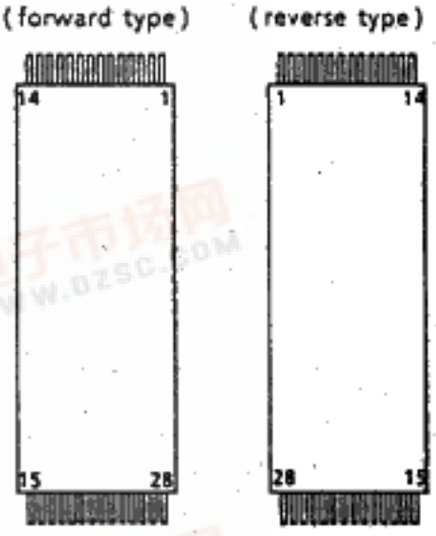
	TC55257CPI/CFI/CSPI/CFTI/CTRI	
	-85L	-10L
Access Time	85ns	100ns
$\overline{CE}$ Access Time	85ns	100ns
$\overline{OE}$ Access Time	45ns	50ns

- Power down feature: $\overline{CE}$
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Wide operating temperature: -40 ~ 85°C
- Package
  - TC55257CPI : DIP28-P-600
  - TC55257CFI : SOP28-P-450
  - TC55257CSPI : DIP28-P-300B
  - TC55257CFTI : TSOP28-P
  - TC55257CTRI : TSOP28-P-A

Pin Connection (Top View)

○ 28 PIN DIP & SOP

○ 28 PIN TSOP

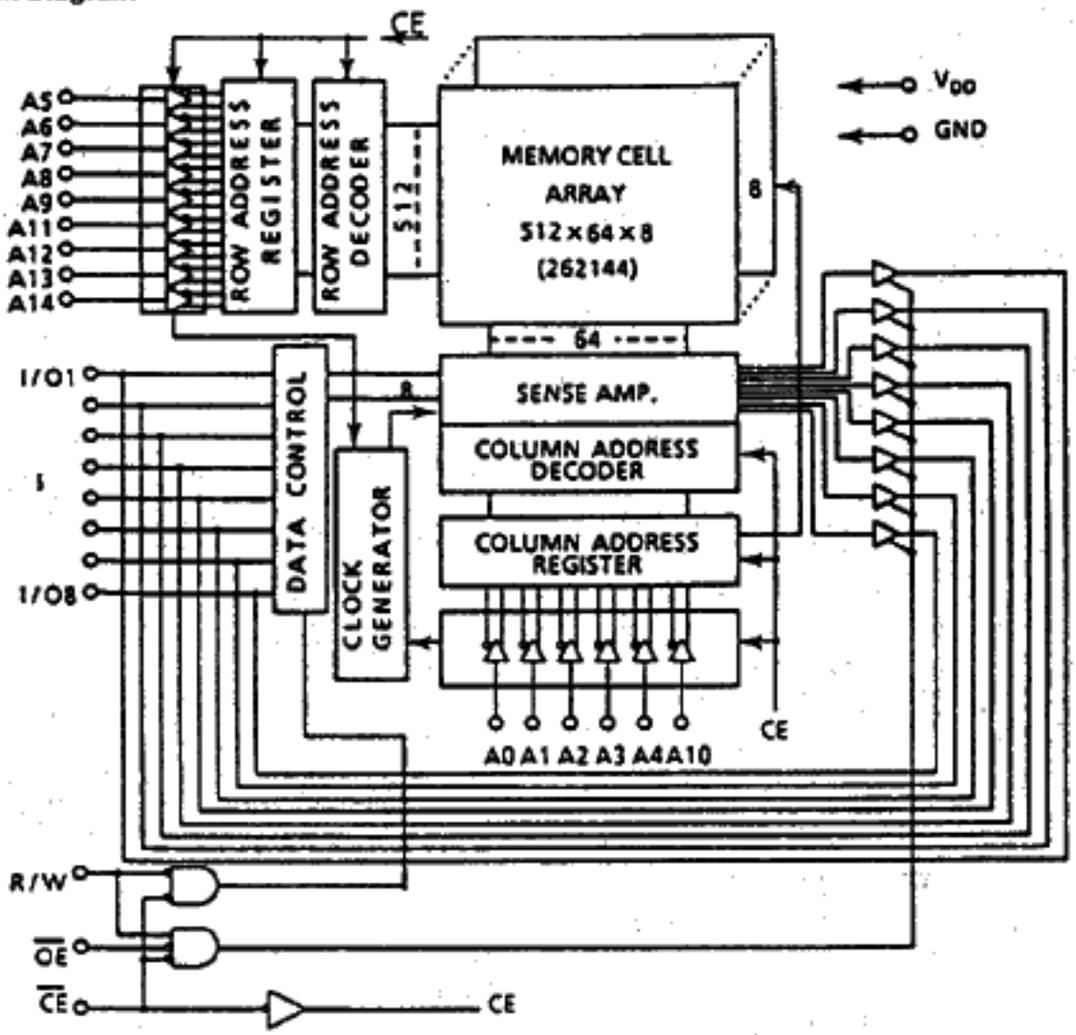


Pin Names

A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	$\overline{OE}$	A_{11}	A_9	A_8	A_{13}	R/W	V_{DD}	A_{14}	A_{12}	A_7	A_6	A_5	A_4	A_3
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE}$	A_{10}

Block Diagram



Operating Mode

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5* ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0/0.8/0.6**	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	-40 ~ 85	°C

* -3.0V with a pulse width of 50ns
** Package dependent: 0.6 inch 1.0W, 0.3 inch 0.8W, 0.45 inch 0.6W

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3*	–	0.6	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	

* -3.0V with a pulse width of 50ns

DC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}		–	–	±1.0	µA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}		–	–	±1.0	µA
I_{OH}	Output High Current	V_{OH} = 2.4V		-1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		4.0	–	–	mA
I_{DDO1}	Operating Current	$\overline{CE}$ = V_{IL} R/W = V_{IH} Other Input = V_{IH}/V_{IL} I_{OUT} = 0mA	t_{cycle} = 1µs	–	10	–	mA
			t_{cycle} = Min. cycle	–	–	70	
I_{DDO2}		$\overline{CE}$ = 0.2V R/W = V_{DD} - 0.2V Other Input = V_{DD} - 0.2V/0.2V I_{OUT} = 0mA	t_{cycle} = 1µs	–	5	–	
			t_{cycle} = Min. cycle	–	–	60	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}		–	–	3	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V V_{DD} = 2.0V ~ 5.5V	Ta = -40 ~ 85°C	–	–	30	µA
			Ta = 25°C	–	–	2	

Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC55257CPI/CFI/CSPI/CFTI/CTRI				UNIT
		-85L		-10L		
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	–	100	–	ns
t_{ACC}	Address Access Time	–	85	–	100	
t_{CO}	$\overline{CE}$ Access Time	–	85	–	100	
t_{OE}	Output Enable to Output in Valid	–	45	–	50	
t_{COE}	Chip Enable ($\overline{CE}$) to Output in Low-Z	5	–	5	–	
t_{OEE}	Output Enable to Output in Low-Z	0	–	0	–	
t_{OD}	Chip Enable ($\overline{CE}$) to Output in High-Z	–	30	–	50	
t_{ODO}	Output Enable to Output in High-Z	–	30	–	40	
t_{OH}	Output Data Hold Time	10	–	10	–	

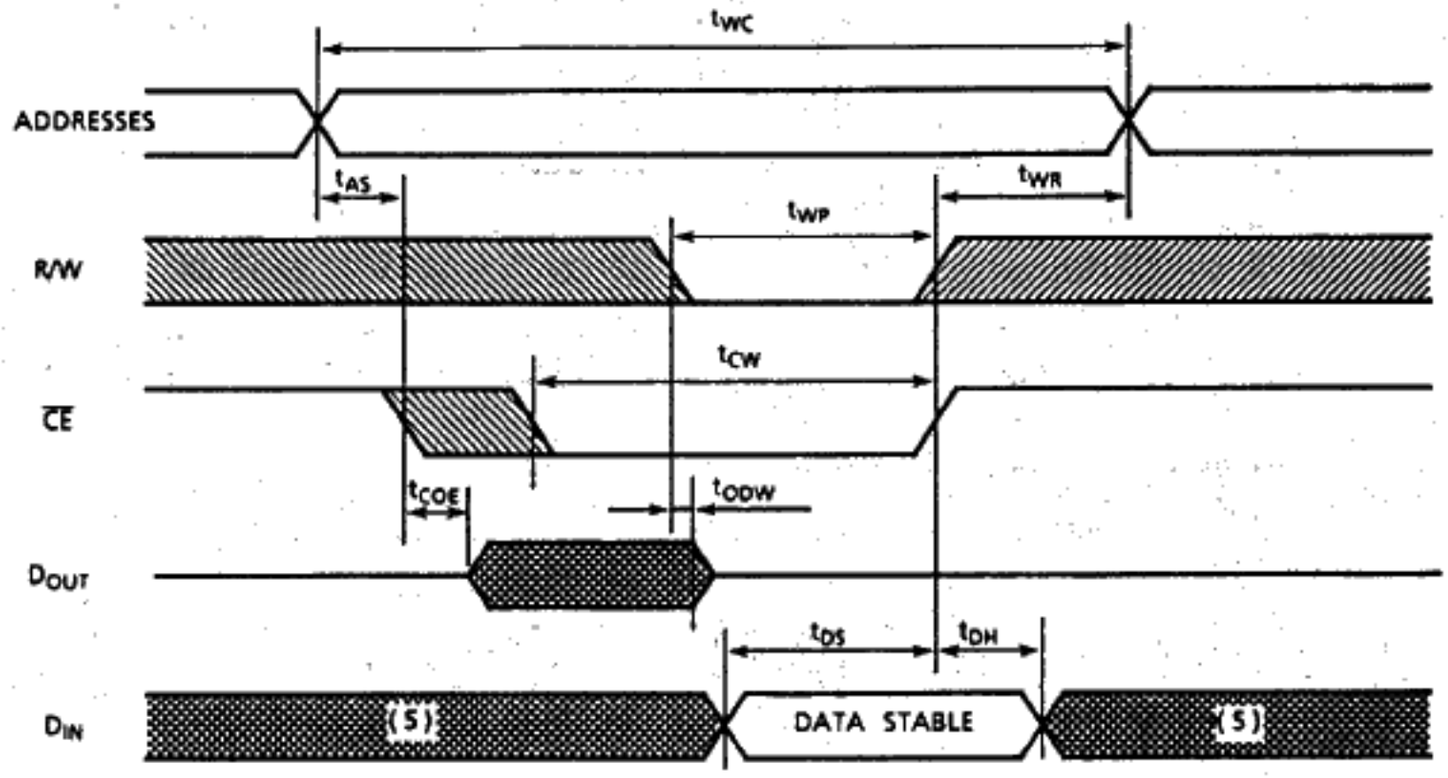
Write Cycle

SYMBOL	PARAMETER	TC55257CPI/CFI/CSPI/CFTI/CTRI				UNIT
		-85L		-10L		
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	–	100	–	ns
t_{WP}	Write Pulse Width	60	–	70	–	
t_{CW}	Chip Selection to End of Write	65	–	90	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	5	–	5	–	
t_{OOW}	R/W to Output in High-Z	–	30	–	50	
t_{OEW}	R/W to Output in Low-Z	0	–	0	–	
t_{DS}	Data Setup Time	40	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	

AC Test Conditions

Input Pulse Levels	2.6V/0.4V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	1 TTL Gate and C_L = 100pF

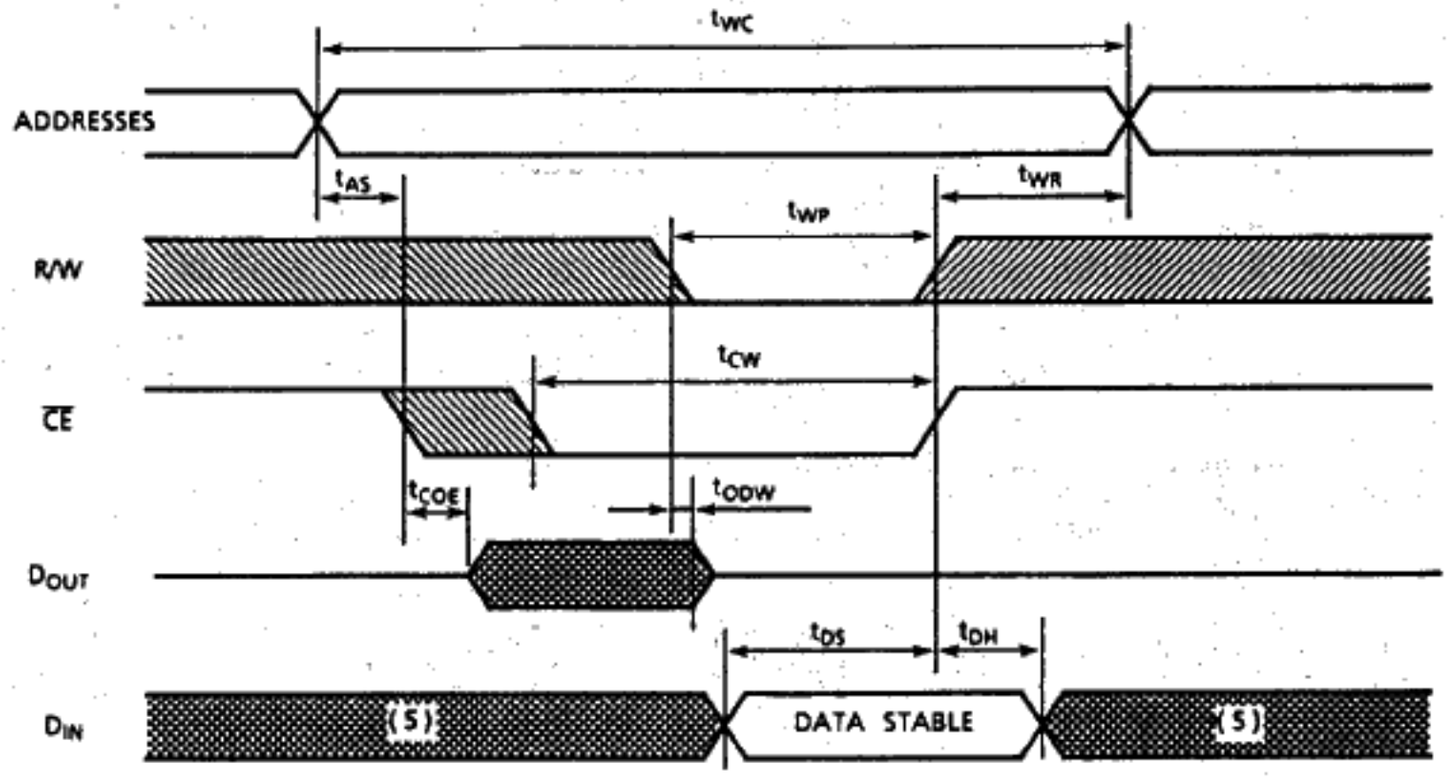
Write Cycle 2 [4] ($\overline{CE}$ Controlled Write)



Notes:

1. R/W is high for read cycles.
2. If the $\overline{CE}$ low transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the $\overline{CE}$ high transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If $\overline{OE}$ is high during a write cycle, the outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; therefore input signals of opposite phase must not be applied.

Write Cycle 2 [4] ($\overline{CE}$ Controlled Write)



Notes:

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4. If $\overline{OE}$ is high during a write cycle, the outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; therefore input signals of opposite phase must not be applied.

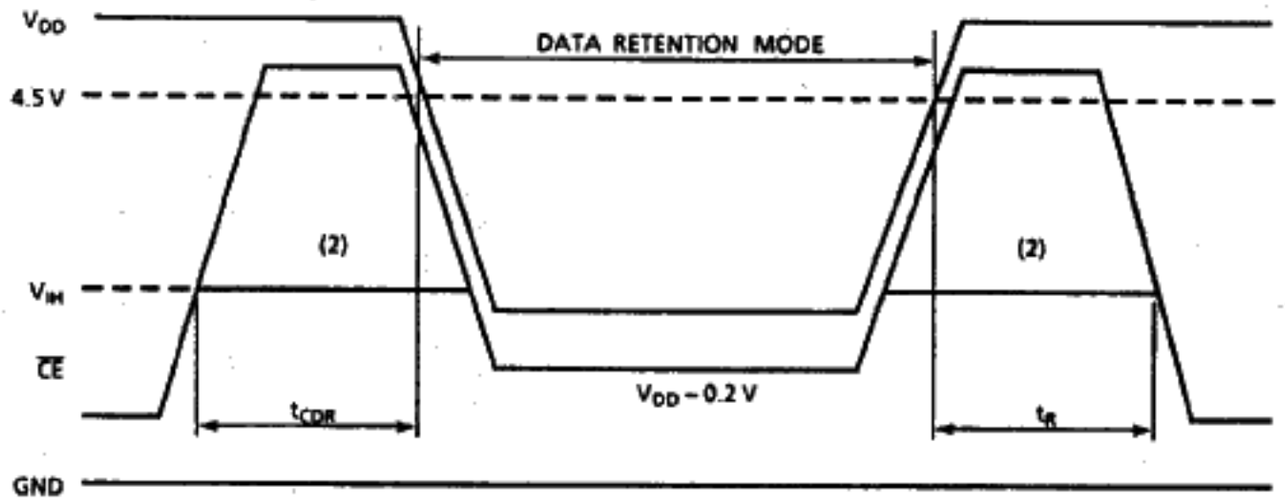
Data Retention Characteristics (Ta = -40 ~ 85°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DH} = 3.0V	–	–	15*	µA
		V_{DH} = 5.5V	–	–	30	
t_{CDR}	Chip Deselect to Data Retention Mode		0	–	–	ns
t_R	Recovery Time		$t_{RC(1)}$	–	–	

Note (1): Read Cycle Time

*2µA (max.) Ta = 0 ~ 40°C

$\overline{CE}$ Controlled Data Retention Mode



Note (2): If the V_{IH} of $\overline{CE}$ is 2.4V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.6V.